Heterogeneously Integrated Power Stages enable Breakthrough Power Density and Speed

APEC Industry Session: Silicon and WBG Power Devices for High Frequency Topologies
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Agenda

• Today’s Efficiency vs. Density Tradeoff

• Sarda Introduction and Technology

• Sarda’s HIPS Approach

• 12Vin HIPS
  - Present: Prototype Performance
  - Future: Progression of Improvements

• 48Vin HIPS
  - Single-stage vs. Two-stage Approaches

• Conclusion
Typical Voltage Regulator Density – Efficiency Tradeoff

12Vin MOSFET-based VR Example

- Efficient Solutions, but Bulky & Slow
- Push to higher Fsw and smaller magnetics, but with huge tradeoff in efficiency
MOSFET-based VRs Density vs. Efficiency Tradeoff

12Vin, 1.2Vout, 10-40A capability
GaN FETs Don’t Significantly Increase Density or Efficiency

12Vin, 1.2Vout, 10-40A capability

![Graph showing current density vs. full load efficiency for different power trains and frequencies.](image-url)
New Paradigm in the VR Density – Efficiency Tradeoff

12Vin VR Example

HIPS enables dramatic shift “up and to the right”
Heterogeneously Integrated Power Stage (HIPS)

- Integrates in 2.5D SiP to minimize switching power loss:
  - GaAs FET die
  - Si Driver die
  - Critical passive components
- Use 3rd party PWM controllers, Inductors and Capacitors
- Lowest Switching Loss
- Supports up to 100V
- Leverages $8B GaAs industry
  - HIPS similar to integrated multi-band RF power amplifiers
  - Integrates GaAs, silicon and passives in compact, low-cost module
## GaAs FET Advantages for <100V Input VRs

<table>
<thead>
<tr>
<th>Benefit</th>
<th>GaAs FETs</th>
<th>GaN-on-Silicon FETs</th>
<th>Vertical MOSFETs</th>
<th>Electron Mobility (cm²/Vs)</th>
<th>R&lt;sub&gt;DS(on) * Q&lt;sub&gt;G&lt;/sub&gt; (mΩ-nC) 80V 25V</th>
<th>R&lt;sub&gt;DS(on) * Q&lt;sub&gt;OSS&lt;/sub&gt; (mΩ-nC) 80V 25V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast Switching</td>
<td>9,000</td>
<td>1,800</td>
<td>1,400</td>
<td>35 → 20 16 → 8</td>
<td>35 → 20 16 → 8</td>
<td>45 → 24 10 → 8</td>
</tr>
<tr>
<td>Reduced Switching loss (ability to go to higher Fsw)</td>
<td></td>
<td>&gt;100 20-30</td>
<td></td>
<td>30-50</td>
<td>30-50</td>
<td></td>
</tr>
<tr>
<td>Reduced Switching loss (ability to go to higher Fsw)</td>
<td></td>
<td>&gt;100 20-30</td>
<td></td>
<td>&gt;300 25-45</td>
<td>&gt;300 25-45</td>
<td></td>
</tr>
<tr>
<td>No Qrr loss</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Monolithic integration of UFET / LFET (reduced parasitics)</td>
<td>Lateral</td>
<td>Lateral</td>
<td>Vertical</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Additional Information on Sarda’s HIPS developments:
- APEC 2013: “The gFET™ Switch: A New Low Voltage High Speed GaAs HEMT for Switching Applications”, Robert White, et al.
GaAs FETs: Lowest $R_{DS(on)} \cdot Q_G$

![Graph showing comparison of GaAs FETs with the lowest $R_{DS(on)} \cdot Q_G$](image)

- **Sarda GaAs**
  - 0.5µm Qorvo
  - Measured (2012)
- **GaN-on-Silicon**
- **MOSFETs**
- **Sarda**
  - 0.4µm Sony GaAs
  - Measured (2016)
- **Sarda**
  - 0.15µm Sony GaAs
  - Projected

**Graph Details**
- Vertical axis: $R_{DS(on)} \cdot Q_G$ (mΩ • nC)
- Horizontal axis: BVds (V)

The graph illustrates the comparison of GaAs FETs with the lowest $R_{DS(on)} \cdot Q_G$ alongside GaN-on-Silicon and MOSFETs, highlighting specific data points and trends.
GaAs FETs: Lowest $R_{DS(on)} \cdot Q_{OSS}$

- GaAs FETs: Lowest $R_{DS(on)}$ measured in 2016.
- Sarda GaAs 0.5μm Qorvo measured in 2012.
- GaN-on-Silicon MOSFETs and GaN-on-Silicon.

Graph showing the relationship between $R_{DS(on)} \cdot Q_{OSS}$ and BVds (V) with data points for different technologies.
Sarda's CMOS Driver IC

- Integrates logic functions (so GaAs integrates only FETs)
- Transparenlty implements GaAs-specific gate drive
- Provides standard interface to controller

**Major Functions**

- **2-phase Driver Output Stage** for depletion-mode GaAs FETs
- **Negative Charge Pumps** to turn off GaAs FETs at startup, shutdown, fault, etc
- **Positive Charge Pumps** to ensure adequate upper drive during periods of inactivity
- **Synchronous Rectifiers** to eliminate BOO Schottky diodes
- **Level Shifters** for high-side signals referenced to SX
- **Vin Switch** to prevent normally-on GaAs FETs shorting input
- **Gate Drive Control** (deadtime adjust) to trim deadtime minimally
- **Control Logic / POR** to handle all system-level start-up, shutdown, fault, and mode scenarios
- **Thermal Protection**
HIPS Integration Minimizes Parasitic Impedances

Minimize
- Common source inductance
- Gate drive loop
- High frequency input commutation current loop

Approach
- Monolithic integration of GaAs FETs
- Co-pack GaAs FETs and drivers
- Co-pack GaAs FETs and bypass capacitors
HIPS 2.5D System-in-Package First Prototype Details

<table>
<thead>
<tr>
<th>Package size / Type</th>
<th>4.5 x 7.2 mm LGA-SIP</th>
</tr>
</thead>
<tbody>
<tr>
<td># of embedded die</td>
<td>2 (GaAs FET + driver)</td>
</tr>
<tr>
<td># of Passive Component</td>
<td>24 Passives</td>
</tr>
<tr>
<td>(Top of substrate surface)</td>
<td></td>
</tr>
<tr>
<td>Component Sizes</td>
<td>10ea 01005</td>
</tr>
<tr>
<td></td>
<td>10ea 0402</td>
</tr>
<tr>
<td></td>
<td>4 ea  0201</td>
</tr>
<tr>
<td>Substrate Thickness</td>
<td>560 um ± 10%</td>
</tr>
<tr>
<td></td>
<td>320um core</td>
</tr>
<tr>
<td>Die thickness</td>
<td>200 um Max.</td>
</tr>
<tr>
<td>Surface finish (Die DAP)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td>Surface finish (Land Pad)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td>Strip Size</td>
<td>188x64mm</td>
</tr>
<tr>
<td>Substrate Metal layers</td>
<td>4 Layer</td>
</tr>
</tbody>
</table>

Assembly Layout

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.
HIPS Prototypes Demonstrate Low Switching Loss

HIPS
7.2x4.5x1mm
Cross-Section

HIPS
Photos

HIPS
Evaluation
Board

Voltage Regulator Efficiency
including 200nH inductors

10MHz, 12Vin, ~3.8Vout

2-5MHz, 12Vin, ~1.8Vout

Next step: reduce conduction loss; FETs sized for 5A/phase

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HIPS Prototypes Demonstrate Benefit of Integration

Driver prototype
Bypass caps
GaAs FET die

Driver & GaAs dice embedded in substrate

Minimal current loops

12Vin, 1.2Vout, 2MHz

Efficiency
0 4 8 12 16
Load (A)

SDT2312_EVAL1 (HIPS)
SDT_EVAL2 (Discrete)
HIPS Prototypes at 12Vin, 10MHz

Sub-ns switching edges

Efficiency

12Vin, ~3.8Vout, 10MHz

Load (A)

0 1 2 3 4 5 6 7 8 9

65% 70% 75% 80% 85% 90% 95%

Modeled Power Loss Breakdown

12Vin, ~3.8Vout, 10MHz

Power Loss (W)

0 1 2 3 4

0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0

Load (A)

0 1 2 3 4 5 6 7 8 9

Measured
Modeled

Power (W)

0 1 2 3 4

0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0

Load (A)
First Products in Family of HIPS

<table>
<thead>
<tr>
<th>HIPS</th>
<th>Input Voltage (V)</th>
<th>Output Voltage (V)</th>
<th>Output Current (A)</th>
<th>Phase Count</th>
<th>Switching Frequency (MHz)</th>
<th>Data Center Applications</th>
</tr>
</thead>
</table>
| Kitty Hawk  | 8 - 16            | 0.3 - 3            | 15 - 25            | 2           | 2 - 5                     | • 48V$_{in}$ two-stage VR (2$^{nd}$ stage)  
• 12V$_{in}$ VR or POL  
• Highest density & transient response                                                   |
| Nags Head   | 40 - 60           | 0.7 - 3            | 15 - 20            | 1           | 0.3 - 1                   | • 48V$_{in}$ single-stage VR or POL  
• Highest density & efficiency                                                             |
| Wrightsville| 40 - 60           | 3 - 15             | 10 - 15            | 1           | 0.3 - 1                   | • 48V$_{in}$ two-stage VR (1$^{st}$ stage) or POL  
• Highest density & efficiency                                                             |

**Thermal Design Current (TDC)**

For thermal solution

\[ I_{\text{max}} \gg I_{\text{TDC}} \]
Planned Progression of Improvements

**FET Efficiency**

Vin = 12V
Vout = 1.2V
Fsw = 2MHz

- **Kitty Hawk**
- **HIPS Rev2**
- **HIPS Rev1**

<table>
<thead>
<tr>
<th>now</th>
<th>Q2 ’17</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GaAs process</strong></td>
<td>Qorvo 0.5µ</td>
</tr>
<tr>
<td><strong>Package Size (mm)</strong></td>
<td>4.5x7.2</td>
</tr>
<tr>
<td><strong>UFET Rdson (mΩ)</strong></td>
<td>40</td>
</tr>
<tr>
<td><strong>LFET Rdson (mΩ)</strong></td>
<td>10</td>
</tr>
<tr>
<td><strong>Rdson-Qg (mΩ-nC)</strong></td>
<td>12</td>
</tr>
<tr>
<td><strong>Rdson-Qoss (mΩ-nC)</strong></td>
<td>30</td>
</tr>
<tr>
<td><strong>tsw_UFET (ns)</strong></td>
<td>0.6</td>
</tr>
<tr>
<td><strong>tsw_LFET (ns)</strong></td>
<td>1.2</td>
</tr>
<tr>
<td><strong>Driver</strong></td>
<td>process drive strength Vin switch</td>
</tr>
</tbody>
</table>

**Driver Die**

- **Rev1**: 4.5mm x 7.2mm
- **Rev2**: 5mm x 5.5mm

**GaAs Die**

- **Rev1**: 4.5mm x 7.2mm
- **Rev2**: 5mm x 5.5mm

**Existing Prototypes**

**Projections**
Kitty Hawk HIPS

HIPS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_{\text{out}} )</td>
<td>200\text{nH}, 2\text{m\Omega}, 4\times 4\times 3\text{mm}</td>
</tr>
<tr>
<td>( F_{\text{sw}} )</td>
<td>2MHz</td>
</tr>
<tr>
<td>( I_{\text{TDC}} )</td>
<td>24A (2\times 12A)</td>
</tr>
<tr>
<td>Efficiency at ( I_{\text{TDC}} )</td>
<td>89.5%</td>
</tr>
<tr>
<td>( C_{\text{out}} )</td>
<td>60\mu\text{F}</td>
</tr>
<tr>
<td>( V_{\text{out}} ) slew rate</td>
<td>180mV/\mu\text{s}</td>
</tr>
<tr>
<td>Density</td>
<td>70mA/mm(^3) (210mA/mm(^2))</td>
</tr>
</tbody>
</table>

FET parameters, per phase

<table>
<thead>
<tr>
<th></th>
<th>UFET</th>
<th>LFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>BVds</td>
<td>25V</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{DS(on)}} )</td>
<td>10.8m\text{\Omega}</td>
<td>3.1m\text{\Omega}</td>
</tr>
<tr>
<td>( Q_{\text{g}} )</td>
<td>0.83nC</td>
<td>2.9nC</td>
</tr>
<tr>
<td>( R_{\text{DS(on)}} \cdot Q_{\text{g}} )</td>
<td>9m\text{\Omega}\cdot\text{nC}</td>
<td>9m\text{\Omega}\cdot\text{nC}</td>
</tr>
<tr>
<td>( Q_{\text{oss}} )</td>
<td>0.83nC</td>
<td>2.9nC</td>
</tr>
<tr>
<td>( Q_{\text{rr}} )</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>( t_{\text{on}} )</td>
<td>0.65ns</td>
<td>1.3ns</td>
</tr>
<tr>
<td>( t_{\text{off}} )</td>
<td>0.65ns</td>
<td>1.3ns</td>
</tr>
<tr>
<td>( t_{\text{dead}} )</td>
<td>1ns</td>
<td>1ns</td>
</tr>
</tbody>
</table>

Projected Efficiency
\( F_{\text{sw}} = 2\text{MHz} \)

Efficiency at \( 12V_{\text{in}} \)

Powerstage
VR

VR

Power Loss (W)

- Switching loss: 0.50W
- Charge loss: 0.16W
- Conduction loss: 1.66W

HIPS at 24A
### Kitty Hawk vs. Low-Profile Modules

#### Powerstage

<table>
<thead>
<tr>
<th>Powerstage</th>
<th>Kitty Hawk HIPS</th>
<th>2x Vendor A</th>
<th>Vendor B - 1</th>
<th>Vendor B - 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Switching Frequency</strong></td>
<td>3MHz</td>
<td>4MHz</td>
<td>650kHz</td>
<td>1.2MHz</td>
</tr>
<tr>
<td><strong>I\textsubscript{DC}</strong></td>
<td>24A (2x12A)</td>
<td>20A</td>
<td>20A</td>
<td>24A</td>
</tr>
<tr>
<td><strong>1.2V\text{out} Efficiency (10A / 20A)</strong></td>
<td>90% / 88.5%</td>
<td>85% / 81%</td>
<td>83% / 81%</td>
<td>80% / 78%</td>
</tr>
<tr>
<td><strong>C\text{out}</strong></td>
<td>50μF</td>
<td>0μF ext (185μF int)</td>
<td>230μF</td>
<td>70μF</td>
</tr>
<tr>
<td><strong>V\text{out} Slew rate</strong></td>
<td>200mV/μs</td>
<td>60mV/μs</td>
<td>45mV/μs</td>
<td>140mV/μs</td>
</tr>
<tr>
<td><strong>Board area</strong></td>
<td>120mm\textsuperscript{2}</td>
<td>270mm\textsuperscript{2}</td>
<td>370mm\textsuperscript{2}</td>
<td>335mm\textsuperscript{2}</td>
</tr>
<tr>
<td><strong>Height</strong></td>
<td>1.5mm</td>
<td>2.3mm</td>
<td>1.9mm</td>
<td>1.8mm</td>
</tr>
<tr>
<td><strong>Current Density</strong></td>
<td>130mA/mm\textsuperscript{3}</td>
<td>32mA/mm\textsuperscript{3}</td>
<td>29mA/mm\textsuperscript{3}</td>
<td>40mA/mm\textsuperscript{3}</td>
</tr>
</tbody>
</table>
HIPS: Highest Efficiency, Density & Transient Response

12Vin, 1.2Vout, 10-40A capability
HIPS: Highest Efficiency, Density & Transient Response
12Vin, 1.2Vout, 10-40A capability

HIPS enables dramatic shift “up and to the right”
Sarda HIPS Resolves Challenges for 48Vin to 1Vout

**Single Stage**

- **Non-Isolated Buck**
  - 48V → 1V

**Advantages:**
- Simple
- More Efficient
- Smaller

**Challenges:**
- Low Duty Cycle
  - 48Vin-to-1V → ~2%
  - UFET on-time ~25nsec at 800kHz
- Switching Losses
- Transient Response

**Two Stage**

- **Non-Isolated Buck**
  - 48V → 12V
- **Non-Isolated Buck**
  - 12V → 1V

**Advantages:**
- 2\textsuperscript{nd} Stage can provide fast transient response
- Duty cycles reasonable

**Challenges:**
- Two Stages of power loss
- Size, especially if 1\textsuperscript{st} Stage is running at 100-200kHz (MOSFET-based)

*GaAs FOMs and HIPS open up new possibilities*
HIPS Enables $48V_{in}$-to-Load Single Stage Buck Regulators

MOSFETs are not practical for $48V_{in}$-to-load single-stage buck regulators due to:

- High switching & charge losses
- Low output current

**FET Efficiency**

- **HIPS (GaAs FETs)**
- **GaN FETs**
- **MOSFETs**

**Power Loss (W)**

- **GaAs FETs (HIPS)**
  - 500kHz
  - 12A
  - 0.34W
  - 0.20W
  - 0.51W

- **GaN FETs**
  - 500kHz
  - 12A
  - 1.02W
  - 0.82W
  - 0.29W

- **MOSFETs**
  - 500kHz
  - 5A
  - 1.01W
  - 1.06W
  - 0.29W

**48V_{in}**

**1.8V_{out}**

**500kHz**
Nags Head HIPS
Defined for 48V-to-1V Single Stage

- **$L_{\text{out}}$**: 300nH, 1.1mΩ, 7.2x7.5x7mm
- **$F_{\text{sw}}$**: 500kHz
- **$I_{\text{TDC}}$**: 15A
- **Efficiency at $I_{\text{TDC}}$**: 89%
- **$C_{\text{out}}$**: 300μF
- **$V_{\text{out}}$ slew rate**: 15mV/μs
- **Density**: 37mA/mm$^3$ (111mA/mm$^2$)

### Powerstage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Power Loss (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$54.5V_{\text{in}}$</td>
<td>0.42W</td>
</tr>
<tr>
<td>$1.0V_{\text{out}}$</td>
<td>0.22W</td>
</tr>
</tbody>
</table>

### FET Switching loss

- $t_{\text{on}}$: 1ns
- $t_{\text{off}}$: 1ns
- $t_{\text{dead}}$: 3ns

### FET Conduction loss

- $R_{\text{DS(on)}}$: 25mΩ
- $Q_{\text{g}}$: 0.8nC
- $Q_{\text{oss}}$: 0.96nC
- $Q_{\text{rr}}$: -

### FET Charge loss

- $R_{\text{DS(on)}}$: 1.8mΩ
- $Q_{\text{g}}$: 11.1nC
- $Q_{\text{oss}}$: 13.3nC
- $Q_{\text{rr}}$: 0
Wrightsville HIPS
Defined for 48V-to-12V 1st Stage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{out}$</td>
<td>8x8.5x8mm, 4.7μH, 9mΩ</td>
</tr>
<tr>
<td>$F_{sw}$</td>
<td>500kHz</td>
</tr>
<tr>
<td>$I_{TDC}$</td>
<td>14A</td>
</tr>
<tr>
<td>Efficiency at $I_{TDC}$</td>
<td>96.5%</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>~100μF</td>
</tr>
<tr>
<td>$V_{out}$ slew rate</td>
<td>N/A</td>
</tr>
<tr>
<td>Density</td>
<td>2.1kW/in³</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>UFET</th>
<th>LFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BVds$</td>
<td>80V</td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>8mΩ</td>
<td>4mΩ</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>2.5nC</td>
<td>5nC</td>
</tr>
<tr>
<td>$R_{DS(on)} \cdot Q_g$</td>
<td>20mΩ•nC</td>
<td>20mΩ•nC</td>
</tr>
<tr>
<td>$Q_{oss}$</td>
<td>3nC</td>
<td>6nC</td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>2ns</td>
<td>4ns</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>2ns</td>
<td>4ns</td>
</tr>
<tr>
<td>$t_{dead}$</td>
<td>4ns</td>
<td>4ns</td>
</tr>
</tbody>
</table>

Projected Efficiency
$F_{sw} = 500kHz$

- Powerstage VR
- VR

FET Switching loss
FET Charge loss
FET Conduction loss

14A $I_{out}$

0.74W
0.13W
1.87W
Design Example 1: (8) 300kHz Nags Head

- Overall full load efficiency ~ 91%
- Overall density ~ 334W/in³ (17mA/mm³)
- Transient response: slower

Single Stage Efficiency
Vin=48V, Vout=1.2V, 300kHz

Single Stage
(8) Nags Head HIPS
Fsw = 300kHz
XAL7070 Inductor: 800nH
2.1mΩ
Power Density ~ 334W/in³
Design Example 2: (8) 800kHz Nags Head

- Overall full load efficiency ~ 86.5%
- Overall Density ~ 1.18kW/in³ (60mA/mm³)
- Transient Response: fast
  - 8-phase, 800kHz/phase
Design Example #3:
(1) 300kHz Wrightsville + (6) 2MHz Kitty Hawk

- Overall full load efficiency ~ 88.5%
- Overall Density ~ 440W/in³ (22.5mA/mm³)
- Transient response: very fast
  - 2nd Stage: 12-phase, 2MHz/phase

1st Stage
Wrightsville HIPS
Fsw = 300kHz
XAL1510 Inductor: 6.8μH
  4.2mΩ
Power Density ~ 800W/in³

2nd Stage
(6) Kitty Hawk HIPS
Fsw = 2MHz
XEL4030 Inductor: 200nH
  2mΩ
Current Density ~ 64mA/mm³
Design Example #4:
(1) 500kHz Wrightsville + (5) 3MHz Kitty Hawk

- Overall full load efficiency ~ 84.5%
- Overall Density ~ 1.18W/in³ (60mA/mm³)
- Transient response: extremely fast
  - 2nd Stage: 10-phase, 3MHz/phase

Two-Stage Efficiency
(1) Wrightsville (500kHz), (5) Kitty Hawk (3MHz)
48V in, 1.2V out

1st Stage
Wrightsville HIPS
Fsw = 500kHz
XAL8080 Inductor: 4.7μH
9mΩ
Power Density ~ 2kW/in³

2nd Stage
(5) Kitty Hawk HIPS
Fsw = 3MHz
XEL3515 Inductor: 72nH
2.8mΩ
Current Density ~ 190mA/mm³
### Design Examples: $48V_{in}$-to-$1.2V_{out}$, 120A

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<td>Per Stage</td>
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| 1              | Single Stage | (8) Nags Head | 0.3       | 17 mA/mm$^3$  
                            |            |           | 334 W/in$^3$         | Slower     | 91%          | 1.6           |
| 2              | Single Stage | (8) Nags Head | 0.8       | 60 mA/mm$^3$  
                            |            |           | 1.18kW/in$^3$        | Faster     | 86.5%        | 1.4           |
| 3              | 1$^{st}$ Stage | (1) Wrightsville | 0.3       | 800W/in$^3$  
                            | 2$^{nd}$ Stage | (6) Kitty Hawk | 2          | 64 mA/mm$^3$  
                            |            |           | 23 mA/mm$^3$         | Fast       | 88.5%        | 1.2           |
| 4              | 1$^{st}$ Stage | (1) Wrightsville | 0.5       | 2kW/in$^3$   
                            | 2$^{nd}$ Stage | (5) Kitty Hawk | 3          | 190 mA/mm$^3$  
                            |            |           | 60 mA/mm$^3$         | Fastest    | 84.5%        | 1.0           |

**Single vs. Two-Stage Buck study for 48V to 1.2Vout, 120A**

![Graph showing efficiency vs. load for different designs](image-url)
HIPS: Highest Efficiency, Density & Transient Response

48V_{in}, 1.2V_{out}, 120A_{out} VRs

Sarda HIPS
GaN FETs
MOSFETs

Transient Response:  
- >100mV/μs
- <100mV/μs

Meet efficiency targets of Open Rack Standard V2.0
HIPS: Highest Efficiency, Density & Transient Response

48\text{V}_{\text{in}}, 1.2\text{V}_{\text{out}}, 120\text{A}_{\text{out}} \text{ Single Stage VRs}

Sarda HIPS
GaN FETs

Transient Response:
- $>100\text{mV/\mu s}$
- $<100\text{mV/\mu s}$

Power Density (W/in$^3$)

Current Density (mA/mm$^2$)

VR Efficiency

Graph showing VR efficiency and power density with different markers for transient response.
Summarizing Single-Stage Buck Approaches

Power Density (W/in$^3$)

- 200
- 400
- 600
- 1,000
- 1,200
- 1,400

Current Density (mA/mm$^3$)

- 70
- 60
- 50
- 40
- 30
- 20
- 10
- 0

VR Efficiency

- 80%
- 85%
- 90%
- 95%

 transient Response:
- >100mV/μs
- <100mV/μs

Sarda HIPS
GaN FETs

HIPs enables dramatic shift “up and to the right”
Conclusion

- **Sarda’s HIPS Approach is a Game-Changing Technology**

- **12Vin HIPS**
  - Best Approach for Small, Fast, Efficient POL Voltage Regulators
  - Enable Granular Power Delivery

- **48Vin HIPS**
  - Will Enable Smallest, Most Efficient VRs for both Single-Stage and Two-Stage Approaches