Gate driver solution for GaN-based low-power motor control applications

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Presentation Outline

- Introduction
- Goals
- The challenge: how to control dv/dt?
- Linearizing Cgd
- Multi-phase current-source gate drive
- Hardware results
- Thermal Performance
- Conclusions
- Acknowledgements
VSI is dominant appliance motor drive topology today

- **VSI = Voltage Source Inverter**
- **Transistor requirements** for VSI:
  - Block voltage in forward direction
  - Conduct current in either direction (Can be diode in reverse direction)
  - Short-circuit handling capability
  - Slew-rate can be controlled/limited
- **LOW COST**
- Additional performance goals:
  - Low conduction loss (in both directions)
  - Low switching loss (dependent only on dv/dt limit – no additional Qrr loss)
Why is slew-rate control necessary for motor drives?

- Typical low-cost motor windings are inserted in overlapping layers
- This results in large voltage gradients between adjacent coils
- Fast $dv/dt$ waveforms can cause insulation breakdown
  - Due to corona and partial-discharge
- Motor bearings can also be damaged due to $dv/dt$ induced capacitive currents
- **Typical limit is 5 V/ns**
- More expensive motors with concentrated windings may tolerate somewhat faster $dv/dt$
So – why use GaN for motor drives?

- GaN is often considered a very **fast**, high-performance (but **expensive**) switch
- Why does it make sense to **slow its switching speed** and use it at **low-frequency** in a low-cost motor drive VSI?
  - Package power dissipation limits output power in today’s IPMs
  - **In the same package, GaN can deliver >2X output power** because lower conduction and switching loss than Silicon
  - The value proposition is **2X power density for <2X cost**
When driven with the proposed gate drive method, CoolGaN™ has good SCSOA

- Has a predictable, repeatable current-collapse that reduces $I_D$ similar to IGBT desaturation

Test Conditions:
- 70 mΩ GaN transistor
- 350 V Bus
- 125° C starting temperature
- 8 µs input pulse-width
- Gate drive = 110/10 mA

Infineon is assessing reliability impact of repetitive short-circuit events in a new arpa-e funded program.
Goals of this work

- Develop **low-cost** Silicon 3-phase gate-driver IC for CoolGaN™ that can:
  - Accurately control voltage slew-rate \((dv/dt)\)
  - (on both turn-on and turn-off edges)
  - Eliminate the need for external passive components except for bootstrap cap
    - (because packaging passives in the IPM is expensive)
- Package driver IC with 6 GaN transistors in 12x12 mm PQFN package
- Successfully demonstrate controlled slew-rate motor drive
- **Improve power density** of existing 12x12 mm MOSFET IPM by a factor of 2
The challenge: how to control $dv/dt$

- For Si IGBT or FET, adjusting gate drive current is common
  - Simplest way is to **adjust $R_g$**

During the “plateau” region, all of the gate input current is discharging gate-collector capacitance

So $dv/dt = Ig/C_{gc}$
But – GaN has very nonlinear Cgd

- Thus – the $\frac{dv}{dt}$ is also very **nonlinear for a fixed gate-drive resistor** (current)

Maximum $\frac{dv}{dt}$ is controlled, but leading and especially trailing edge are very slow, leading to significant additional switching loss.

**Figure 20** Typ. capacitances

$V_{ds} = 50 \text{ V/div}$

$\frac{dv}{dt} = -4.85 \text{ V/ns}$
The solution: add small linearizing capacitor to $C_{gsd}$

- Now – a simple fixed-time 2-phase gate drive will provide linear $dv/dt$ control
- Gate charge is doubled, but at 16 kHz PWM, it is still so low it is insignificant
Block diagram of gate driver IC (one channel)

dv/dt-Controlled Gate Driver for CoolGaN

Input  Level-Shift Isolation  Logic Sequencing Timing

Steady-State ON Current

Turn-ON dv/dt

Turn-OFF dv/dt

OFF-state “Miller” Clamp

Linearizing capacitor

GaN HEMT

Note no negative gate drive is necessary with slower dv/dt and driver IC in same package as GaN
Gate drive circuit provides precise, linear $dv/dt$ control

Low-side hard-switching 620 $\mu$H phase inductance

$V_{GS}$ high-side 1 V/div

$I_L$ 1.5 to 2.0 A

$I_L$ 1.0 to 1.5 A

$I_L$ 0.5 to 1.0 A

$I_L$ 0 to 0.5 A

$V_{GS}$ low-side 1 V/div

Phase output 50 V/div

200 ns/div

Turn-on slew-rate precisely limited to -5.0 V/ns at any current

At 0.5 A, slew-rate is limited by inductor current to +3.03 V/ns

≥1 A, slew-rate is limited by gate drive to +5.0 V/ns
Excellent dynamic transition from slow $dv/dt$ to controlled commutation

PVM E-400 motor, 325 V bus, 720 RPM, 88 W

Phase output 50 V/div

$V_{GS}$ high-side 1 V/div

Then hard-switched 5 V/ns slew-rate at end of deadtime

Phase current

Natural slew-rate 0.17 V/ns so transition not completed by end of deadtime

$V_{GS}$ low-side 1 V/div

200 ns/div
3-phase motor drive test board temperature rise using thermal imaging

Local Max. surface temperature for each device

<table>
<thead>
<tr>
<th>Device</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>97°C</td>
</tr>
<tr>
<td>Q3</td>
<td>105°C</td>
</tr>
<tr>
<td>Q5</td>
<td>100°C</td>
</tr>
<tr>
<td>Q2</td>
<td>90°C</td>
</tr>
<tr>
<td>Q4</td>
<td>91°C</td>
</tr>
<tr>
<td>Q6</td>
<td>92°C</td>
</tr>
<tr>
<td>IC</td>
<td>84.4</td>
</tr>
</tbody>
</table>

Test Condition: Vbus=320V, Ta=25°C, Fsw=16 KHz, 2-phase modulation
1.07 A rms phase-current, 233 W output
Comparing performance results between existing Si vs GaN solution

- All 3 IPMs compared are 12x12mm PQFN package
- All 3 gate driver ICs are made with the same HVJI Silicon process
- The test is: **How much power can each technology deliver with 80° C max temp-rise?**

<table>
<thead>
<tr>
<th>Device</th>
<th>Transistor technology</th>
<th>Rds(on) (typ)</th>
<th>Phase current</th>
<th>Motor power</th>
<th>Increase in delivered power</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRSM836 (existing product)</td>
<td>Trench FREDFET</td>
<td>1.5 Ω</td>
<td>0.23 A rms</td>
<td>50 W</td>
<td>(baseline 0%)</td>
</tr>
<tr>
<td>IMMxx-046M (in development)</td>
<td>CoolMOS™</td>
<td>1.4 Ω</td>
<td>0.54 A rms</td>
<td>117 W</td>
<td>134%</td>
</tr>
<tr>
<td>GaN with new IC driver prototype</td>
<td>Gen 1 CoolGaN™</td>
<td>0.8 Ω</td>
<td>1.04 A rms</td>
<td>226 W</td>
<td><strong>352%</strong></td>
</tr>
</tbody>
</table>

**GaN with controlled dv/dt driver provides clear power density benefit**

- Allowing faster dv/dt will directly reduce switching loss, enabling even higher power
Conclusions

- GaN can be effective solution in low-frequency, slow-$dv/dt$ VSI motor drive
- Switching loss is lower than any competing technology
- Conduction loss can be very low and fit inside IPM due to low specific $R_{ds(on)}$
- Performance is enabled by low-cost Si gate driver IC in Integrated Power Module
- Smooth waveforms for low EMI signature
- Performance exceeds expectations, >2X power density improvement
- Ongoing work assessing reliability of GaN and SCSOA for motor drive applications
Acknowledgements

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- www.psma.com