The Case for GaN Integrated-Circuits

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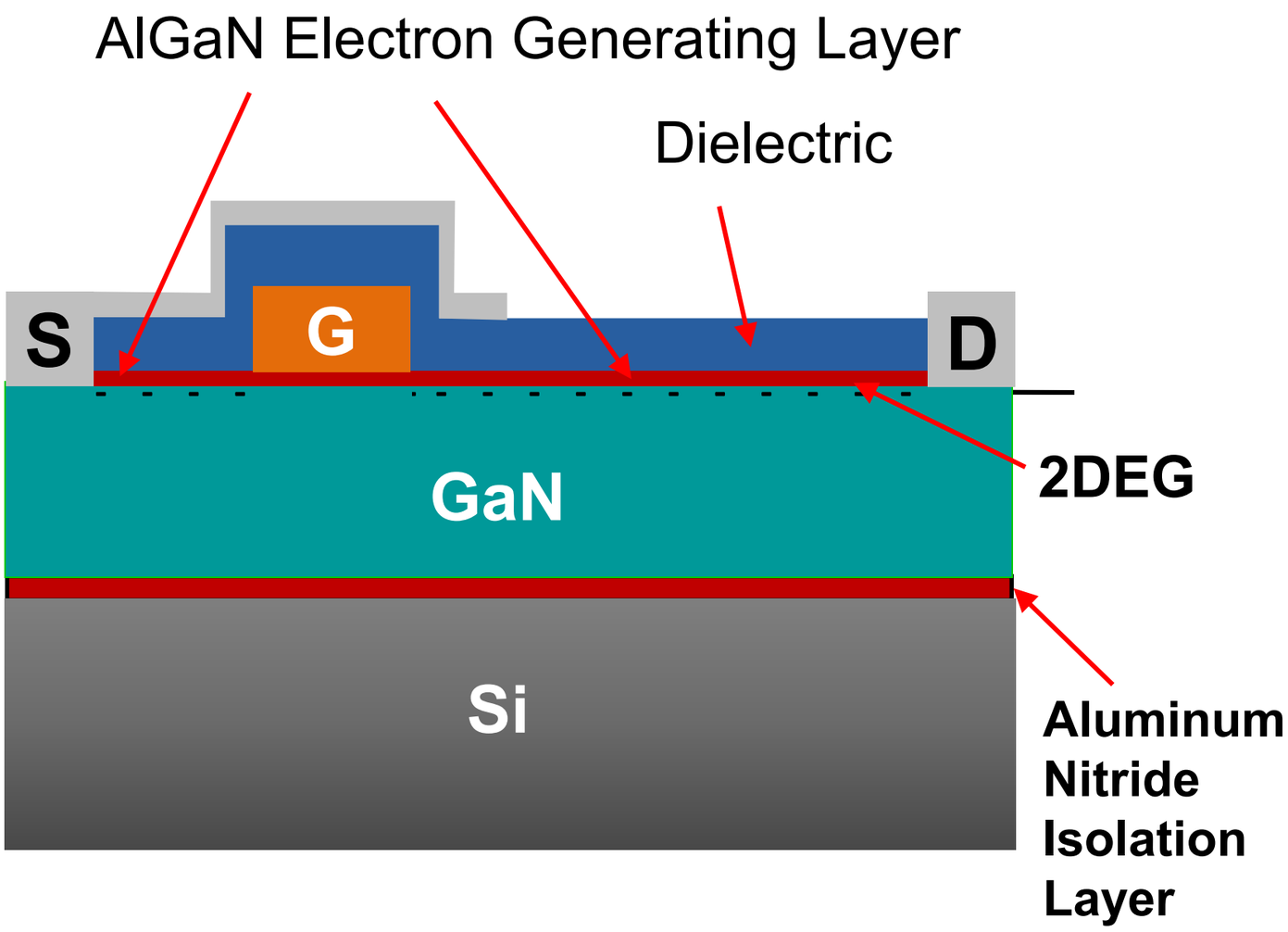
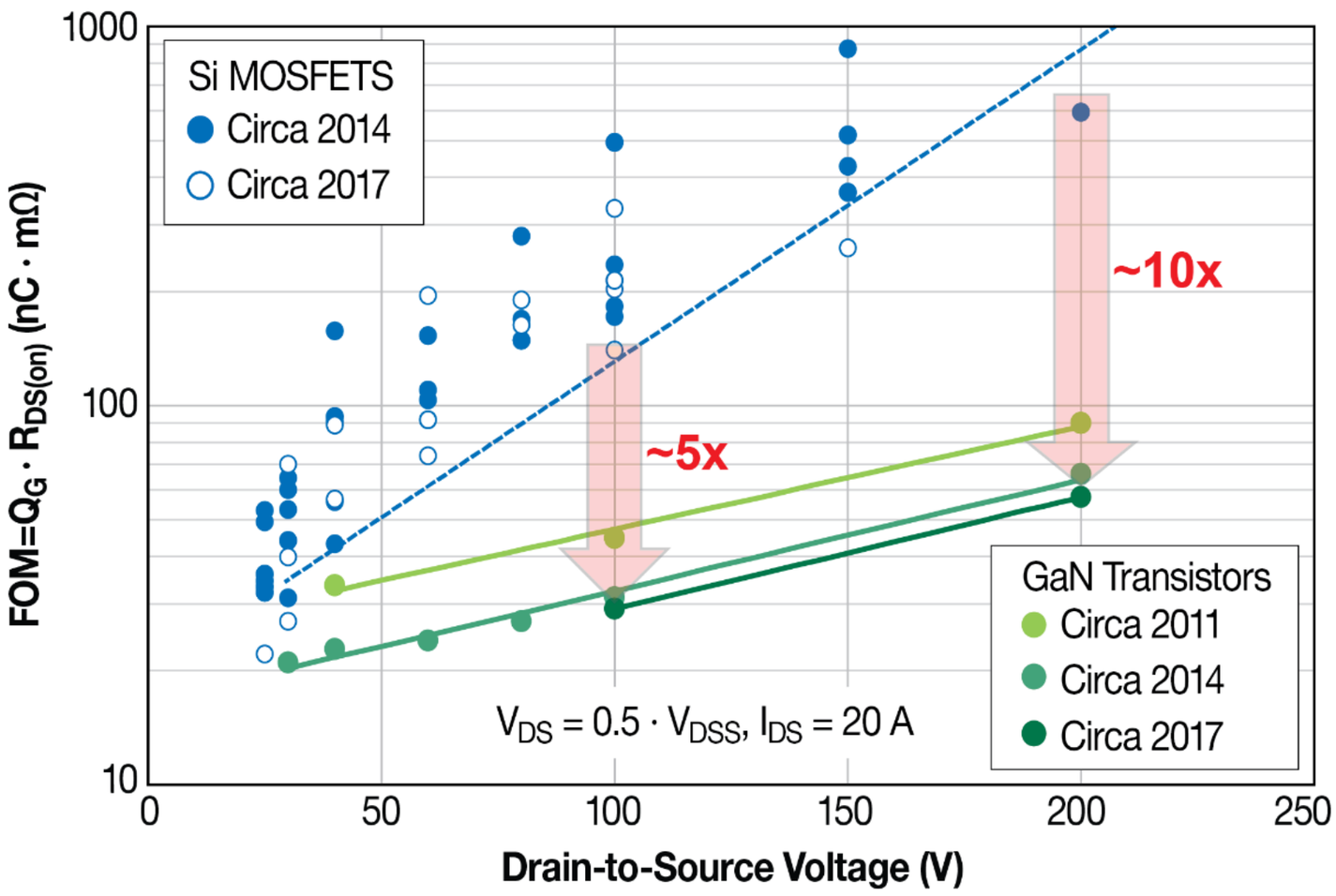
GaN Devices: An Introduction



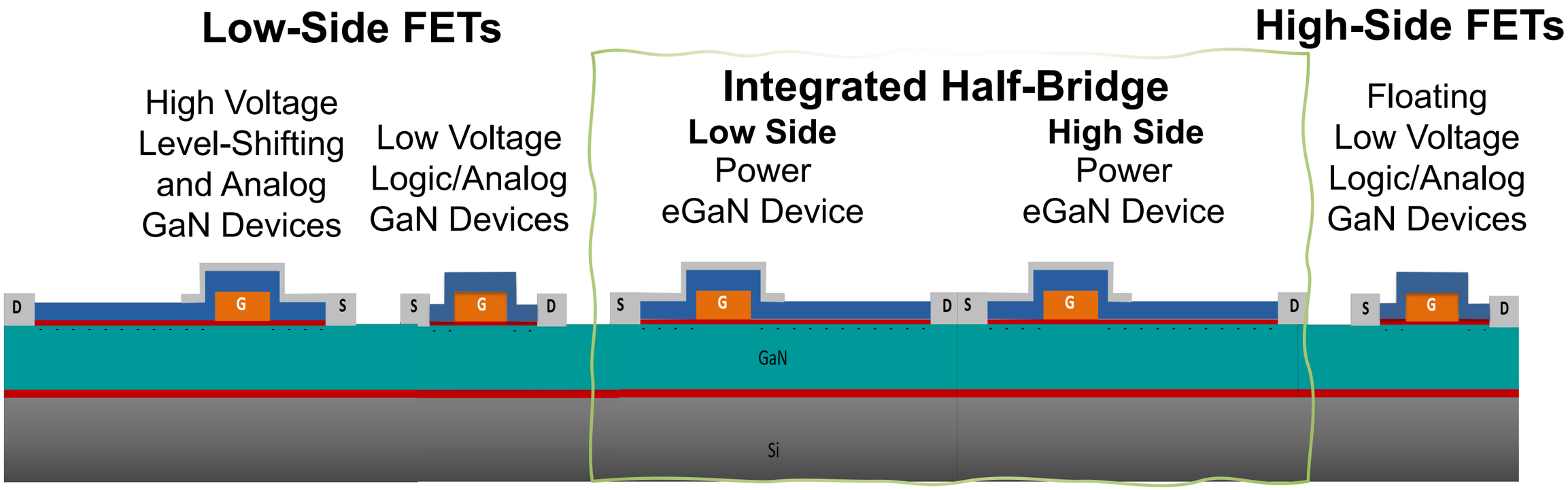
- Enhancement-mode (eGaN®) FETs have lateral structures
- Two-dimensional Electron Gas (2DEG) forms bi-directional conduction channel
- Majority carrier flow-direction determined by V_{GS} or V_{GD}
- eGaN FET has no reverse-recovery charge trapping like MOSFET

The Merits of GaN Devices

- GaN devices have much smaller $R_{DS(on)} \times C_{IN}$ *and* $R_{DS(on)} \times C_{OSS}$ than MOSFETs
- No minority carriers, i.e. zero reverse recovery
- For a given $R_{DS(on)}$, same driver can switch 'ON' or 'OFF' a GaN FET much faster than a MOSFET
- Lower C_{IN} and C_{OSS} means lower switching losses and hence ability to switch at higher frequencies in contrast to MOSFETs



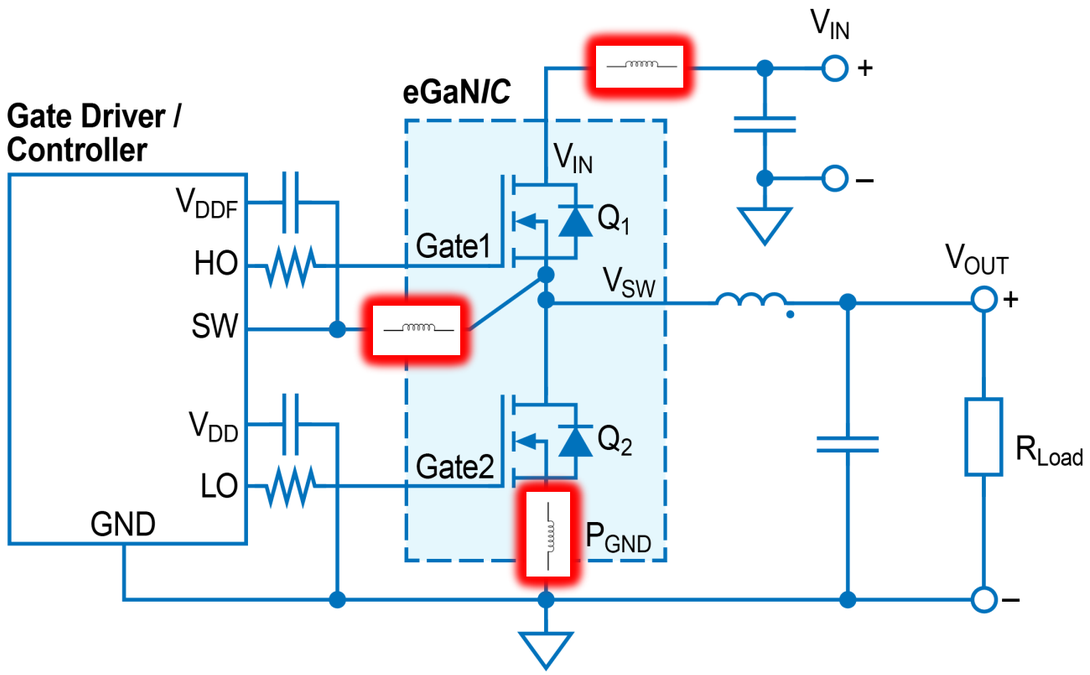
Lateral Build of GaN Devices to Form Circuits



- Multiple FETs, resistors, and capacitors can be built on a process that allows for high-side and low-side circuits

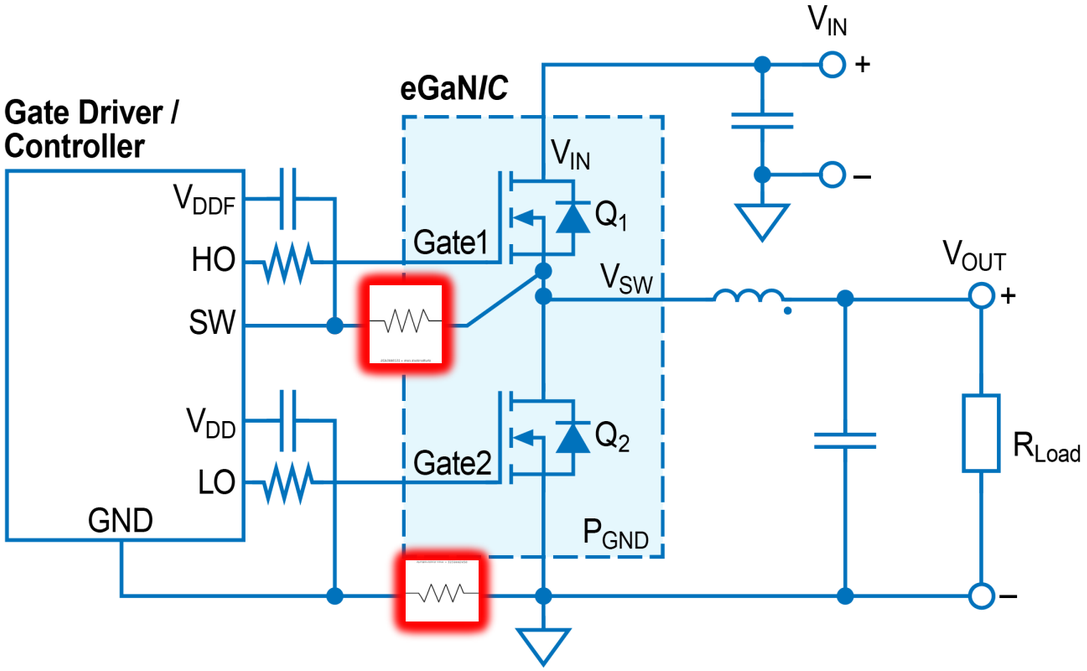
Challenges in Discrete Implementation of the Half-Bridge Power Stage

- Discrete board implementation creates un-wanted resistive and inductive connections between critical nodes such as ‘SW’, GND, and Gate
- Gate-loop and common-source inductance (CSI), caused by the trace inductance between the FET’s source and gate driver, can reduce the V_{GS} applied to the FET due to the source voltage created by the large di/dt



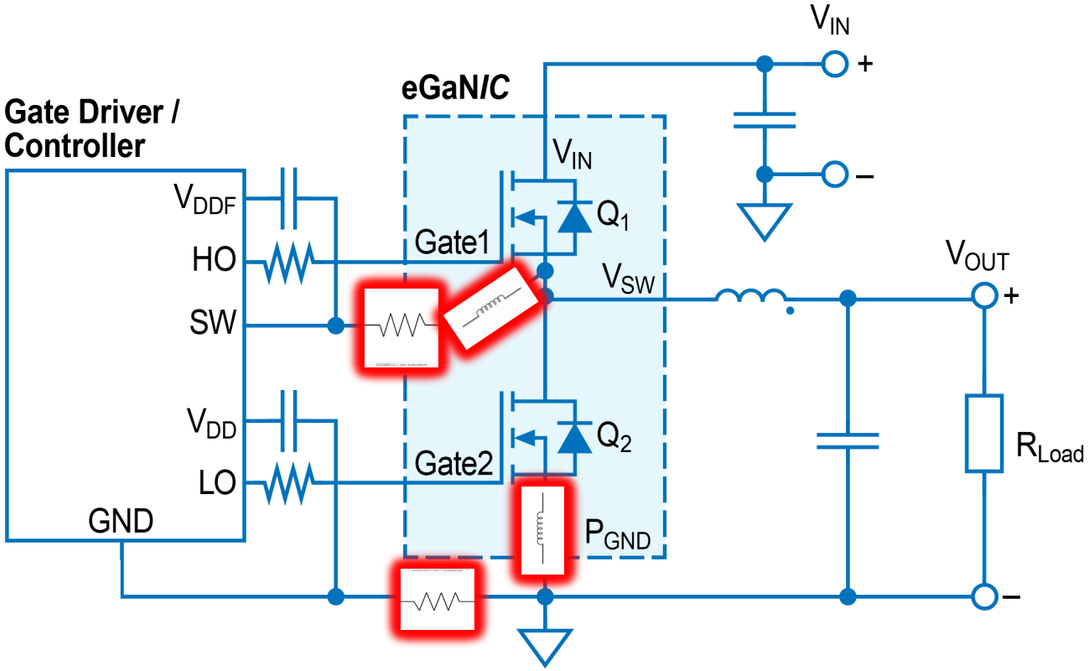
Challenges in Discrete Implementation of the Half-Bridge Power Stage

- Trace resistance between Q1 and Q2's source with respect to their drivers can cause issues with the driver and play havoc on the level-shifted Gate drive for Q1



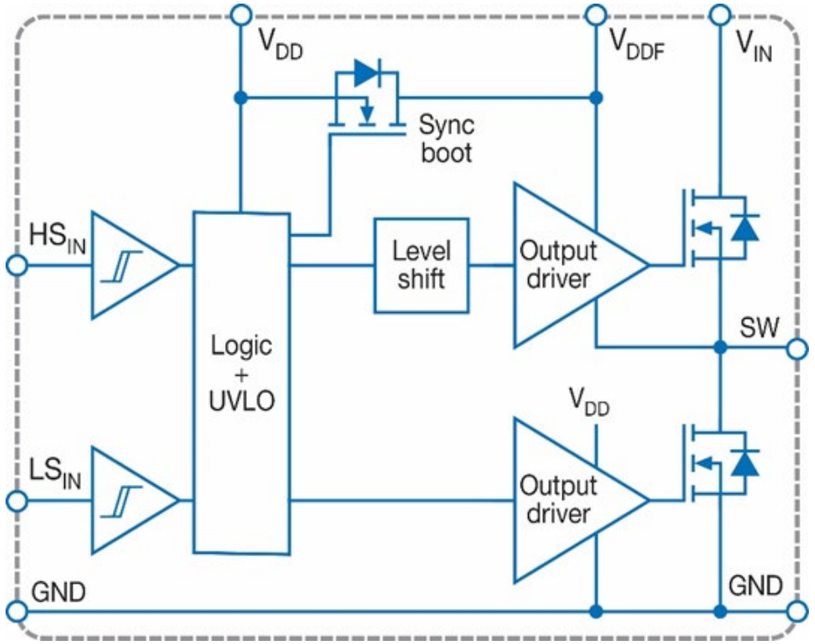
Challenges in Discrete Implementation of the Half-Bridge Power Stage

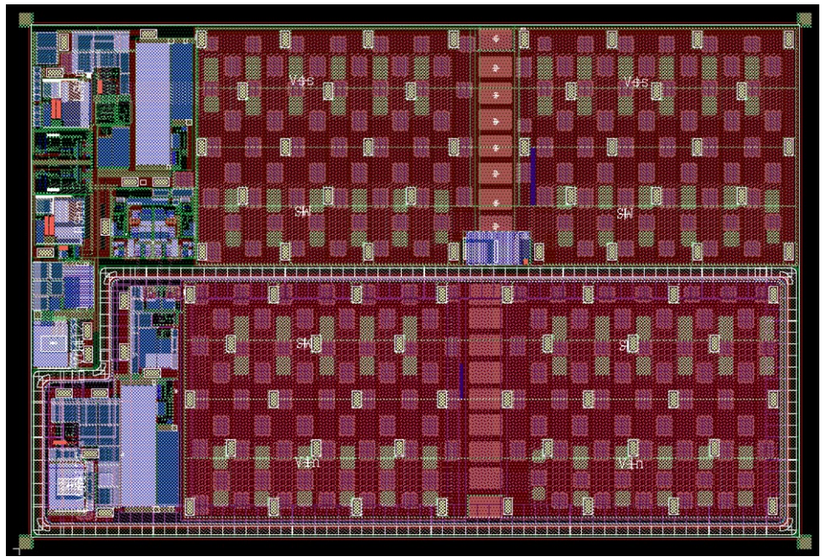
- Propagation delays between low-side Q2 FET gate drive and high-side Q1 gate drive are harder to match
- Variation in propagation delays requires larger dead-times between when Q1 and Q2 FETs are turned ON to avoid shoot-through
- Larger dead-time creates larger “diode” commutation losses



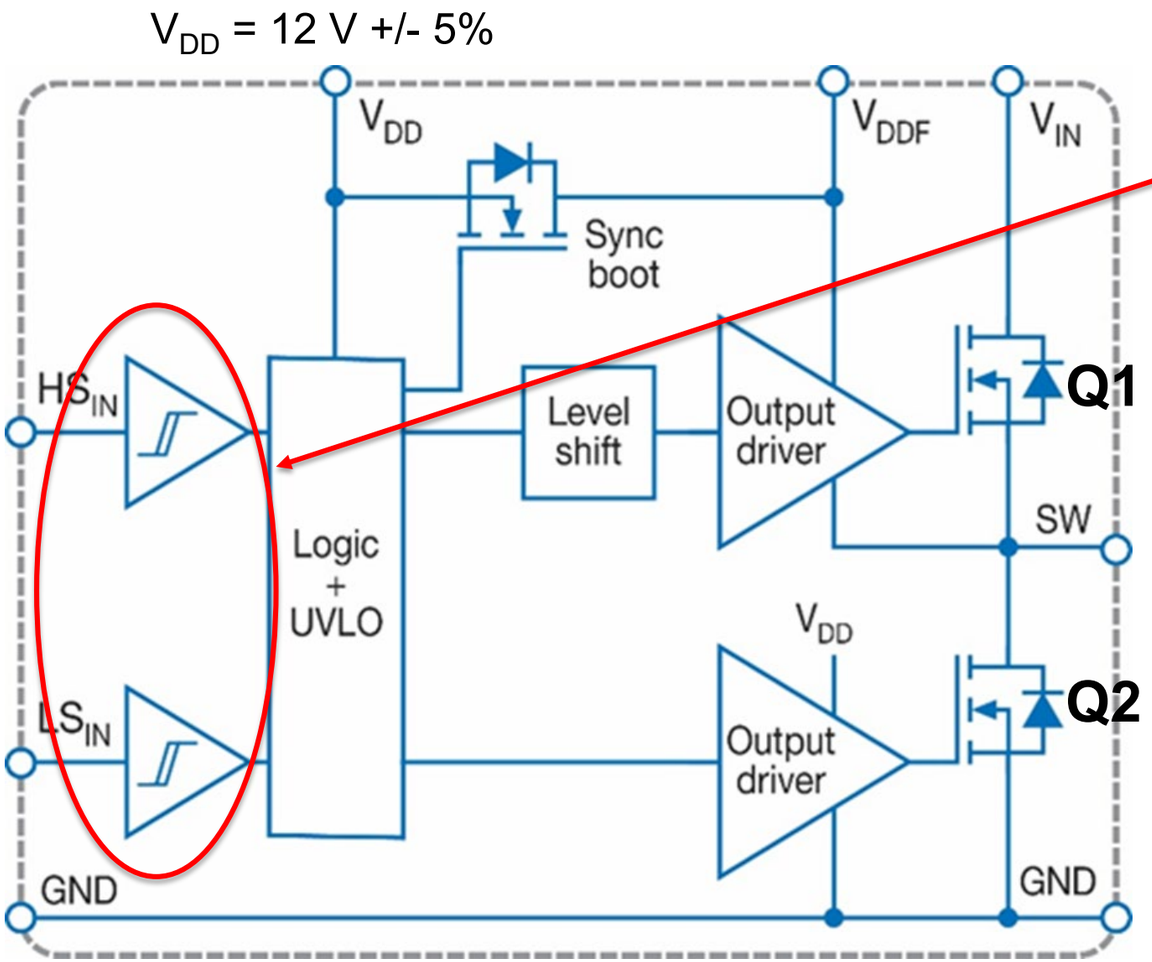
Motivation for a Fully GaN Monolithic Power Stage

- Dramatically reduce gate-loop & CSI due to on-chip integration of driver and power FETs
- Minimize resistance and inductance between associated circuit blocks by being on the same substrate or well
- Equalized heat distribution among devices
- Customized driver strength based on size of power FET to minimize over or under shoot
- Minimized PCB layout with optimized IC pad layout and fewer components



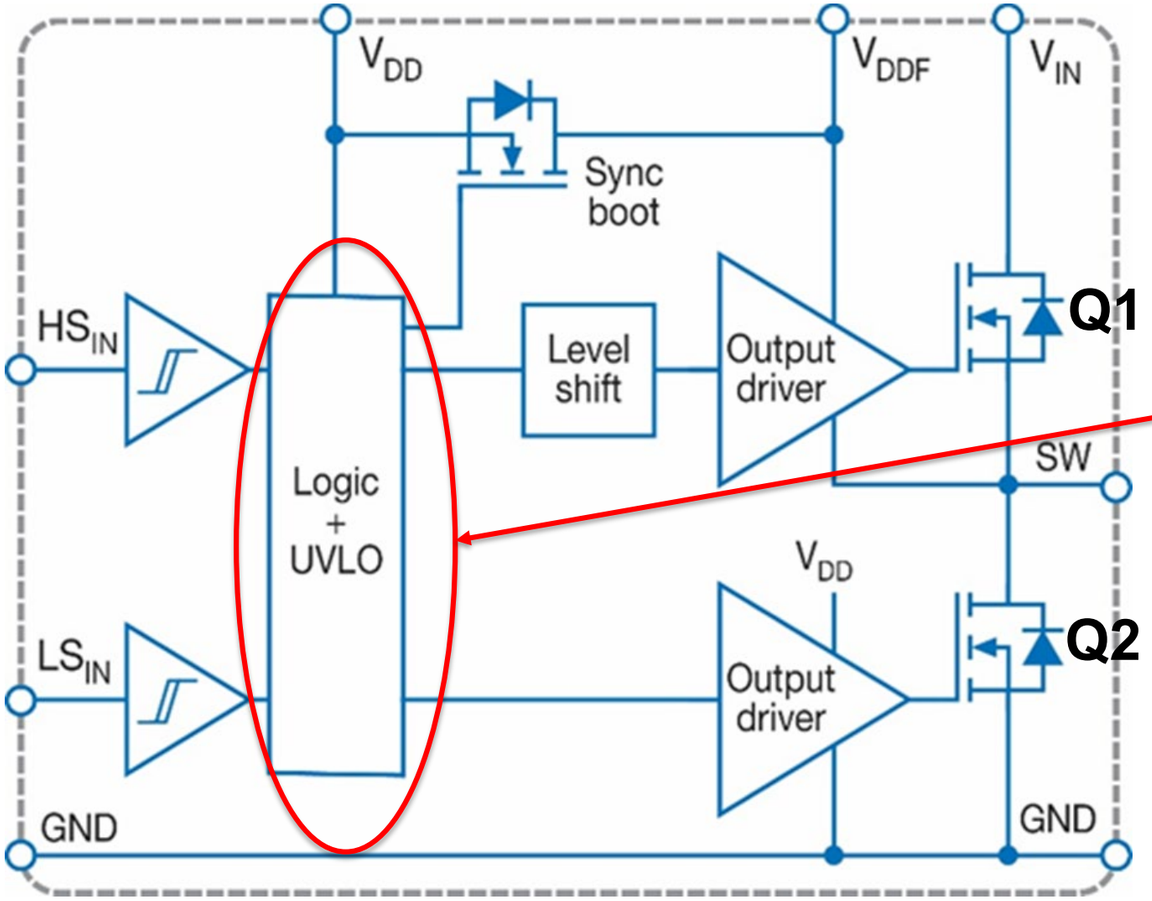


Monolithic Power Stage: Input Control



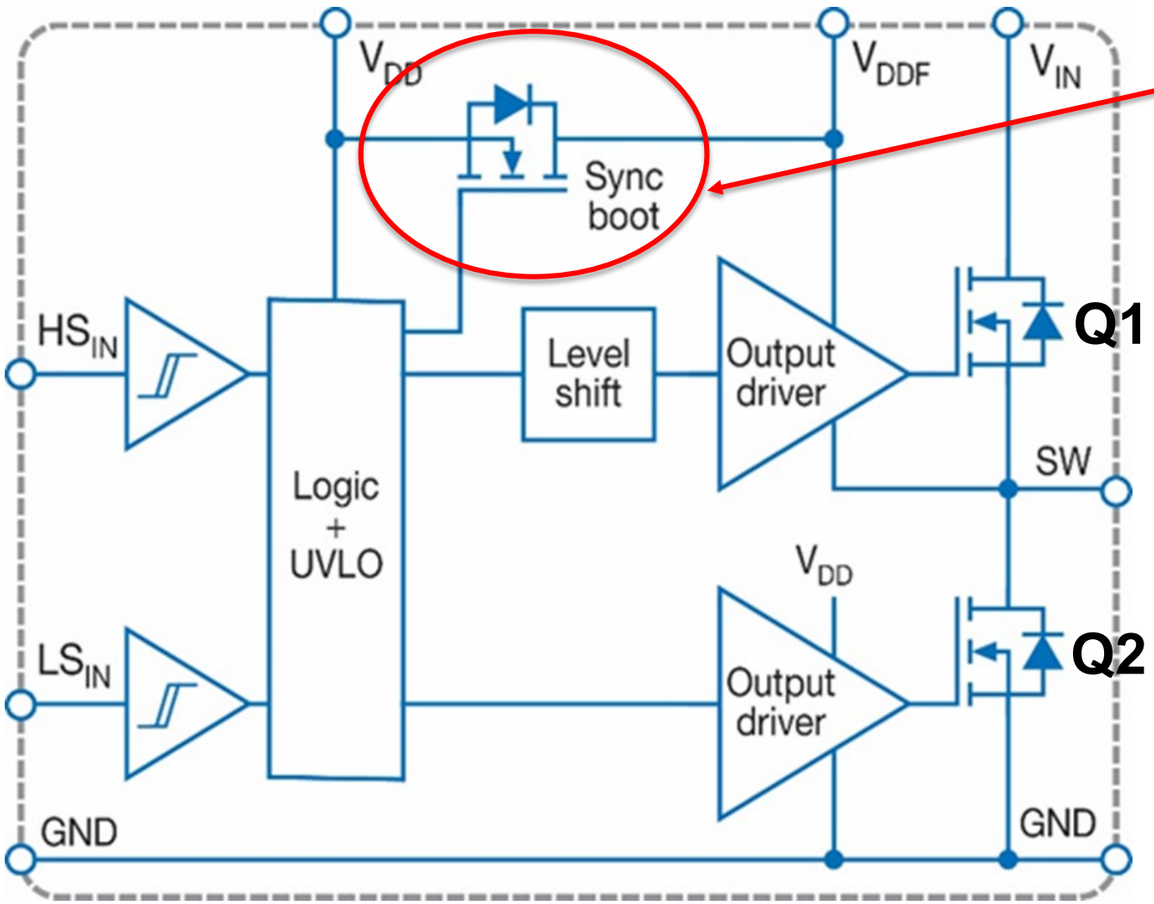
- Input level-translators interface with 2.2 V or higher voltage level logic controls as well as analog PWM controller output signals up to 12 V
- Differential input structure with hysteresis to maximize immunity to common-mode switching noise
- Process and temperature independent by design
- Fast response down to input pulse-width less than 20 ns

Monolithic Power Stage: UVLO and Logic



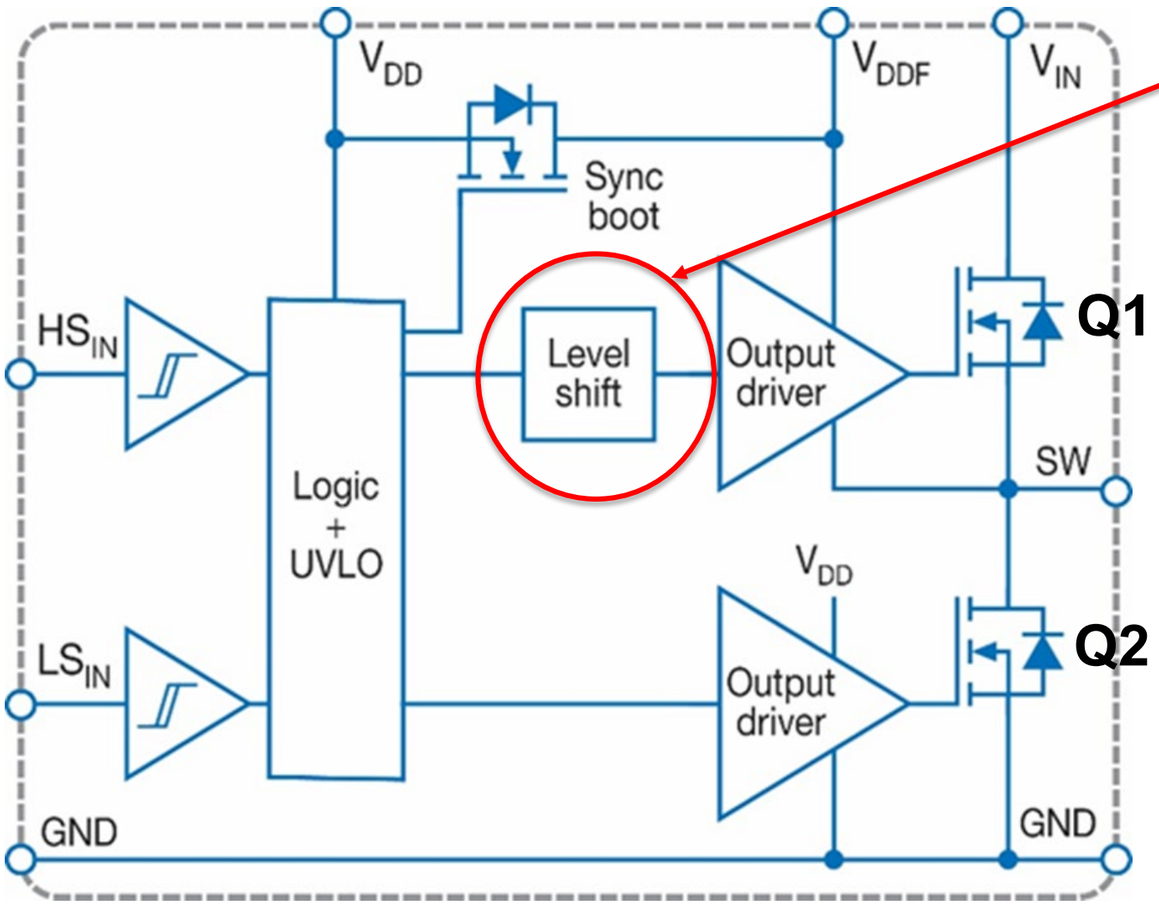
- Under-Voltage Lockout ensures both V_{DD} and floating V_{DDF} are above minimum supply level required to avoid low gate drive level to FETs
- Logic signals for high and low-side go through delay-matching blocks to ensure that final Q1 and Q2 gate drive signals have similar propagation delays
- Above matching of delays allows for smaller dead-time settings between Q1 and Q2 switching

Monolithic Power Stage: Synchronous Boot-Strap



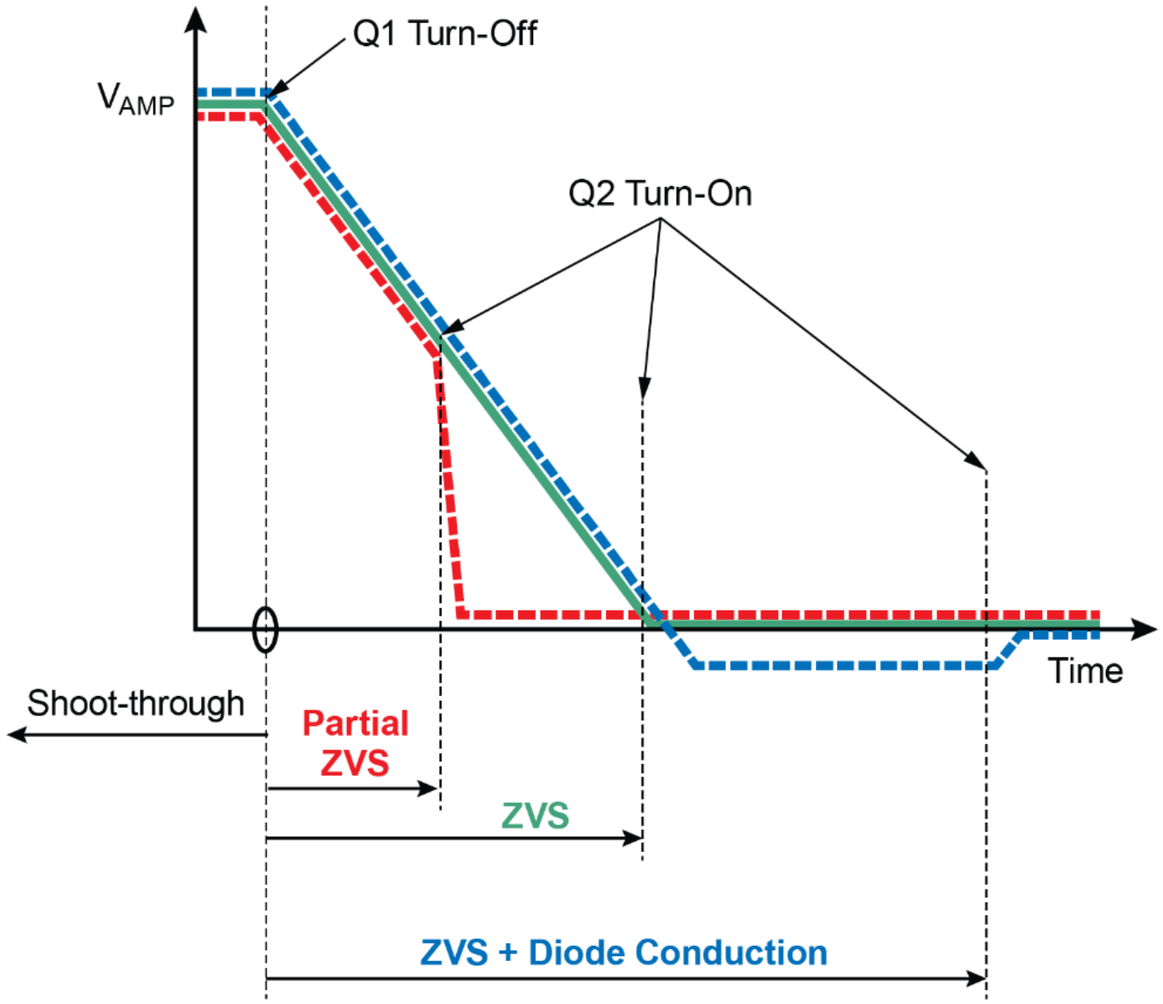
- Integrated synchronous-bootstrap circuit ensures V_{DDF} is close to V_{DD} level without losing a diode voltage drop
- Internal logic guarantees V_{DDF} not being charged during dead-time to prevent over-charging during negative SW transients
- No reverse-recovery losses incurred during the boot-strap transition
- Robust operation in all transient conditions

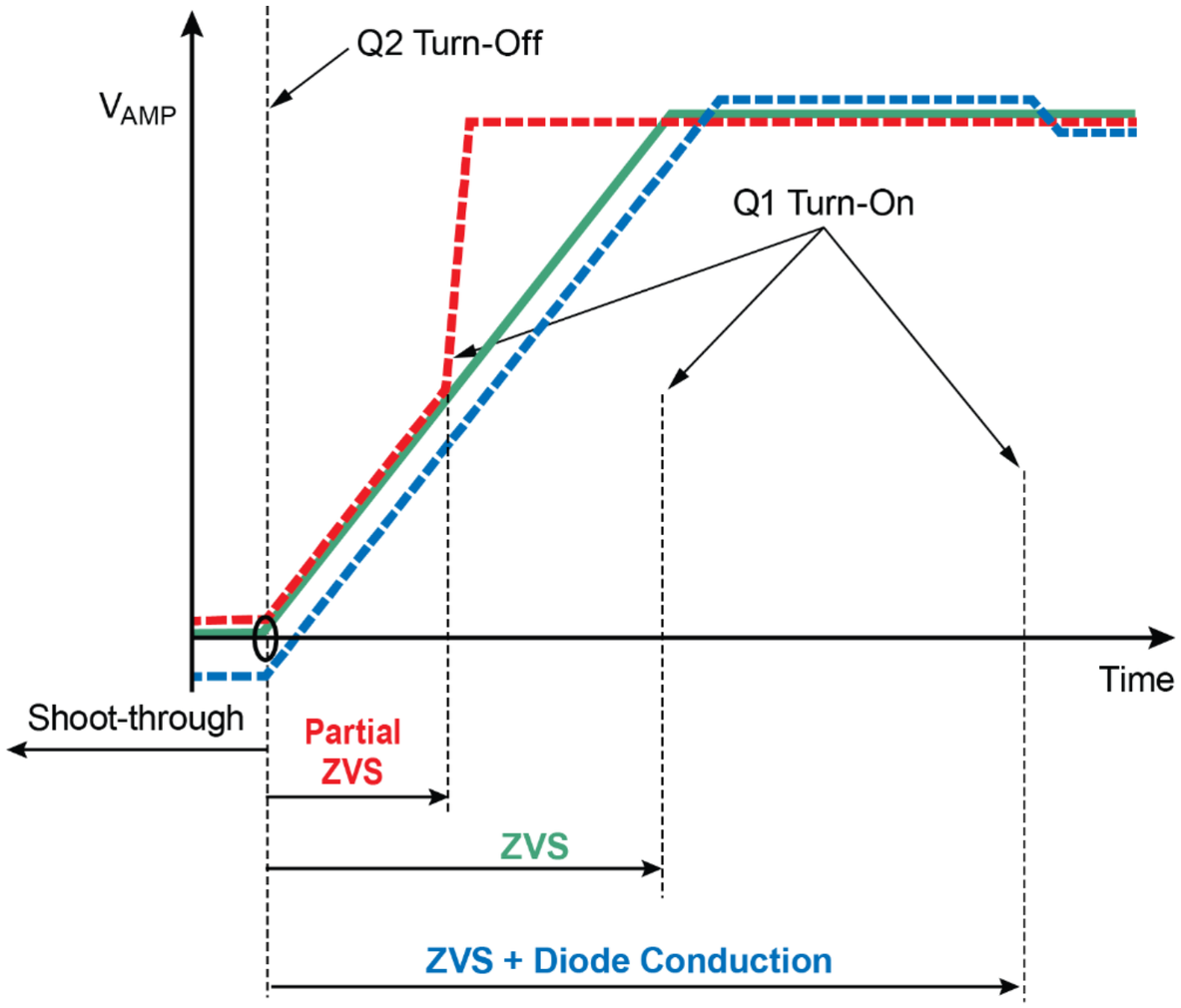
Monolithic Power Stage: Level Shifter



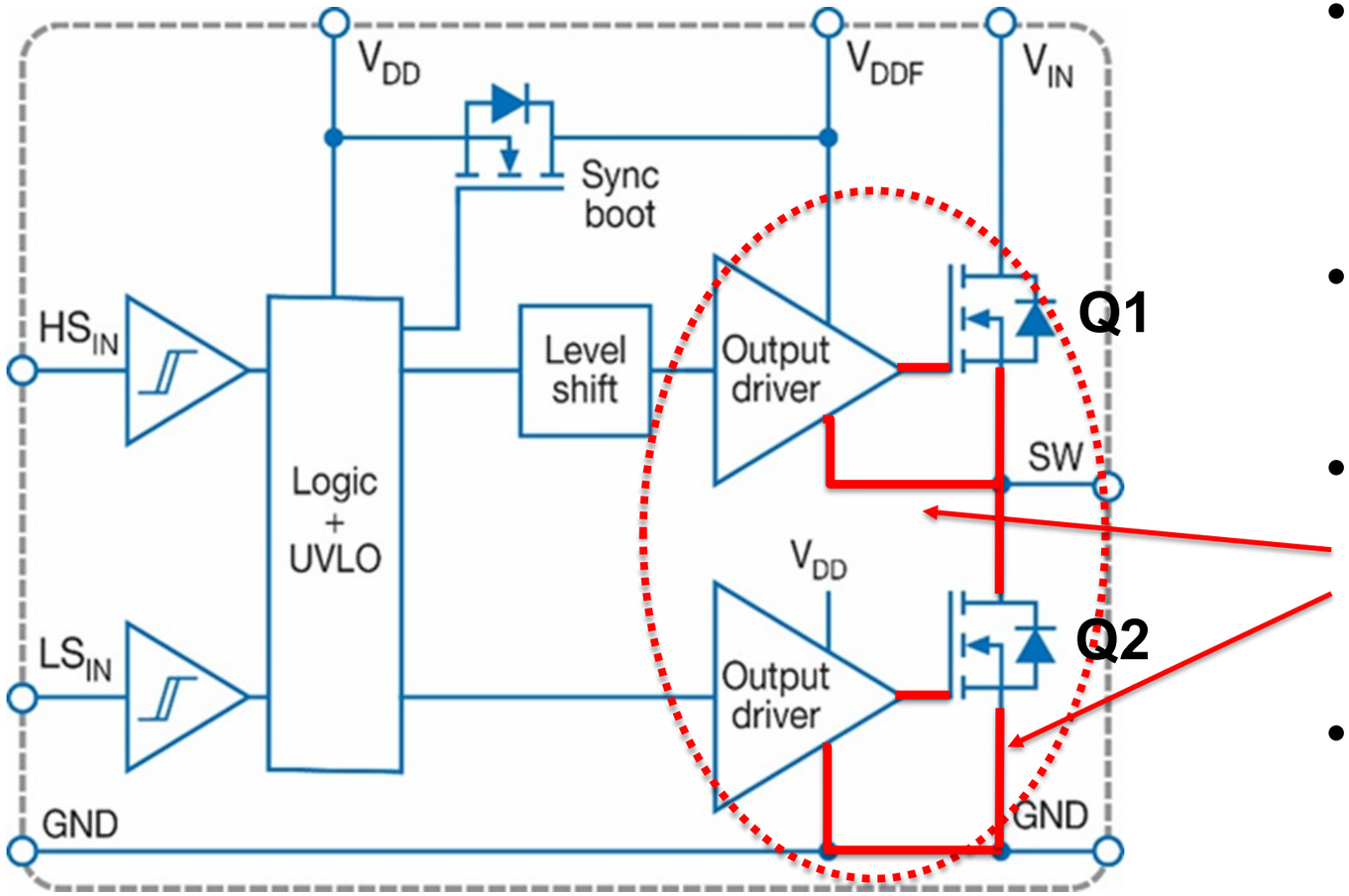
- Integrated Level Shifter shifts ground referenced HS_{IN} control to logic level referenced to SW
- Operates with negative SW transient to -5 V and immune to dv/dt transients of up to 100 V/ns on SW
- Robust operation under all known transient conditions of SW, from partial ZVS to rapid turn ON/OFF of Q1 and Q2 FETs in both first and third quadrants of operation

Level-Shifter Operation in Various Modes





Monolithic Power Stage: Output Drivers

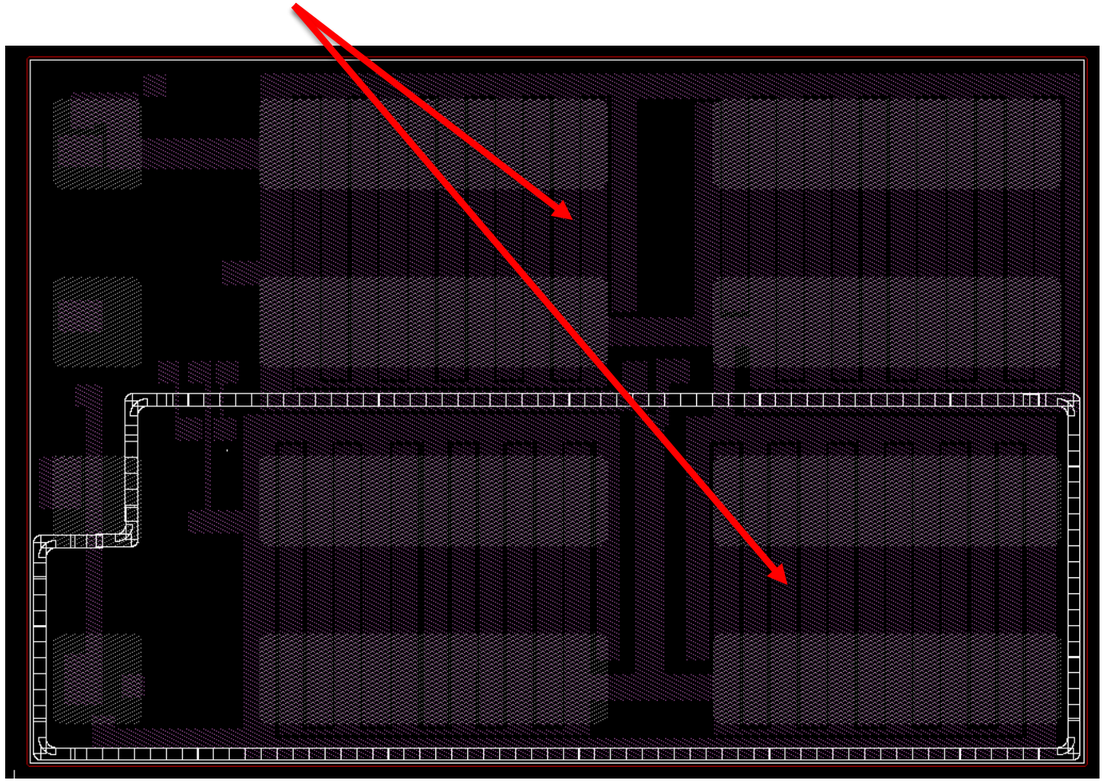


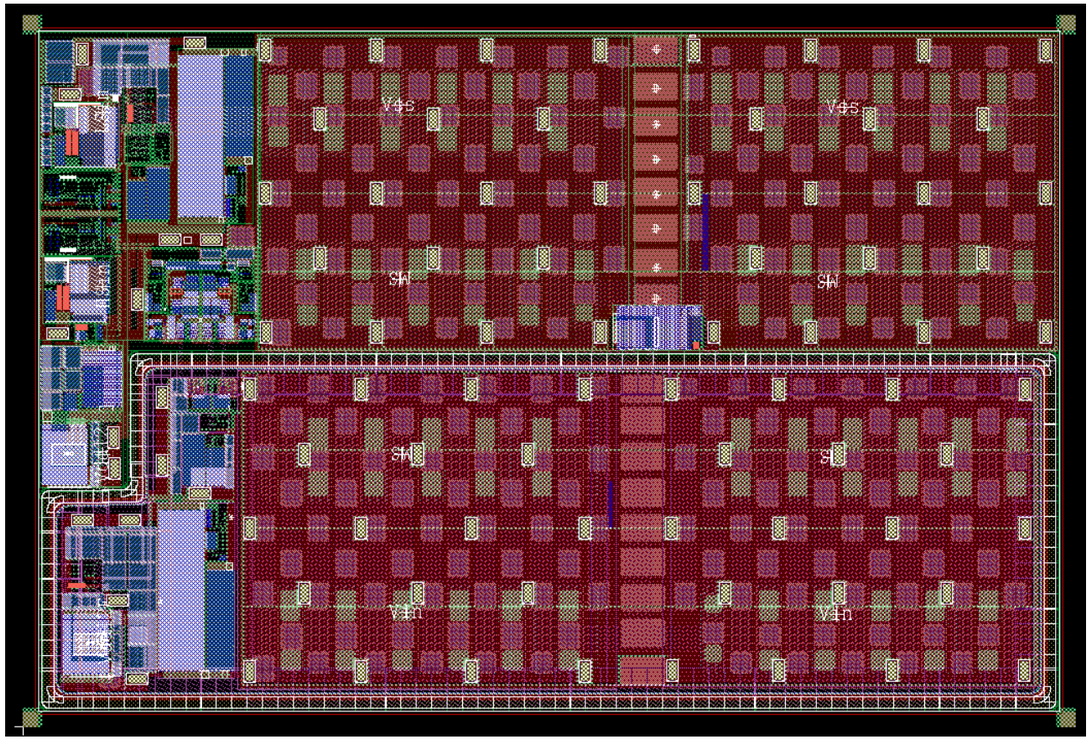
- Gate driver output proportional to V_t of process (tracks process and temperature)
- Integrated half-bridge with isolated wells
- Q1 and Q2's proximity to high-side and low-side gate drivers minimize parasitics
- Tight layout and use of copper routing minimizes CSI and routing resistance

Monolithic Power Stage Layout

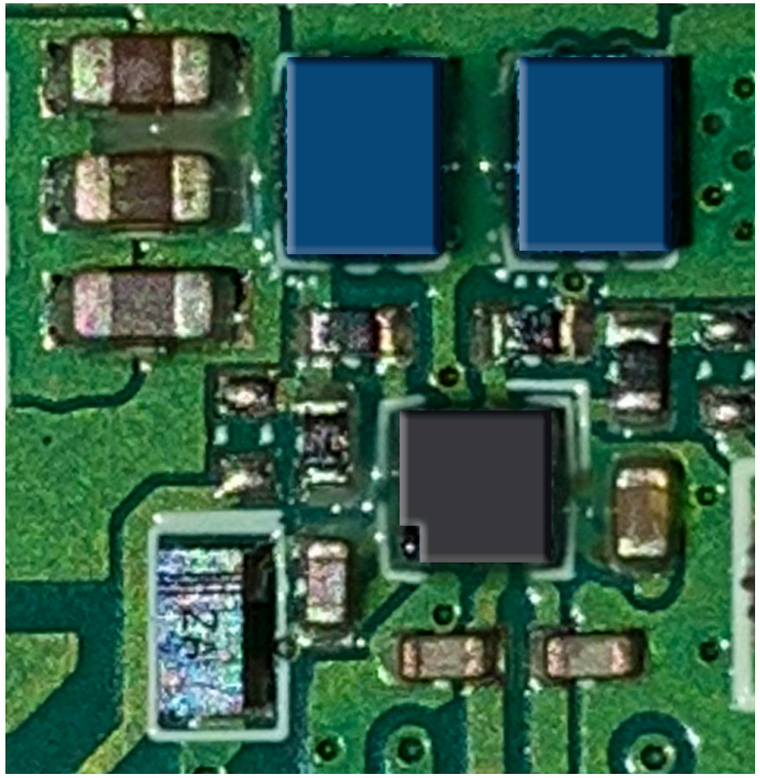
- Layout incorporates isolated high and low-side circuits and copper routing for all power nets
- CSI and routing resistance is negligible compared to discrete implementation on PCB
- Monolithic power stage with Driver + HB-FETs measures only 3.9 mm x 2.7 mm (~10.2 mm^2)

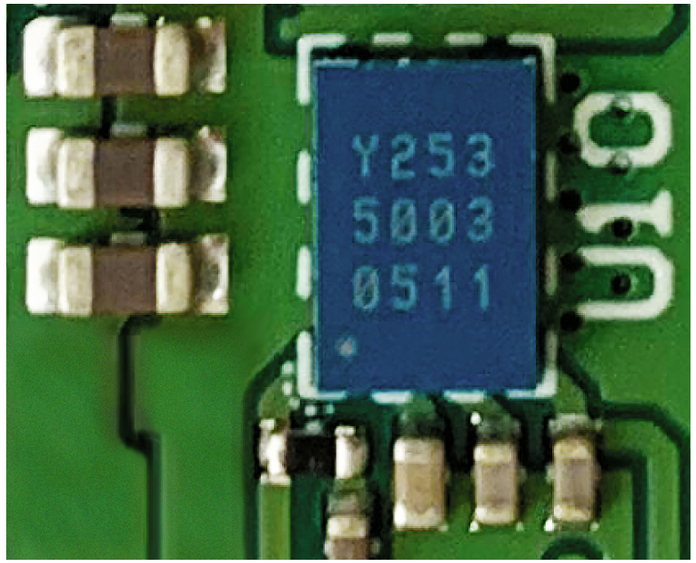
Copper Routing





Discrete vs. Monolithic Power Stage on PCB

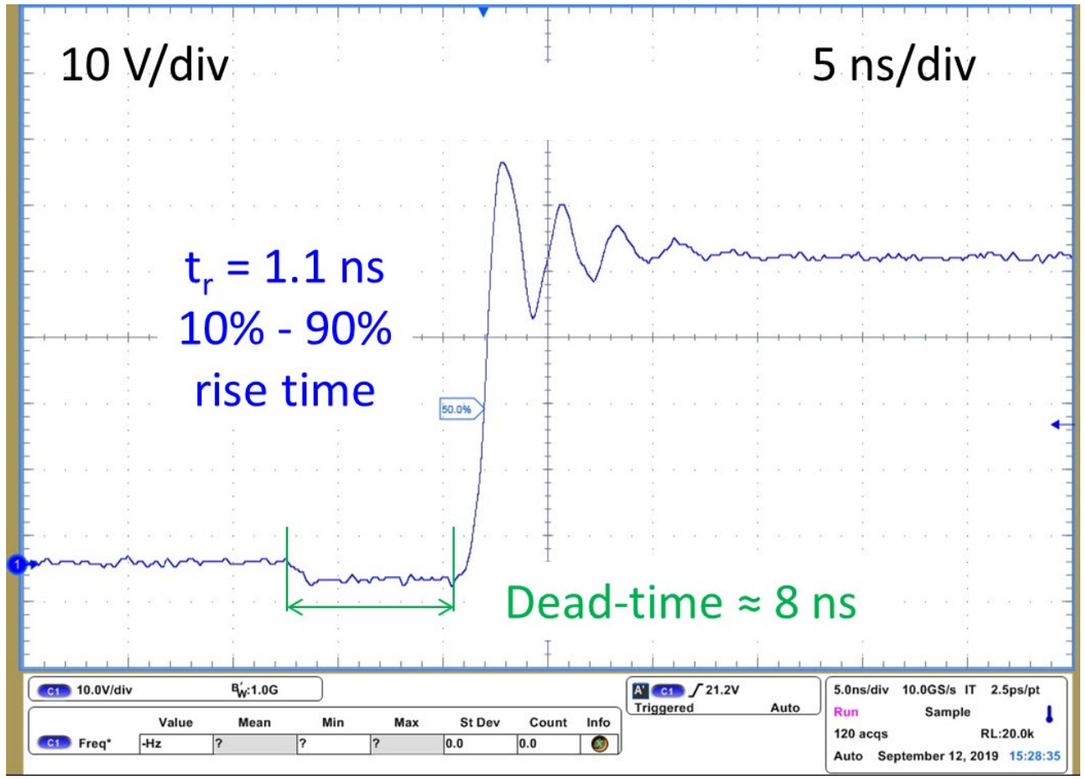


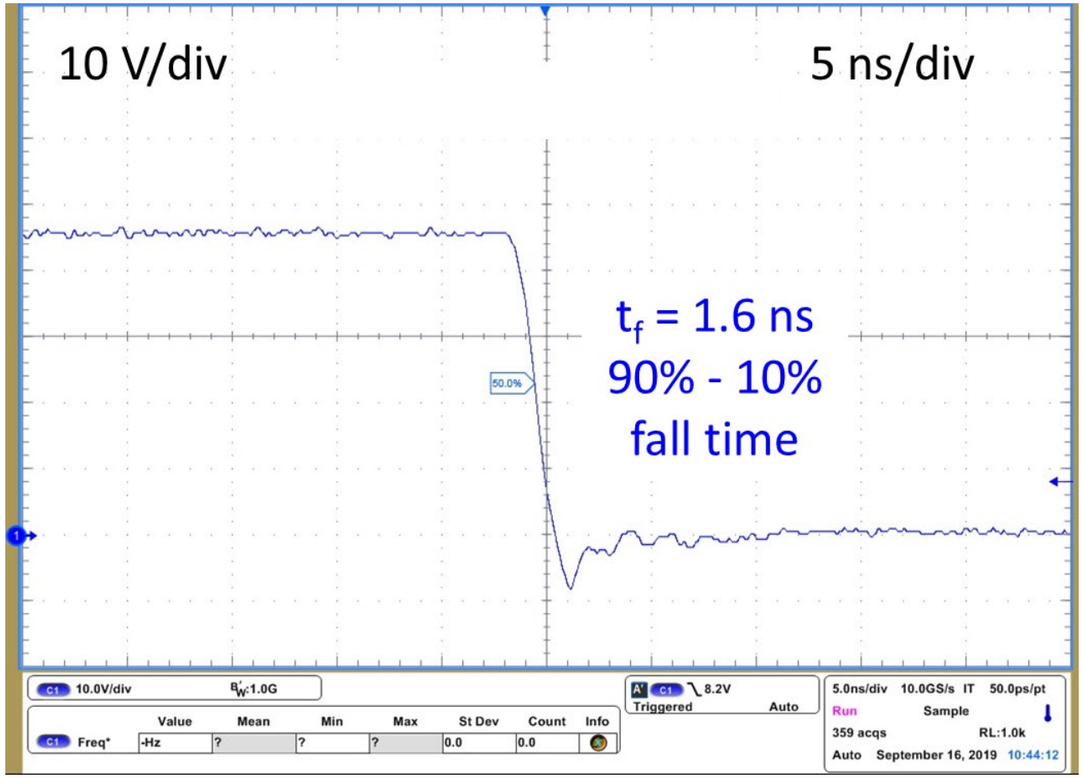


- ~ 35% smaller in size on PCB
- Reduced component count
- Easy to implement and use: Digital In/Power Out

‘SW’ Node Switching

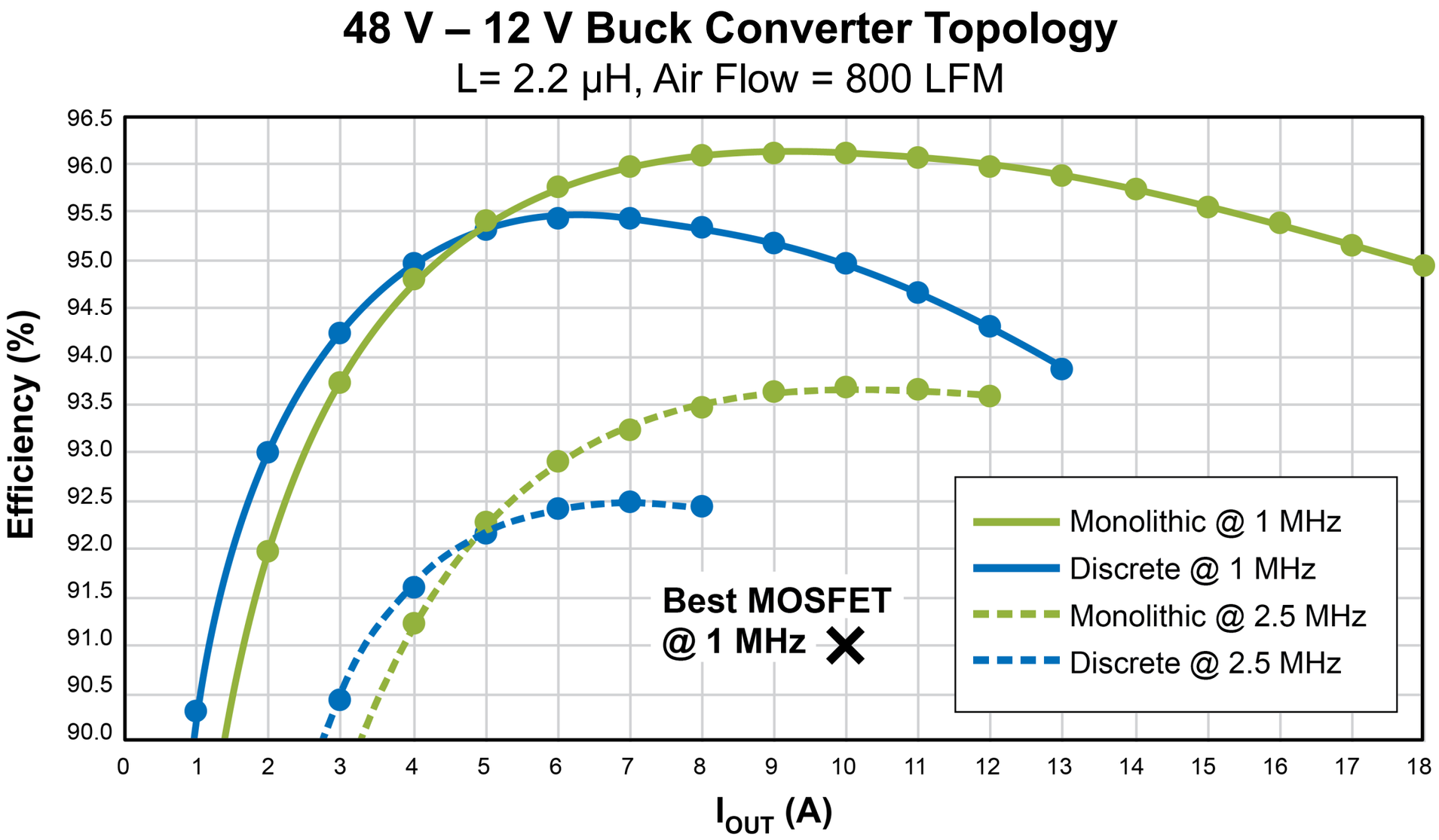
V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 10 A, f_{sw} = 1 MHz, L = 2.2 µH



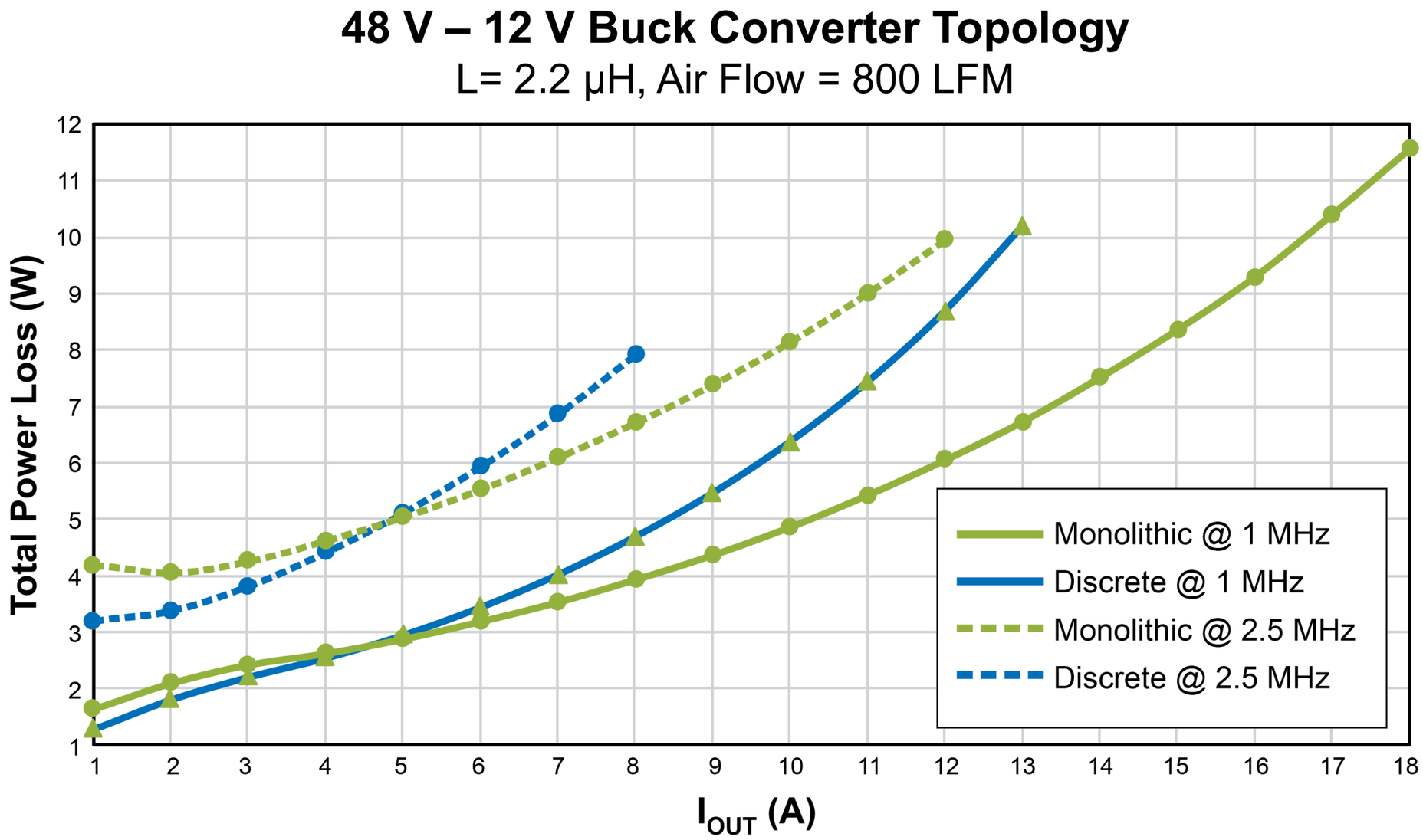


- Switching Frequencies over 1 MHz
- **1ns** Switching Time at Rated Load

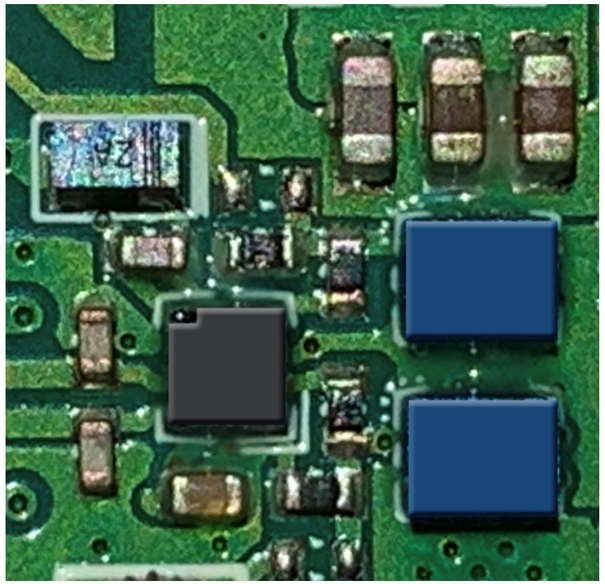
Efficiency Comparisons of Monolithic vs. Discrete Power Stage

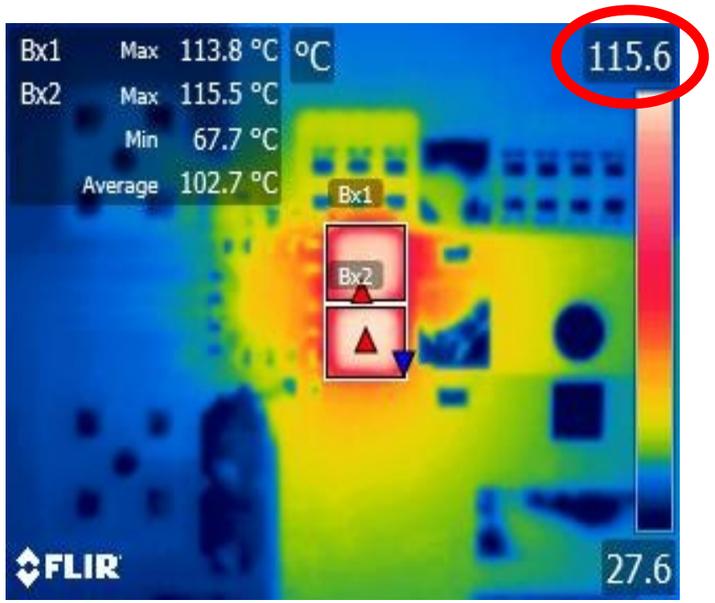


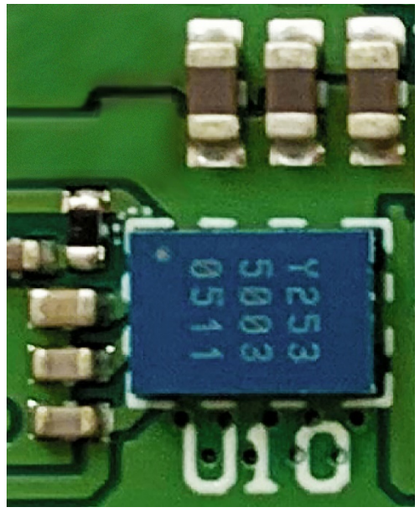
Power Loss Comparisons of Monolithic vs. Discrete Power Stage



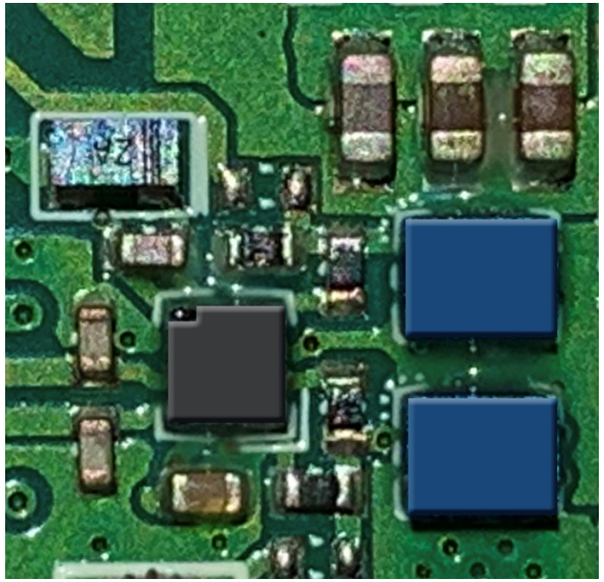
Heat Map of Discrete vs. Monolithic at 11 A for F_S = 1.0 MHz

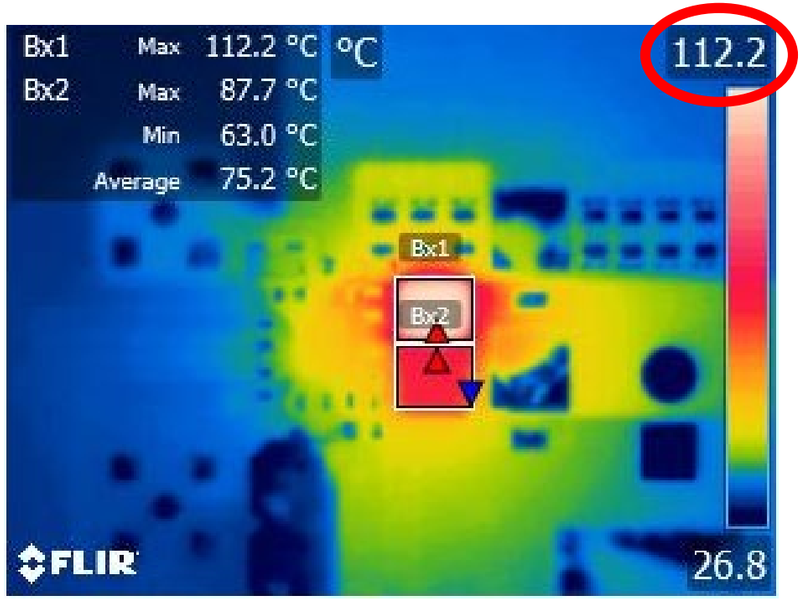


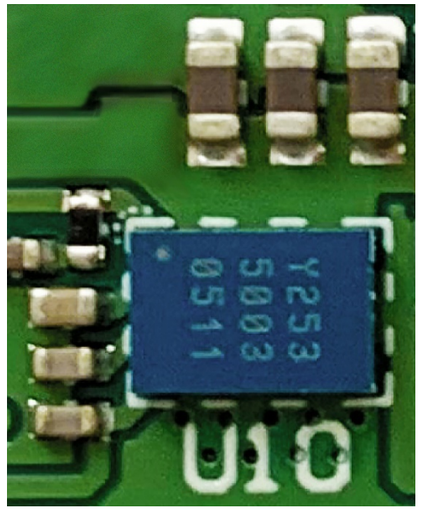


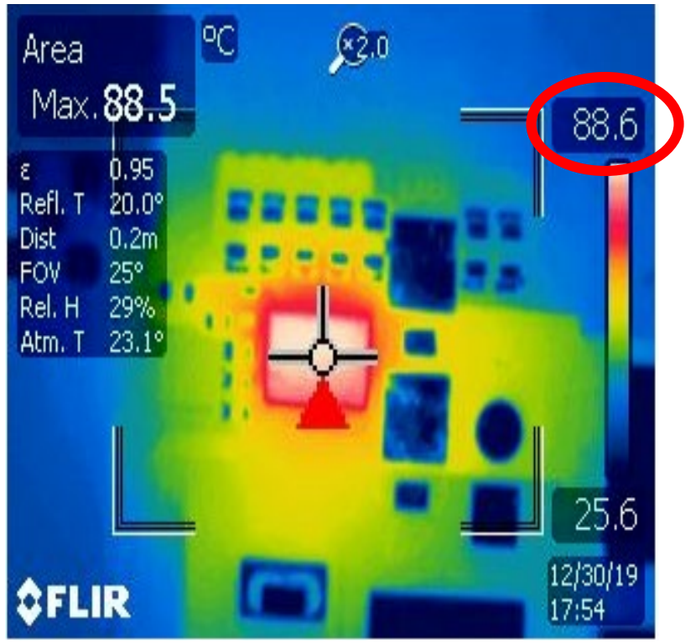


Heat Map of Discrete vs. Monolithic at 6 A for F_S = 2.5 MHz









Performance Summary

Comparison Parameter	Discrete	Monolithic
Maximum efficiency and attained current at 1 MHz	95.45% at 7 A	96.12% at 10 A
Load current at power loss of 10 W at 1 MHz	12.8 A	16.6 A
Maximum efficiency and attained current at 2.5 MHz	92.51% at 7 A	93.69% at 10 A
Load current at power loss of 8 W at 2.5 MHz	7.9 A	9.8 A
Normalized PCB area with respect to monolithic PCB	1.35	1.00

Observations and Conclusions

- EPC's eGaN® technology is at a point where integrated circuits are now a reality
- GaN integrated circuits make product designs ***smaller, easier, and faster*** to design, while increasing efficiency
- Discrete GaN implementations will become obsolete