An 800V 0.25um HVIC Technology for High Speed, Cost Efficient GaN Drivers

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800V HVIC Application Domain

• **High Performance 800V Monolithic HB Drivers** (General Purpose)
  – **NCP51530** 700V, 2.5A Dual Output Driver

• **High power adapters, ATX, LCD TV, Industrial, Medical power supplies**
  – **NCP1399** Resonant LLC controller
    • 100-300W, Low off-load consumption

• **Wide Band-Gap (GaN) Drivers**
  – **NCP51820** High Performance GaN Driver

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**Smarter & More Efficient: Maximizing the power of ON Semiconductor**
NCP51820 High Speed GaN Half-Bridge Driver

- 650-V, Integrated High-Side and Low-Side Gate Drivers
- Independent UVLO Functions for VDD, High and Low-Side Drive Regulators
- Typical 1 A/2 A Source/Sink Current
- Separate Source/Sink Driver Output Pins
- 1 ns Rise and Fall Times Optimized for HEMT and HEMT GiT GaN devices
- PGND; SW Negative Voltage Transient up to -3.5 V below SGND
- 200V/ns dV/dt Immunity
- Maximum Propagation Delay of 50 ns
- Matched Propagation Delays
- User Programmable Input Logic
  - Allow Overlapping Gate Drive
  - Cross-Conduction Prevention
  - Programmable Dead-time
- QFN 4mm x 4mm 15 Leads
800V HVIC Technology Requirements

- 800V Integrated FETs for High-Side Isolation and Level-shifting
- High Side compatible MV devices such as nLDMOS and pLDMOS
- Signal Propagation Delay < 50 ns
- NTI > -50V for 100ns (application dependent)
- dVdt immunity > 150 V/ns
- Latch-up immunity
- ESD > 2 kV HBM
- > 10 year over operating Temperature
- Electrical specs met -40C – 125C over process corner
- Full PDK support
ONC25 UHV HB Technology

- An extension of already existing 0.25um BCD baseline with addition of 2 extra masks
- Junction Isolation for High-Side monolithic integration
- Self-Shielding Integrated Level Shifters
- Spiral Poly Resistor Field Plating
- 4 and 5 Metal Layer Options
800V HVIC Isolation\Level Shifter

• A scalable 800V nJFET architecture was developed for 800V isolation and Level-shifter.
• Robust JFET architecture provides rugged design against shifts and reliability concerns.
Breakdown Voltage

- BVDSS of 800V + 150V Margin Guaranteed from Silicon Measured Data through:
  - Optimization of device architecture
  - Patented Field Plate Design
Breakdown Voltage

6 Architectural parameters optimized during development phase to enable a stable operation of level-shifters during transients

\[ \Delta V_{BD} = V_{CC} + 4V \]
Integrated ESD SCR

- >4kV HBM capability with improvement actions underway
- P+ inserted for SCR action, HVNW inserted for hole pickup
- Salicide blocked P+ to improve ESD performance
- Corner Engineering for Superior ESD performance
Negative Transient Immunity

Negative Transient Voltages can lead to:
- HVIC Output Disturbance
- Latch-up and catastrophic failure

[Diagram showing HVIC Termination and Die Edge with a 25 ns time scale and density (cm^3) ranges from 2.21e-20 to 3.21e-03]

[Graph showing failing waveforms at 50mS PW failed at -36.8V with DRVH Should Stay L]

[Image of catastrophic failure on a microchip]

Public Information
**ONC25UHV_HB** enables state of the art NTI performance that outperforms competitors.

- Substrate Engineering
- Level-Shifter Special Design
- Minority Carrier Collector Engineering
- Lifetime control
Negative Transient Immunity

- DTI Isolation protects the IC against post-NTV latch-up.
- Extensive TCAD study has proved DTI effectiveness in improving latch up resilience of the technology
ONC25 UHV HB proven to be reliable and function at dVdt up to 200V/ns