APEC - PSMA Industry Sessions
MPS and EPC Drive Efficiency and Power Density in 48V Datacenters
EPC eGaN™ enables MPS high power density fixed ratio Intermediate Bus Converters

Alex Richardson – Product Marketing, MPS
The Demand for More Power

As demand for cloud computing, AI applications, and high-power processors/accelerators grows, datacenters are evolving to accommodate new high-power requirements.

**Problem**

12V legacy power distribution too lossy for new current requirements ($I^2R$)

**Solution**

Migrate to 48V datacenter, 1/16th distribution loss

**Challenge**

$R_{DS(ON)}$ of FETs non-linear with $V_{IN}$. Similar $R_{DS(ON)}$ leads to much larger FET capacitance & switching loss

Power providers *must* adopt new technologies to improve efficiency and provide more power in the same form-factor.
MPS Design Principles

**Planar Transformer**
- Excellent Heat Dissipation for high-efficiency & density
- Low-height, easy to fit into existing server form-factor

**Primary-side GaN FET**
- Improved FOM for $R_{DS(on)}*Q_G$
- Smaller FET sizes for better form-factor

**Primary & Secondary-side FETs**
- Significant decrease of start-up stress by MP2981 soft-start control. Can power-on under severe conditions

**Synchronous Rectifier**
- Accusense™ current sensing for accurate sensing (+/-2%) without significant loss from sense resistor or passive network
- Designed as counterpart to controller for optimized control & telemetry

**Dedicated LLC Controller**
- Adjusts Frequency for Best Efficiency
- MTP for fine-tune control
- I²C/PMBus for fault and performance monitoring
**Specifications**

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>40</td>
<td>54</td>
<td>60</td>
<td>Volts</td>
</tr>
<tr>
<td>Vout</td>
<td></td>
<td>5.4</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Pout</td>
<td></td>
<td>300</td>
<td></td>
<td>Watt</td>
</tr>
<tr>
<td>Size(X &amp; Y)</td>
<td></td>
<td>18x27</td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>Total Thickness</td>
<td></td>
<td>6.1</td>
<td></td>
<td>mm</td>
</tr>
</tbody>
</table>

**Benefits:**

1. Common Footprint
2. Soft-switching for all FETs
3. OVP/UVP/OCP/OTP
4. PMBus/I²C Compatible
5. Programmable soft-start

**Efficiency vs. Output Current**

- Efficiency (%)
- I_{out} (A)
- Vin=40V
- Vin=48V
- Vin=54V
- Vin=60V
Why 48V → 12V? Key Reasons:

1. **System Development.** Easiest method for 48V migration – can reuse an existing 12V system

2. **Solution Size.** 4:1 conversion can be placed in smaller form-factor, improving system layout

Datacenter power products follow trend for higher power density & efficiency. Regardless of winding ratio or topology new techniques and technologies are vital to maintain relevance.
The electrical challenge
The Electrical Advantage

- The theoretical on-resistance versus blocking voltage of a GaN transistor is more than three orders of magnitude lower than that of silicon.

- Using the $R_{DS(ON)} \cdot Q_G$ figure of merit, GaN devices show an improvement between almost three times to more than ten times that of silicon, with larger advantages at higher voltage.

Lidow, Alex; de Rooij, Michael; Strydom, Johan; Reusch, David; Glaser, John. GaN Transistors for Efficient Power Conversion (pp. 43-44). Wiley. Kindle Edition.
High Density applications operate at fsw ~ 1 MHz

EPC transistors widely outperform alternative solution for primary (100 V or 80 V)

EPC transistors offers competitive performance for 12 V output with ½ of the size vs Si MOSFET

<table>
<thead>
<tr>
<th>Specification</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>40</td>
<td>48, 54</td>
<td>60</td>
<td>Volts</td>
</tr>
<tr>
<td>Vout</td>
<td></td>
<td>12</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Pout</td>
<td>300 W – 2.5 KW</td>
<td></td>
<td></td>
<td>Watt</td>
</tr>
</tbody>
</table>

- Shown with 2 paralleled FETs for secondary and for 4:1
eGaN FETs for LLC DCx

Primary Side eGaN FET

<table>
<thead>
<tr>
<th>Typical Specification</th>
<th>EPC2204</th>
<th>EPC2218</th>
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</thead>
<tbody>
<tr>
<td>$V_{ds,max}$</td>
<td>100 V</td>
<td>100 V</td>
</tr>
<tr>
<td>$R_{ds,on}$</td>
<td>4.5 mΩ</td>
<td>2.5 mΩ</td>
</tr>
<tr>
<td>$Q_{oss}$</td>
<td>25 nC</td>
<td>46 nC</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>0.9 nC</td>
<td>1.6 nC</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>6.4 nC</td>
<td>11.8 nC</td>
</tr>
<tr>
<td>$R_{θ,jc}$</td>
<td>1 °C/W</td>
<td>0.54 °C/W</td>
</tr>
<tr>
<td>$R_{θ,jb}$</td>
<td>2.5 °C/W</td>
<td>1.8 °C/W</td>
</tr>
</tbody>
</table>

Secondary Side eGaN FET

<table>
<thead>
<tr>
<th>Typical Specification</th>
<th>EPC2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ds,max}$</td>
<td>40 V</td>
</tr>
<tr>
<td>$R_{ds,on}$ at 4.5 $V_{GS}$</td>
<td>1.2 mΩ</td>
</tr>
<tr>
<td>$Q_{oss}$</td>
<td>45 nC</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>2.4 nC</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>18 nC</td>
</tr>
<tr>
<td>$R_{θ,jc}$</td>
<td>0.4 °C/W</td>
</tr>
<tr>
<td>$R_{θ,jb}$</td>
<td>1.1 °C/W</td>
</tr>
</tbody>
</table>

6.05 mm
The Thermal Challenge
How to achieve optimal thermal performance:

- Thermal Vias
- Gap pads
- Heat-spreader (dual sided cooling)
Vias Construction (VIPPO)

- Vias are
  - non-conductive filled (better CTE vs board)
  - plated over
  - hole diameter (typical) = 7.8 mil
  - annular ring = 13.8 mil diameter min.
  - wall thickness = 0.78 mil per IPC standard class 2
- Used for under bump and close to component pads
- Used for up to 2 oz copper thickness

Practical Example layout showing vias for EPC2204
Effect of Vias On Thermal Performance

- Vias improve heat conduction into the board
  - High thermal conduction path into the FR4 insulating layers
  - Use heat spreading in copper layers
- Board design without vias has ~18% higher FET temperature rise

Simulations with EPC2204, LLC application 750W, 6 layers 2oz PCB

With Thermal Vias

\[ T_j = 181 \, ^\circ\text{C} \]

With Thermal Vias

\[ T_j = 158 \, ^\circ\text{C} \]
Effect of Heat-Spreader Size

- Larger area heat-spreader is more effective \( \sim 52 \times A_{FETs} \)
- Small area heat-spreader \( \sim 13 \times A_{FETs} \) insufficient for optimal heat spreading

**Diagram:**

- Board only 400 lfm: \( T_j = 158 \) °C
- 11x7 mm HSp: \( T_j = 149 \) °C
- 23x17 mm HSp: \( T_j = 114 \) °C
Case A
- TIM material: 0.3 mm T-Global A1760 with $\kappa = 17.6 W/m.K$

Case B
- TIM material: 0.2 mm, $\kappa = 3 W/m.K$

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Case A $T_J(°C)$, $\Delta T(°C)$</th>
<th>Case B $T_J(°C)$, $\Delta T(°C)$</th>
<th>Increase ($°C$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu heat-spreader (23x17mm)</td>
<td>114, 89</td>
<td>121, 96</td>
<td>+ 7</td>
</tr>
<tr>
<td>Heatsink (3.5 mm total)</td>
<td>82, 57</td>
<td>90, 65</td>
<td>+ 8</td>
</tr>
<tr>
<td>Heat-spreader +Heatsink (4.5 mm total)</td>
<td>77, 52</td>
<td>86, 61</td>
<td>+ 9</td>
</tr>
</tbody>
</table>
Effect of Heatsink

- Thermal heat dissipation from the top can be further increased by using a heat sink instead of the heat spreader.

![Temperature Distribution Diagram]

- Without heatsink, temperature $T_j = 114^\circ C$
- With heatsink, temperature $T_j = 82^\circ C$

23x17 mm HSp

with HSK, no HSp
1. Distance between heatsink and FET is critical for performance: 1mm standoffs is typically used

2. Area of heatsink is critical to improve heat spreading effect

The challenge is to find low profile components that go around the FET to allow the heat sink mounting.
The Manufacturing challenge
EPC devices are available in WLCSP

This allows for the smallest PCB area utilization and highest power density
The quality of the solder bump interfacing the eGaN device to the PCB is crucial for a reliable electrical, thermal, and mechanical connection.

The top of the device is the Silicon substrate, it is not part of the active device. However, it is connected to the source potential, so care must be taken when attaching to a heat-sink.

EPC2023: 6.05 mm x 2.3 mm
MPS and EPC are pushing the limits of power density and power efficiency for datacenters 48V power

- MPC1100A is the first in a series … more to come!
- EPC eGaN enables MPS roadmap where Si is reaching its limits
How To GaN Video Series

3rd Edition Textbook

eGaN® FETs and ICs

Evaluation Kits

epc-co.com