Advanced High Power-Density Thermal Packages & Mother-Boards Enable Ultimate Power GaN & SiC Performance & Efficiency

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Power Wide-Band-Gap (WBG) Device Thermal Management

- **WBG** Compound Semiconductors are typically GaN or SiC
- WBG can have higher power-density & efficiency than silicon (Si)
- WBG places new thermal & parasitic demands on packages
- Evolving near chip-scale surface mount (SMD) packages also require high power-density & very low parasitics
- Power SMDs place special thermal & isolation requirements on their Mother-Boards
- New Thermal or Power PCB can be called PPCB
Why are Thermal Improvements so Important for WBG Packages?

- Higher efficiency may reduce losses & heating, but
- Higher power-density increases heat-flux density
- So, power-densities generally increase about twice as fast as losses reduction
- Although power dissipation is reduced, $R_{jc}$ per area must still be reduced to accommodate higher heat-flux
- SMD devices remove heat through their mother-boards, and not directly to heatsinks
- Supplementary top-side heatsinks are possible, but are usually awkward and more costly
Why do WBG Devices Demand Thermal Mother-Board or PPCB?

- SMD packages transfer heat through their PPCB
- PPCB can distribute heat to reduce PPCB heat flux density
- PPCB must provide low thermal resistance paths to attached heatsinks and/or ambient
- PPCB must provide high electrical isolation, especially for 600V to 1200V products, & higher
- PPCB can contain more system integration, improving performance, and managing heat dissipation & interconnect isolation
Traditional Si MOSFET & IGBT Power-Packages Do Not Enable Full WBG Device Performance

Historically

- Too large, complex & expensive
- Require large high R & L internal & external leads & terminals
- Contained many internal high R & L wire-bonds
- Electrically connected by PCBs/bus/cables, but thermally connected to heatsinks, and both by mechanical screws
- Hard-tool, expensive, and difficult to customize & optimize

Today

- Their size & parasitics limit power WBG device power-density speed, performance & efficiency
- Unacceptable for evolving high-performance power WBG devices
Honey, they Shrunk the Power Transistor Packages!

Figure 1: Power Semiconductor Packages (like TO220 & TO247) have Historically been large with leads to PCB & Case/Tab to Heatsink. New & smaller semiconductor SMD packages are being used for power devices, and that trend is being accelerated with smaller & more efficient WBG devices. WBG SMD packages (like QFN & LGA) are leadless & can be wire bondless with Lower R, L & Rjc. The reduced size enables multiple die in SMD packages (like QFN 3-Phase Bridge), and can include vertical integration.
But, They forgot to shrink the Modules!

Figure 2: These Large Packages are Unacceptable for WBG
Why Shrink the Packages for Power WBG Packages?

- To improve performance - lower R, L & C
- To enable mobile & miniature applications
- To enable more system integration
- To reduce materials & unit costs
- To reduces tooling costs & equipment costs
- To be flexible - soft-tooling to customize & optimize
- To use existing automatic assembly – commercial QFN & LGA assembly lines, processes & equipment
- To reduce new product risk & time to market
How does Shrinking the Package Improve Power WBG Performance?

• Shorter interconnects reduce package R, thereby reducing device conduction losses

• Shorter interconnects reduce package inductance (L), thereby increasing device speed & reducing device switching losses

• Reduced package size can reduce C, thereby increasing device speed & reducing switching losses

• Higher speed can reduce passive component size & costs

• Smaller components enables more integration, and even higher power-densities
How Do Power WBG Devices Enable Shrunken Packages?

- Smaller WBG die require less space – *assume 1/10th
- Leadless & wirebondless die require less space
- Higher efficiencies reduce power dissipation (PD) - *assume 1/5th
- Less PD reduces thermo-mechanical structures, package & system
- Smaller die reduces CTE mismatch to Cu - enabling simple direct die-to-Cu soldering – also reducing thermal resistance
- Direct soldering enables proven commercial automated assembly, reducing cost & increasing available assemblers
- Lower PD SMD enable more system integration on PPCBs
- System integration - reduces mechanical structures, and hi-voltage & hi-current connectors & costs

* Assumptions based on today’s potential – the future will be even better!
## Current & Evolving Power WBG Packages with Bench-Mark products encircled in Red

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Size</th>
<th>SMD</th>
<th>Leadless</th>
<th>Wirebondless</th>
<th>Resistance</th>
<th>Inductance</th>
<th>Rjc</th>
<th>Reliability</th>
<th>Cost</th>
<th>Manufacturing</th>
<th>Tooling</th>
<th>Integration*</th>
</tr>
</thead>
<tbody>
<tr>
<td>TO220/TO247</td>
<td>P</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>O</td>
<td>U</td>
<td>O</td>
<td>O</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td>P</td>
</tr>
<tr>
<td>BGA/LGA</td>
<td>G</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>O</td>
<td>P</td>
<td>P</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
<tr>
<td>QFN/DFN</td>
<td>G</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>O</td>
<td>P</td>
<td>G</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
<tr>
<td>PLGA</td>
<td>G</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>G</td>
<td>O</td>
<td>G</td>
<td>O</td>
<td>P</td>
<td>P</td>
<td>O</td>
<td>P</td>
</tr>
<tr>
<td>PQFN/PDFN</td>
<td>G</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>E</td>
<td>G</td>
<td>E</td>
<td>O</td>
<td>P</td>
<td>P</td>
<td>O</td>
<td>P</td>
</tr>
<tr>
<td>LGA-Embedded</td>
<td>E</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>G</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>O</td>
<td>E</td>
<td>G</td>
</tr>
<tr>
<td>LGA-Cavity</td>
<td>E</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>G</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
<tr>
<td>QFN/DFN-Cavity</td>
<td>E</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>E</td>
<td>E+</td>
<td>E+</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>G</td>
</tr>
</tbody>
</table>

**Abbreviations:**
- **E** - Excellent
- **P** - Poor
- **G** - Good
- **O** - Okay
- **U** - Unacceptable

* Vertical Integrate

Table 1: WBG Package Comparisons
Key Evolving WBG Package Types

• Leadless Laminate-based packages enable low parasitics, and higher integration, component count & connectivity, flexibility/customization & reduced time-to-market

• Leadless Leadframe-based packages enable even higher currents, powers & speeds with lower R, L & Rjc, and thick leadframes add transient heat-capacity. Robust leadless-leadframes can often replace complex & costly hi-power DBC modules

• Hybrids with leadframes for high current & top-side laminate chip-carriers for functions like gate-drivers & control, can enable the best of both world, but do add complexity & cost

• All three types are enhanced by vertical integration of supporting components & functions

• Both leadless-laminate & leadless-leadframe packages can provide very low parasitics

• Package-less Power Bump-chips like EPC’s LGA die provide excellent performance & power-density for lower voltage power GaN. But all integration is on the mother-board or within the LGA die
Common Features of the “Bench-Mark” Power WBG Packages Described in Table 1

- High power-density
- Surface Mount(SMD)
- Leadless - near chip-scale
- Wirebondless(bump-chip power die)
- Low R, C & Rjc, and very low L
- Suitable for hi-voltage & hi-current
- Integrated multi-power die & switches
- Vertical integration – components & functions
- Simple, cost effective & reliable assembly
- Flexible soft-tooling - low risk designs & optimization
Bench-Mark Leadless Laminate (PLGA) with Embedded Power Bump-Chip (like the GaNsystems GaNpx & Infineon’s Dr. Blade)

Figure 3a: Embedded Vertical FET LGA with Green Laminate, Orange Cu Foil & Laser Via, and Drain, Source & Gate External Pads

Figure 3b: Embedded Vertical FET + Gate Driver (GD) LGA with Green Laminate, Orange Cu Foil & Laser Via, and Drain, Source & Gate External Pads
Power LGA with Embedded Power Die
(like the GaNsystem’s GaNpx & Infineon’s Dr. Blade)

Key Features
• Embedded bump-chip architecture & technology
• Flexible design with laminate-base
• Low Rjc with power LGA die near package bottom
• Leads & wirebondless - lower current-loop R & L
• Multiple switches configurations (like HB), can further reduces loop R & L
• Near chip-scale provides high power-density
• Vertical integration of GD to WBG-G can virtually eliminates common-source L, enabling other component/function integration
• Enables supplementary top-side heatsink for very hi-power

Limitations
• Thin Cu foil & via limit I, R & L reductions
• Laminates limit maximum temperature & hi-temp solder
• Embedding process new/complex with mechanical & HV risk & yield issues
• Complex structures & processes increase costs
Bench-Mark Leadless Leadframe: PQFN with Power Bump-Chip in Open Bottom-Cavity (like the Semiconductor Packaging Solutions Leadframe μMaxPak)

The electrical and thermal path responsible for the low inductance, thermal resistance and thermal resistance are outlined, but all details are not shown.

The leadframe thickness is generally 0.5 mm with 0.25 mm cavity depth.

The gate drive IC in the inverted configuration can be horizontally adjacent to the FET in the same cavity, but will have slightly higher output-to-gate inductance.

The electrical and thermal path responsible for the low inductance, thermal resistance and thermal resistance are outlined, but all details are not shown.

The leadframe thickness is generally 0.5 mm with 0.25 mm cavity depth.

In the half-bridge configuration, there are two adjacent cavities and the hi-side source connects to the lo-side drain.

(The drawings are not to scale, and the electrical connections are structurally symbolic)
**Bench-Mark Leadless Leadframe: PQFN with Power Bump-Chip in Open Bottom-Cavity**

(like the Semiconductor Packaging Solution Leadframe μMaxPak)

Figure 4c: μMaxPak Single-Switch Cross-section showing inverted vertical power FET die in bottom-side leadframe cavity with drain to leadframe. The molding compound is black and the solder is gray.

The electrical and thermal path responsible for the low inductance, thermal resistance and thermal resistance are outlined, but all details are not shown.

Leadframe thickness is generally 0.5 mm with 0.25 mm cavity depth.

(The drawing is not to scale)
μMaxPak QFN Potential Measurables with 5x5mm Power WBG die in Bottom-Cavity

Key Features

- Proprietary architecture enables double-side (DS) QFN leadframe assembly
- Flexible design with soft-tooled QFN leadframe
- Compatible with commercial QFN assembly line
- Lowest Rjc (0.1 °C/W*) with exposed power bump-chip bottom-cavity(s), and heavy Cu to top-side die pads
- Leadless & wirebondless - lowest current-loop R(100-200 μohm*) and L(0.1-0.2 nH*)
- Lower capacitance coupling & RFI
- Multiple power switch configuration (like HB) further reduces loop R & L
- Highest near chip-scale power-density
- Vertical integration of GD above power WBG gate pad can virtually eliminate common-source L, enabling other component/function integration
- Enables supplementary top-side heatsink for very hi-power

Limitations

- Robust Cu leadframe limits hi-complexity - may require top-side laminate chip-carrier for functions (like cascode FET & controller)
All WBG Die not Created Equal, which can Influence Package Complexity, Fit & Costs

- Vertical vs lateral power die
- Efficiency & Power-Density vary with type of GaN & SiC technology
- Isolated vs non-isolated die substrates
- Unique die pad configuration & spacing
- Normally-Off(enhanced-GaN) vs Normally-On(depletion-GaN) with cascode FET, and some SiC(JFET) like UnitedSiC’s cascoded devices
- Anti-paralleled diodes, typically for JFET & BJT SiC die
- Die thermal conductivity & cost differences for Si, GaN or SiC substrates
- Single vs Parallel die per switch
- Standard vs special gate-drive requirements
How Do You Remove Heat from a Shrunken Power SMD Packages?

High power-density WBG packages can be near zero Rjc, but soldered to isolated mother-boards. New PPCB mother-boards with low thermal resistance can utilize some old & new techniques:

• Heavy Cu foil & filled thermal Cu via
• Thermal pre-preg(T-preg) in PPCB or IMS(insulated metal substrate)
• DBC Substrates with Al2O3, Si3N4 or AlN ceramic isolators
• Embedded Cu Heatslugs
• Embedded Isolated DBC Heatslugs*
• Heatsink(s) or cold-plate attached to PPCB
• Forced-Air Convection

* Embedded DBC thermal resistance can be lower than module DBC substrates, being smaller & thinner.
Power PCB & Substrate Thermal Resistance Case-to-Sink (Rcs) with 5x5 mm Die in PQFN

1) Heatsink soldered to back of PPCB
2) Calculations use commercially available T-preg & DBC
3) Calculations use isolator thickness rated >3.5 & 5.0 kVA for 600V/1200 V product, respectively
4) In best PQFN with Rjc<0.1 °C/W, Rjs & Rcs are about the same
High-Speed WBG Devices Require Lower Capacitance to Heatsink(Ground) at Mother-Board Isolation Layer

- There are compromises between capacitance, thermal resistance & isolation voltage, and product requirements define what is optimum
- \( C = \frac{KA}{t} \), where \( C = \) capacitance, \( K = \) dielectric constant, \( A = \) area & \( t = \) thickness
- Increased Thickness - reduces capacitance, increasing thermal resistance & BV
- Typical thickness – T-preg=4mil(3.5KV) & 6mil(5.0KV), Al\(_2\)O\(_3\)=20mil(module) & Al\(_2\)O\(_3\)=10mil(embedded-LGA) and AlN=25mil(module) & AlN=15mil(embedded-LGA)
- Increased Area – increases capacitance, reducing thermal resistance
- Dielectric Constant - properties of isolation material & frequency. Typical dielectric constants @ 1MHz are T-preg=4.0-7.5, Al\(_2\)O\(_3\)=9.0 & AlN=8.5
- WBG die may be 10% Si die area, and leadless & wire bondless embedded isolators area may be 5% the power module DBC area
- Reduced isolator area is a key advantage for New WBG packages & mother-boards with potentially 5% the capacitance die to ground
Ultimate Power WBG Packages are:

- Near Chip-Scale - High power-densities
- Leadless & Wire Bondless - Maximum speed & efficiency
- Near-zero Package Rjc - In SMD Packages
- Vertically Integrated - Added functions with even higher power-density, speed & efficiency
- Used with Power Mother-Boards - Manage HV Isolation & high heat flux densities to heatsink
- Used with Mother-Board System Integration - Higher product power-density & performance
- Built on QFN & LGA Platform - Commercial assembly for low cost, availability, flexible & short time-to-market