Monolithic GaN Integrated Power Stages and Gate-Drivers: The Next Level

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Challenges of Driving GaN

Pitfalls

A GaN HEMT is NO MOSFET:

• Lower and tighter controlled gate turn-on voltage
• Lower threshold voltage ($V_{th}$)
• Significantly faster Turn On and Off times -> High $dV/dt$
• Lower $C_{gate-source} / C_{drain-gate}$ ratio

⇒ An ideal recipe for expensive fireworks
⇒ Needs an optimized gate-drive approach
Challenges of Driving GaN

On PCB level:
- Gate-loop inductance
- Supply inductance
- Gate resistors
- Drain-source inductance

On Gate-driver IC level:
- Dead-time control
- LS/HS delay-matching
- $dV/dt$ immunity
- Negative source voltage = GND inductance
- Gate overcharging
Challenges of Driving GaN

Block Diagram MDC901

Co-integrate
Gate driver and
GaN power stage

Monolithic GaN IC

Silicon IC

GaN

Co-integrate Gate driver and GaN power stage

MDC901
The Ultimate Solution: Monolithic GaN ICs

The Delta

- Reduce # external components in the system
- Getting GaN up to speed by killing gate-loop parasitics
- Reliability: minimize the gate voltage overshoot
- Increasing the overall system power density
The Ultimate Solution: Monolithic GaN ICs
Technology Makes the Difference

• SOI wafer as base for GaN HEMTs

TEM cross-section of GaN/AlGaN superlattice-based buffer on SOI substrate.

• DTI to electrically insulate HEMTs from each other

Schematic cross-section of GaN-on-SOI structure, featuring buried oxide, oxide filled deep trench, local substrate contact and p-GaN HEMT devices.

pictures courtesy of IMEC
Point-of-Load GaN IC Implementations

First Iteration

- Monolithic Half-Bridges for PoL DCDC
- 200V / 10A RMS
- HS & LS Gate-Drive integrated
- HS & LS decoupling / BS cap integrated
- <10ns propagation delay
- ns turn-on/off
- LS current sensing
- Temperature sensing

No concerns about the gate-driver!
Point-of-Load GaN IC Implementations

First Iteration: The Assembly symmetrical version

• Chip-on-Board: FR4 and AluOx
Point-of-Load GaN IC Implementations

First Iteration: The Assembly asymmetrical version

- Chip-on-Board: FR4
Point-of-Load GaN IC Implementations

Second Iteration

- Monolithic Half-Bridge for PoL DCDC
- 200V / 10A RMS
- HS & LS Gate-Drive integrated
- HS & LS decoupling / BS cap integrated
- Isolated level-shifter integrated
- HS & LS Floating Supplies for gate-drive
- Dead-time control integrated
- Temperature sensing

No concerns about the gate-driver!
Point-of-Load GaN IC Implementations

Second Iteration: The Real Thing

- 9.3 x 3.8mm²
- GaNIC4S ESA Project
Point-of-Load GaN IC Implementations

Second Iteration: The Assembly

- Chip-on-Board: FR4
- 125um Bondwires for Power
- 50um Bondwires for signals & test pads
GaN IC Measurements

Second Iteration Efficiency

Sample S4 Efficiency vs I_{out}
300KHz DC = 8%

48V in -> 3.3V out

Sample S4 Overall Efficiency vs I_{out}
300KHz DC = 25%

48V in -> 12V out
GaN IC Measurements
Second Iteration Signals

• On-chip dead-time generation
GaN IC Measurements

Second Iteration Signals

• On-chip Isolated Level-Shifter, off-chip transformer

40MHz RF signal

PWM input

Modulator output

Demodulator input

PWW output
GaN IC Measurements

Second Iteration Signals

• Switching Buck Converter
Future Work

• Measure prototype resistive type level-shifters (no galvanic isolation, higher speed)
• Add over-current / de-saturation protection
• Add current sensing
• Add a closed-loop control system
Conclusions

• GaN HEMTs are not inexpensive components, thus to maximize GaN benefits - Get Your Gate DRIVE(R) Right!

• Monolithic GaN IC enables the true benefits of GaN
  ▪ transient speed
  ▪ low losses
  ▪ Reliability
  ▪ Power density

• The future of GaN is monolithic power stages and integrated gate-drive + level-shifters
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