High voltage integrated Smart GaN boosting consumer applications

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• High-performance power converters need Smart power integrated devices

• Need for simplification

• Power system-in-package devices integrate gate drivers and half-bridge enhancement mode GaN transistors

• No need for additional external components
Integrated Smart GaN

- The structure of the gate driver ensures more effective driving of each transistor by minimizing current loops
- Thermal management is easier
- The integrated power GaN switches are enhanced mode transistors fully exploiting the zero-recovery characteristic of the HEMT
Block diagram at a glance

Digital section Supply

Integrated DBoot

Floating driver Supply

High Side GaN

Low Side GaN

Low side driver Supply
1. Level shifters are implemented
2. Different turn-on and off current capability
3. Prevention of accidental GaN turn-on when PVCC and VBO are below turn on threshold.
Reverse conduction operation

- GaN FET's channel can operate in direct or reverse conduction mode
- The reverse conduction results in large reverse voltage drop across source to drain terminals
- The reverse conduction is typical in resonant topologies
- Large voltage can create large dissipation → dead time optimization is important to reduce the power dissipation on both Low side and High side
- Reverse conduction of low side generates negative voltage on OUT pin
Supply sources - consumptions

• Input logic section has quiescent current < than 900µA

• Low side driver, when there is no switching activity and gate is low, exhibits negligible power consumption

• High side driver – with no switching activity and low gate - exhibits an extremely low power consumption: 220µA

• Low voltage rail compatibility (6V typ) allows low power consumption
Logic inputs – truth table

<table>
<thead>
<tr>
<th>Input pins</th>
<th>GaN transistors status</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD/OD</td>
<td>LIN</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
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<tr>
<td>H</td>
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1. X: Don’t care

Disabled input port
Normal Operation Configurations
Interlocking

Normal Operation
Interlock
Input disabled
Logic inputs – propagation delays

$T_{d_{GL}}$ and $T_{d_{GH}}$: matched between on, off HS and LS

$T_{(GaN)}$: $T_{(GaN)} \ll T_{d_{Gx}}$

Turn on delay time is negligible when compared with $T_{(driver)}$

$LIN$ or $HIN$

$LON$/LOFF or HON/HOFF

$GL$, $GH$

$SD$/OD

$t_{(On)}$, $t_{(OFF)}$, $t_{SD}$
How to prepare a PCB for heatsink application

Board: 40mm x 40mm x 1mm FR4
Copper: 2 layers 70µm
Vias: Filled with CU

Estimated
Rth,j-bot = 9.5°C/W
Rth,j-a = 59°C/W
(ideal case with no external pins)

Design

Real board - Top

Real board – Bottom
(Heatsink interface)
Typical applications

Typical examples of topology for consumer applications
- low to high output power levels up to 500W

Active Clamp Flyback (ACF)
Resonant LLC converter (LLC)
Typical topologies
LLC resonant

- Suggested 6V typ
- Suggested 10Ω
- Hi performance Ceramic Cap to be as close as possible between Vs and Sense
- RC network for OTP extended time constant
- Shunt is optional: lossless Capacitive divider on resonant capacitor is normally used
250W LLC converter

Integrated Smart GaN

Synchronous rectification
Suggested 6V typ

Typical topologies
Active clamp flyback

Hi performance Ceramic Cap to be as close as possible between HV and Sense and between HV and VS

Suggested 10ohm

Shunt is very common: LS driving is guaranteed until the voltage difference between PGND and GND is within +/-2V 😊
Application example – ACF with SR
Application example – ACF with SR

Efficiency measurements
Conclusion

• The integrated Smart GaN device in half-bridge configuration is a viable solution for easy and safe design of low power building blocks for power converters

• Thanks to the integration both electrical and thermal designs are straightforward and robust

• The high voltage integrated approach is fully exploited in consumer applications where performance, size and cost are the key selection criteria
THANK YOU!