A Deep Dive of Isolated Gate Driver Robustness – $\text{dv/dt (CMTI)}$

Zhang, Wei, Texas Instruments

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Why is Isolation Required?

- A) Safety
- B) Breaking ground loop – CM noise
- C) Power delivery – $V_1/V_2 = N_1/N_2$
- D) Signal Communication

<table>
<thead>
<tr>
<th>Voltage Line-to-neutral $V_{\text{RMS}}$</th>
<th>1min DC Test Voltage *</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Insulation and Supplementary Insulation</td>
<td>Reinforced Insulation</td>
</tr>
<tr>
<td>$\leq 150$</td>
<td>$1900V$</td>
</tr>
<tr>
<td>$&gt;150, \leq 300$</td>
<td>$2100V$</td>
</tr>
</tbody>
</table>

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What is the Popular Isolation methods in gate driver?

• **A) Optocoupler**
  – Signal transfer between two isolated circuits using light – LED + phototransistor, 1970s ~ (Avago, Fairchild, Toshiba and others)

• **B) Transformer**
  – Integrated micro-transformer and electronic circuitry, 2001~ (ADI, Infineon, Rohm and others)

• **C) Capacitor**
  – Signal transmission through capacitive isolation with On-Off-Keying (OOK) modulation, 2004~ (Silabs, TI and others)
TI’s Capacitive Isolation Technology

- SiO₂ is the most stable dielectric over temperature and moisture
- Distance through insulator is commensurate with dielectric strength
  - Breakdown field is 500-800V/um (vs. <50V/um for silicon/mold compound in optocoupler*)
  - Highest lifetime in the industry, >1.5 kV_{RMS} for >40 years
  - Superior transient protection for harsh environments, >12.8kV
  - High CMTI

* Typical values are used. Data is for approximate comparison purposes only
What is CMTI?

- Definition: Common mode transient immunity, CMTI, is the maximum tolerable rate-of-rise (or fall) of the common-mode voltage. It is given in kV/us, or V/ns.
What is the Static CMTI?

- Static CMTI Criteria: Maximum slew rate of $V_{CM}$ at which the output of the coupler (OUT) remain at the specified (logic) high or low level.

Static CMTI - $CM_H$

Static CMTI - $CM_L$
What is the Dynamic CMTI?

- **Dynamic CMTI Criteria:** Maximum slew rate of $V_{CM}$ with switching edge ($H \rightarrow L, L \rightarrow H$) coincident or near to the common mode transient pulse.

![Diagram showing IN, OUT, and CMT signals with normal, missing pulse, delay, H or L error, and latch stages.]
**Why CMTI is so Critical?**

**GaN - Cascode**  
**State-of-Art Silicon**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>600V Si</th>
<th>600V GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>600V</td>
<td>600V</td>
</tr>
<tr>
<td>$R_{DS}$</td>
<td>0.14Ω$^0$</td>
<td>0.15Ω$^0$</td>
</tr>
<tr>
<td>Dynamic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{OSS(Tr)}$</td>
<td>314pF$^2$</td>
<td>71pF$^2$</td>
</tr>
<tr>
<td>Reverse Operation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>8200nC$^3$</td>
<td>42nC$^4$</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>460ns$^3$</td>
<td>24ns$^4$</td>
</tr>
</tbody>
</table>

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[1] GaN: TPH2006; Si:IPx60R160C6

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![dv/dt (I_{OFF}=15A) Diagram](image)
Why CMTI is so Critical?

W. Zhang, X. Huang, F. C. Lee and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," APEC 2014

Primary GND noise

PWM_T (5V/div)

V_{gsT} (10V/div)

V_{SW} (100V/div)

I_L (5A/div)

W. Zhang, X. Huang, F. C. Lee and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," APEC 2014

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UCC2152x: 4A, 6A, 5.7kV\textsubscript{RMS} Isolated Dual Channel Gate Driver

5.7kVrms isolation voltage with \textbf{100V/ns} Min. CMTI

The first of a new isolation family in TI's gate driver portfolio

DT, UVLO, etc. and optimized switching performance

Flexible – used as a low-, high-, high-/low- or half-bridge driver.

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How to Characterize CMTI for UCC2152x?

Common Mode Surge Generator

Passive Probe BW=1GHz
Off-the-Shelf Common Mode Surge Generator

- Typical Features
  - R-C Charge/Discharge
  - No parasitic induced overshoot or undershoot
  - $\leq 400\text{V}$, or $\geq 4\text{kV}$

Source: NoiseKen
How to Generate Programmable CMTI Rising Slew Rate to Emulate End Equipment?

\[ I_L = \frac{V_{Chg} \cdot T_{ON}}{L_f} \]

\[ \frac{dV_{CMT}}{dt} = \frac{I_L}{2 \cdot (C_{OSS} + C_D)} \]

\[ \frac{dV_{CMT}}{dt} \propto V_{Chg} \bigg|_{T_{on}, L_f=\text{const.}} \]
CMTI Rising Slew Rate Example Waveform

\[
\frac{dV_{CMT}}{dt} \propto V_{Chg} \bigg|_{T_{on}, L_f=\text{Const}}.
\]

\( V_{CMT} \)

\( L_f \)

\( C_D \)

\( V_{CM} \)

(400V, 800V, 1200V)

\( I_L \)

\( V_{Chg} \)

\( C_{OSS} \)

\( d \)

\( \alpha \)

\( \bigg|_{T_{on}, L_f=\text{Const}} \)

\( \propto \)
System Configuration for Rising Slew Rate

- Battery ≈28V
- LDO 3V to 18V
- Common Mode Surge Generator
- Passive Probe BW=1GHz
- LDO Output 3V to 18V
- Battery ≈28V
- Lf inductor
- Vchg
- VCC, GND
- Input Logic
- Reinforced Isolation
- Functional Isolation
- PW-100us, f_s=200Hz

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How to Generate Programmable CMTI Falling Slew Rate?

\[ V_{\text{Chg}} \]

\[ L_f \quad I_L \]

\[ C_{\text{OSS}} \quad V_{\text{CM}} \]

\[ (400V, 800V, 1200V) \]
How to Generate Programmable CMTI Falling Slew Rate?

$$\frac{dV}{dt} \propto V_{Chg} \bigg|_{T_{on}, L_f = \text{Const.}}$$

$(400V, 800V, 1200V)$
CMTI PCB Design

Bottom Layer

Falling Slew

Rising Slew

Top Layer

Daughter Card with DUT
CMTI Hardware Design and Measurement Considerations

- MOSFET, SiC-MOSFET, or GaN with small $C_{\text{OSS}}$;
- SiC Diode with small $C_{\text{D}}$;
- Air core inductor with small parasitic winding capacitance;
- Minimization of two separate ground capacitive coupling;
- Use floating battery to drive the high side switch for falling slew CMTI, instead of isolated power supply;
- **Characterization on measurement location and DUT**
CMTI Measurement Location

Right Next to DUT

Under PCB due to Thermal Stream
CMTI Test Setup Characterization

175V/ns

201V/ns

Same Test Condition
CMTI Test Setup Characterization

\[ y = 0.0005x^2 + 0.0467x + 4.4635 \]

\[ y = 0.0368x + 24.864 \]
CMTI Measurement Data for UCC21520

- VCCI=12V, VDD=25V
Summary

• Isolation in gate driver
• Deep dive of common mode transient immunity (CMTI)
• Bench CMTI design, measurement and design considerations

THANK YOU