APEC 2★18
SAN ANTONIO, TEXAS ★ MARCH 4-8
THE PREMIER GLOBAL EVENT IN APPLIED POWER ELECTRONICS™

A Deep Dive of Isolated Gate Driver Robustness – dv/dt (CMTI)

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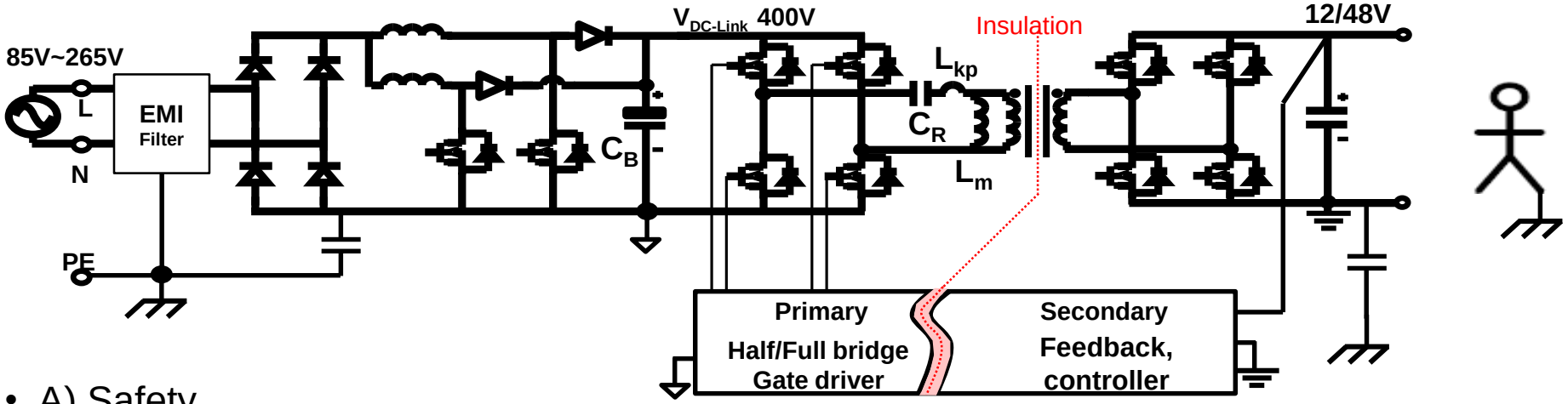
Mar. 6th, 2018

Why is Isolation Required?



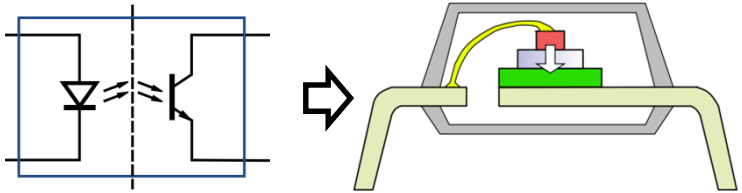
- A) Safety
- B) Breaking ground loop – CM noise
- C) Power delivery – $V_1/V_2=N_1/N_2$
- D) Signal Communication

Voltage Line-to-neutral V_{RMS}	1min DC Test Voltage *	
	Basic Insulation and Supplementary Insulation	Reinforced Insulation
≤150	1900V	3800V
>150, ≤300	2100V	4200V

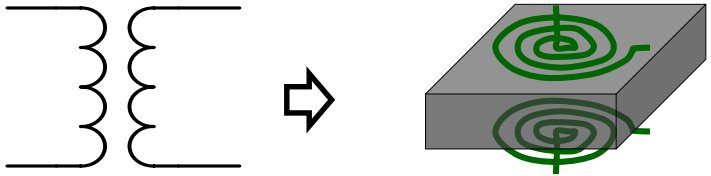
* *IEC61010-1 ed. 3.0*

What is the Popular Isolation methods in gate driver ?

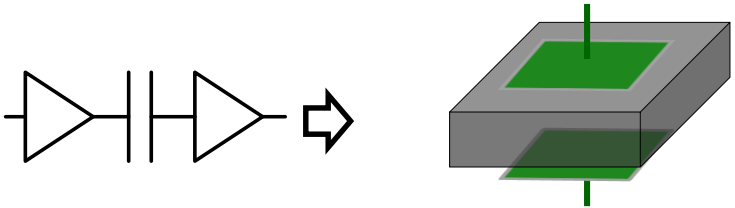
- A) **Optocoupler**
  - Signal transfer between two isolated circuits using light – LED + phototransistor, 1970s ~ (Avago, Fairchild, Toshiba and others)



- B) **Transformer**
  - Integrated micro-transformer and electronic circuitry, 2001~ (ADI, Infineon, Rohm and others)

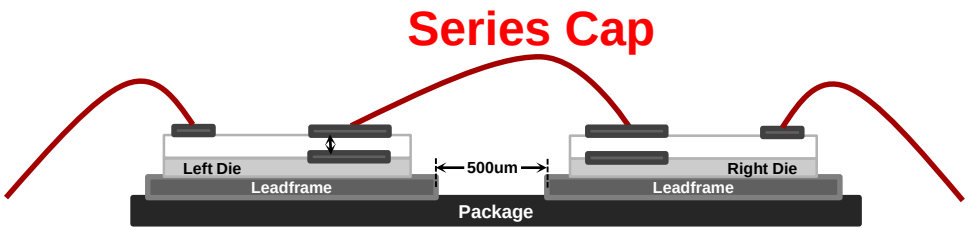


- C) **Capacitor**
  - Signal transmission through capacitive isolation with On-Off-Keying (OOK) modulation, 2004~ (Silabs, TI and others)



TI's Capacitive Isolation Technology

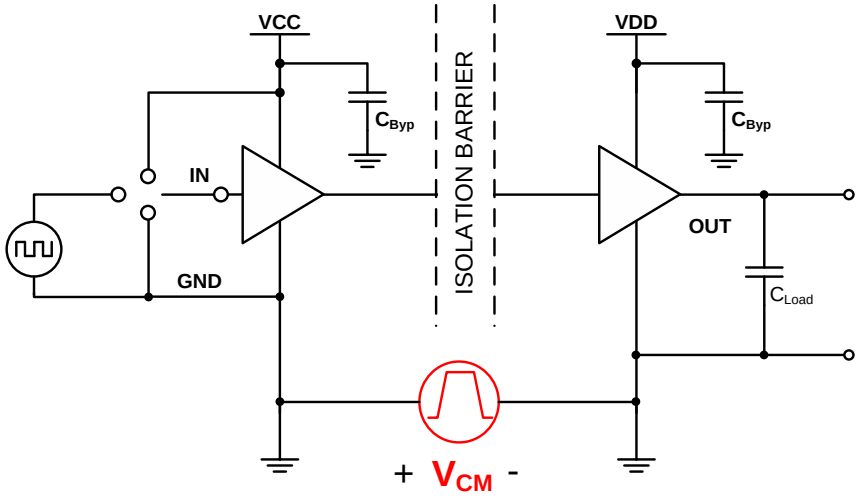
- **SiO_2 is the most stable dielectric over temperature and moisture**
- **Distance through insulator is commensurate with dielectric strength**
  - Breakdown field is 500-800V/um (vs. <50V/um for silicon/mold compound in optocoupler*)
  - Highest lifetime in the industry, >1.5 kV_{RMS} for >40 years
  - Superior transient protection for harsh environments, >12.8kV
  - High CMTI

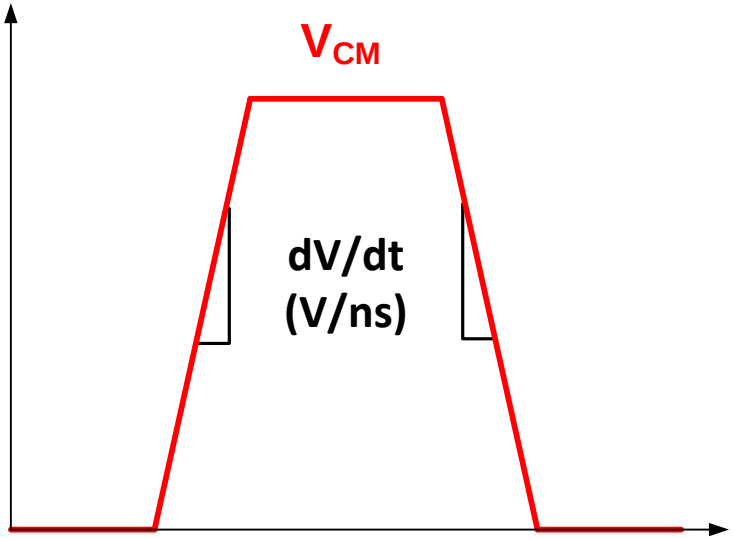


* Typical values are used. Data is for approximate comparison purposes only

What is CMTI?

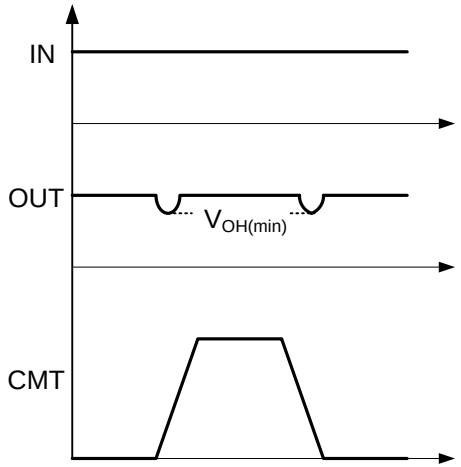
- Definition: Common mode transient immunity, CMTI, is the maximum tolerable rate-of-rise (or fall) of the common-mode voltage. It is given in kV/us, or V/ns.



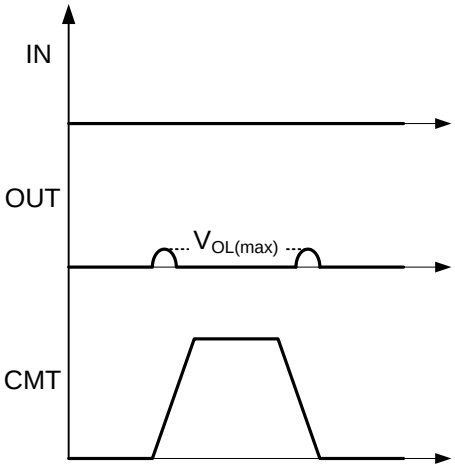


What is the Static CMTI?

- Static CMTI Criteria: Maximum slew rate of V_{CM} at which the output of the coupler (OUT) remain at the specified (logic) high or low level.



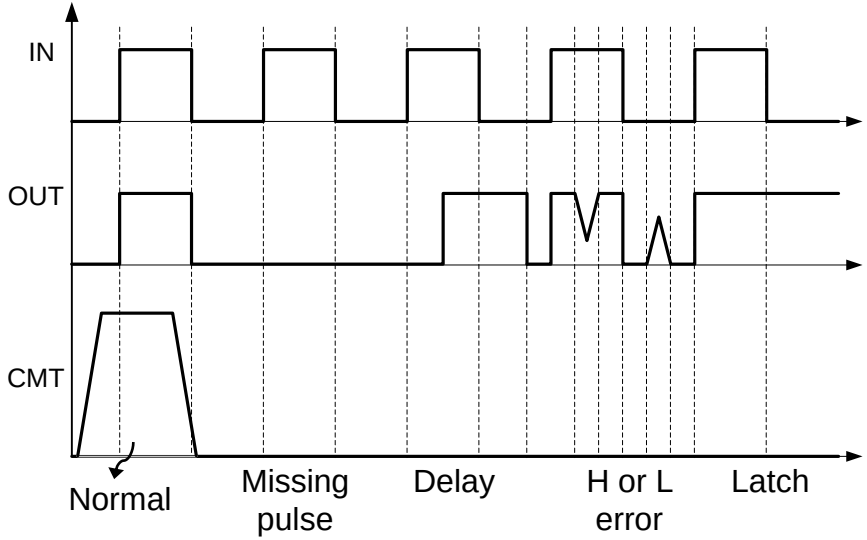
Static CMTI - CM_H



Static CMTI - CM_L

What is the Dynamic CMTI?

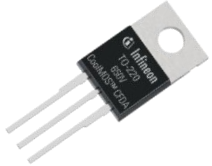
- Dynamic CMTI Criteria: Maximum slew rate of V_{CM} with switching edge (H→L, L→H) coincident or near to the common mode transient pulse.



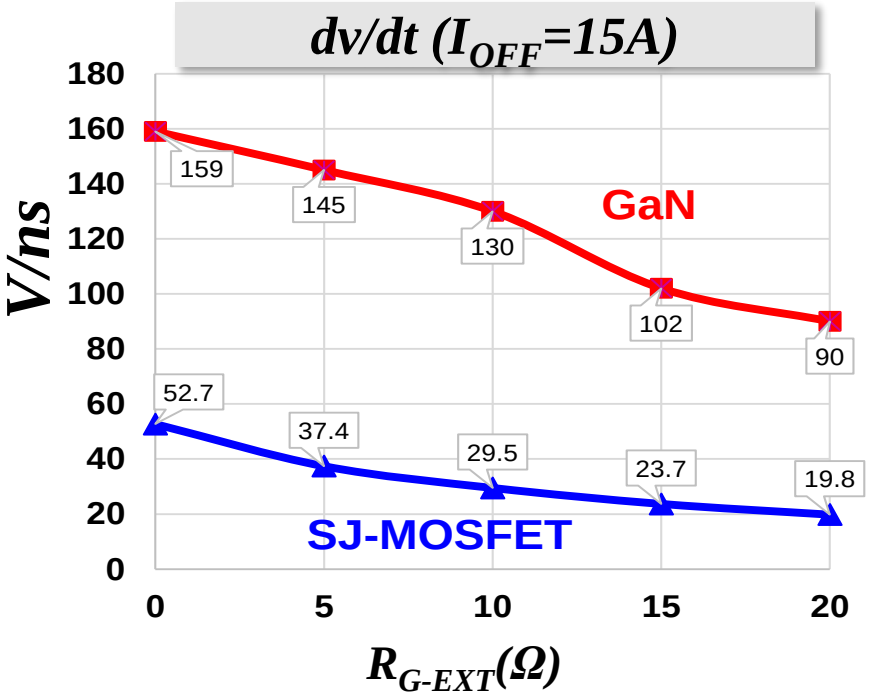
Why CMTI is so Critical?

GaN - Cascode

State-of-Art Silicon

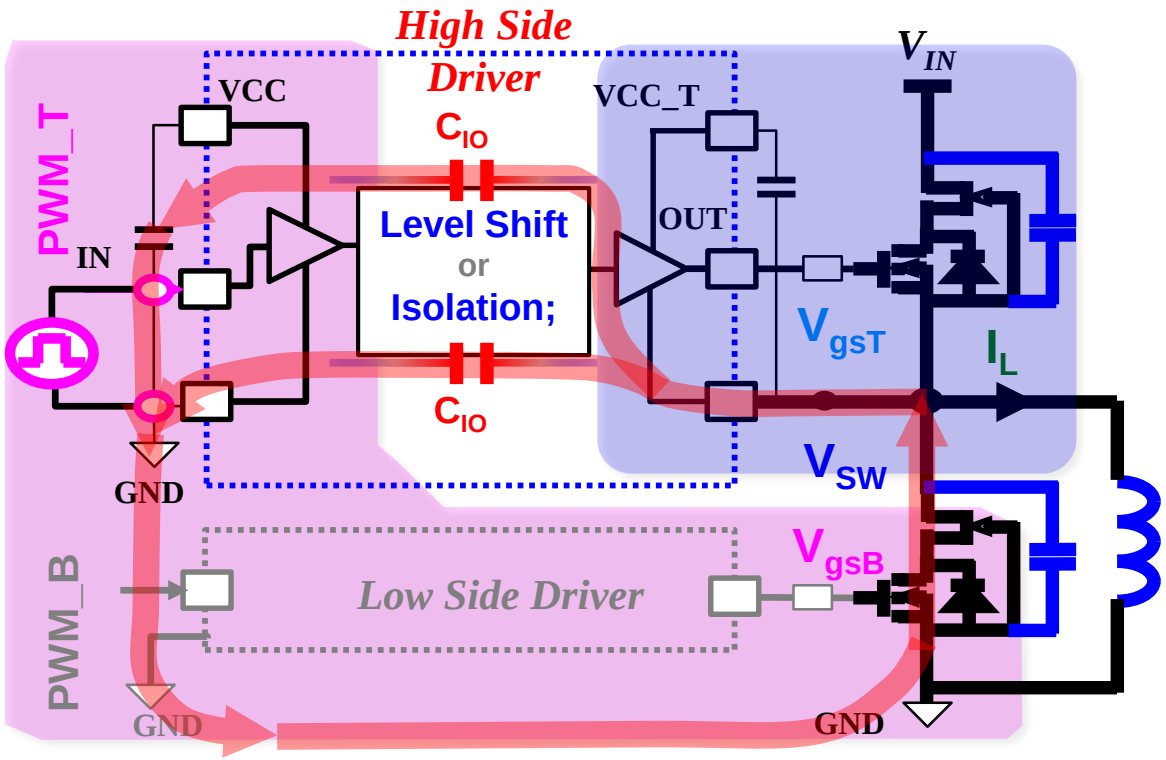


	Parameter	600V Si	600V GaN
Static	V_{DS}	600V	600V
	R_{DS}	0.14Ω[0]	0.15Ω[0]
Dynamic	$C_{OSS(Tr)}$	314pF[2]	71pF[2]
Reverse Operation	Q_{rr}	8200nC[3]	42nC[4]
	t_{rr}	460ns[3]	24ns[4]

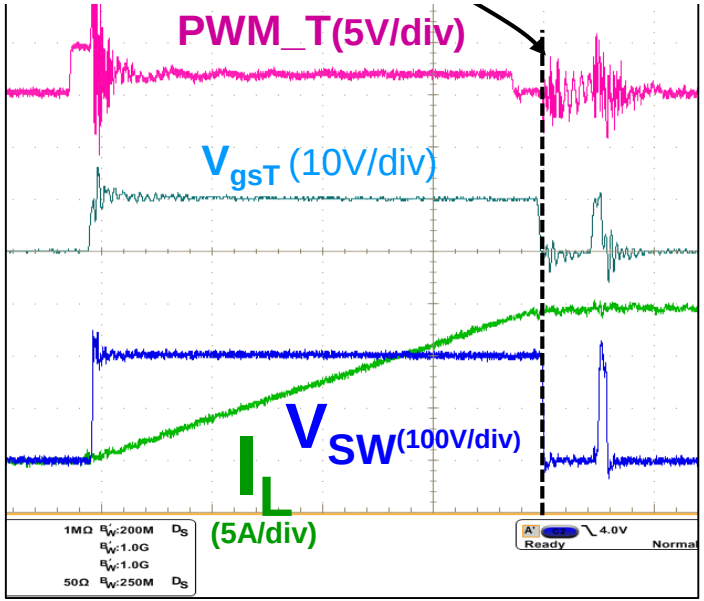


[1] GaN: TPH2006; Si:IPx60R160C6

Why CMTI is so Critical?

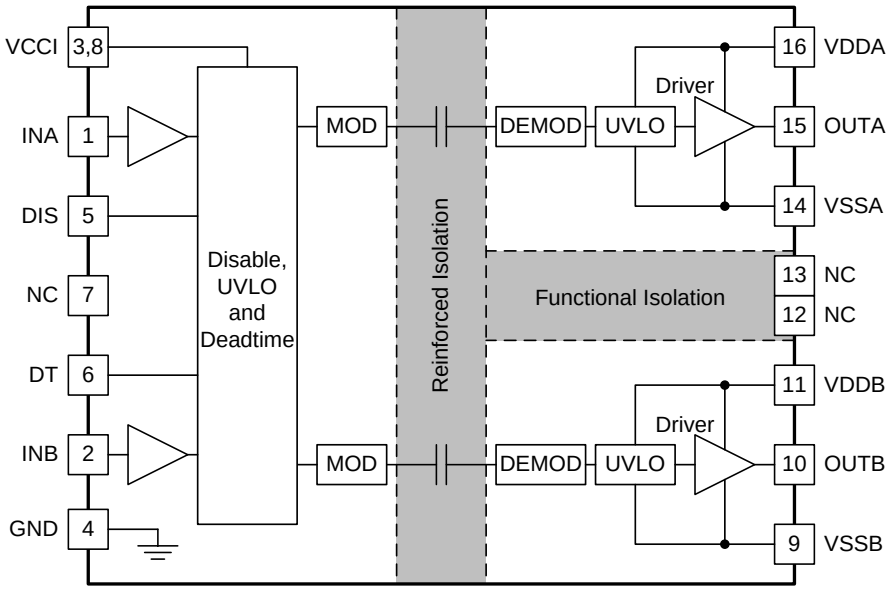


Primary GND noise



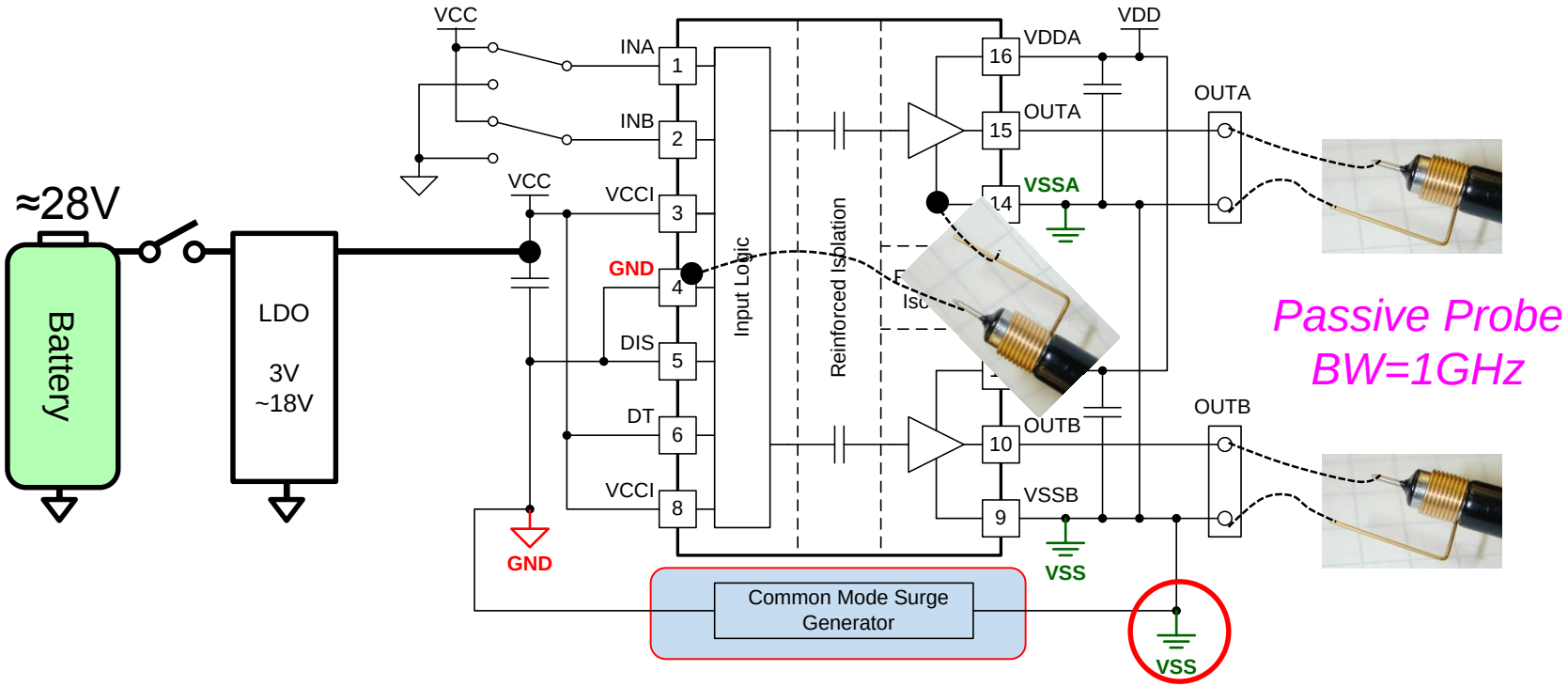
W. Zhang, X. Huang, F. C. Lee and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," *APEC 2014*

UCC2152x: 4A, 6A, 5.7kV$_{RMS}$ Isolated Dual Channel Gate Driver



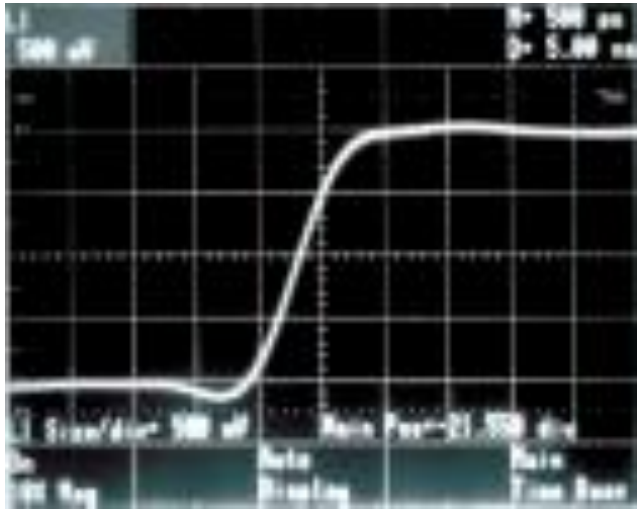
- 5.7kVrms isolation voltage with **100V/ns** Min. CMTI
- The first of a new isolation family in TI's gate driver portfolio
- DT, UVLO, etc. and optimized switching performance
- Flexible – used as a low-, high-, high-/low- or half-bridge driver.

How to Characterize CMTI for UCC2152x?



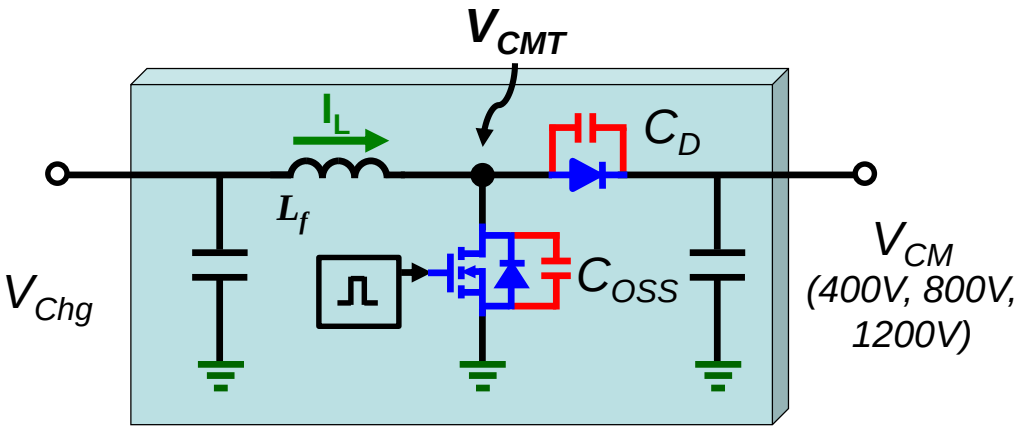
Off-the-Shelf Common Mode Surge Generator

- Typical Features
  - R-C Charge/Discharge
  - No parasitic induced overshoot or undershoot
  - ≤400V, or ≥4kV



Source: NoiseKen

How to Generate Programmable CMTI Rising Slew Rate to Emulate End Equipment?



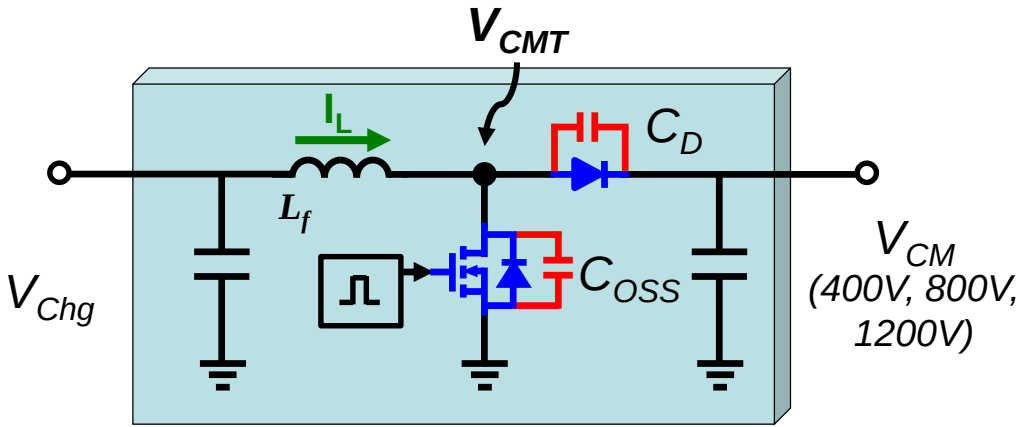
$$I_L = \frac{V_{Chg} \cdot T_{ON}}{L_f}$$

$$\frac{dV_{CMT}}{dt} = \frac{I_L}{2 \cdot (C_{OSS} + C_D)}$$

$$\frac{dV_{CMT}}{dt} = \frac{V_{Chg} \cdot T_{ON}}{2 \cdot L_f \cdot (C_{OSS} + C_D)}$$

$$\frac{dV_{CMT}}{dt} \propto V_{Chg}\Big|_{T_{on},\, L_f = Const.}$$

CMTI Rising Slew Rate Example Waveform



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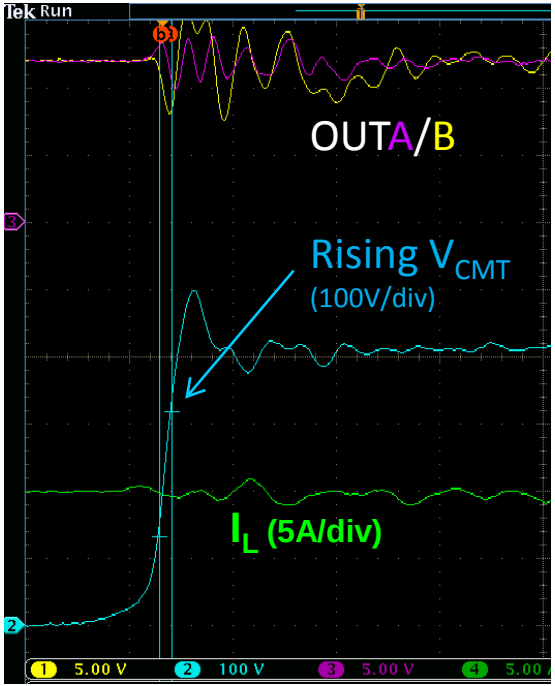
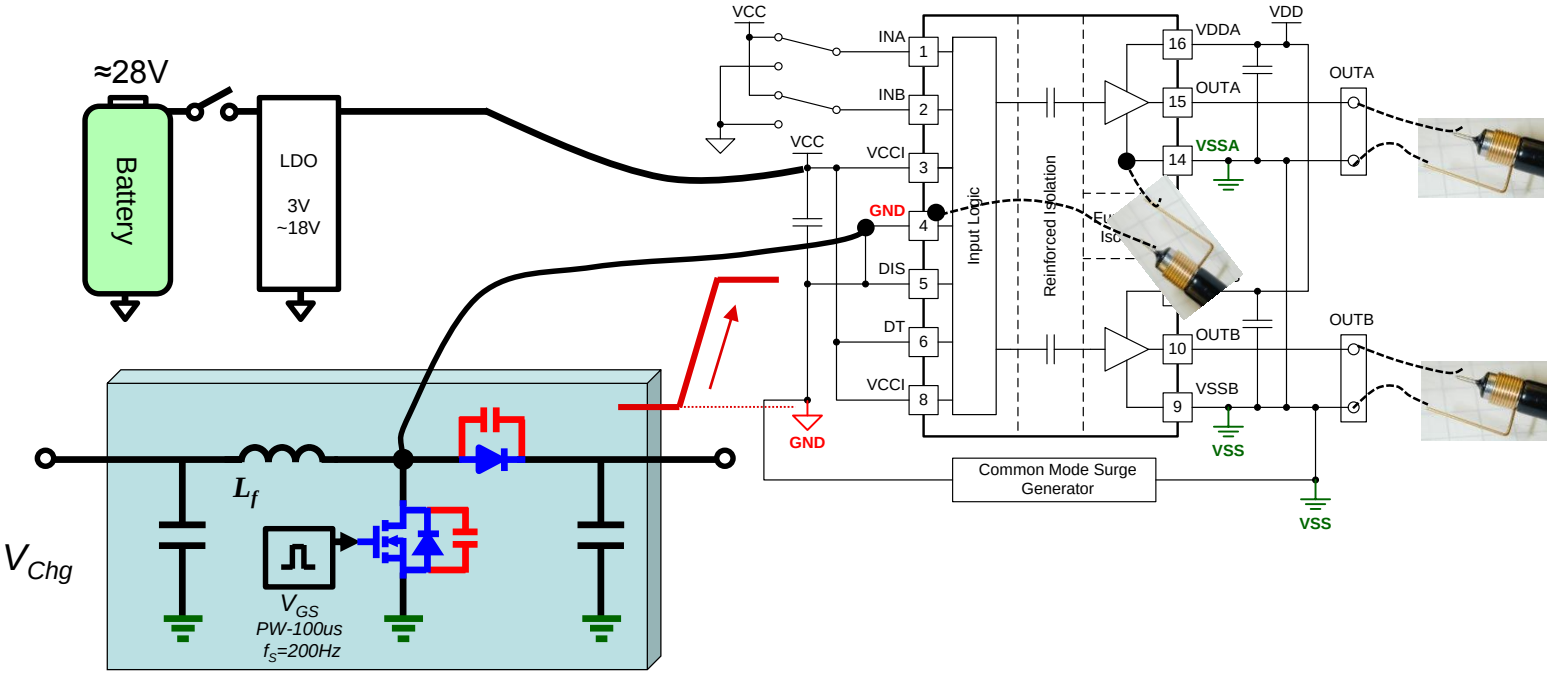
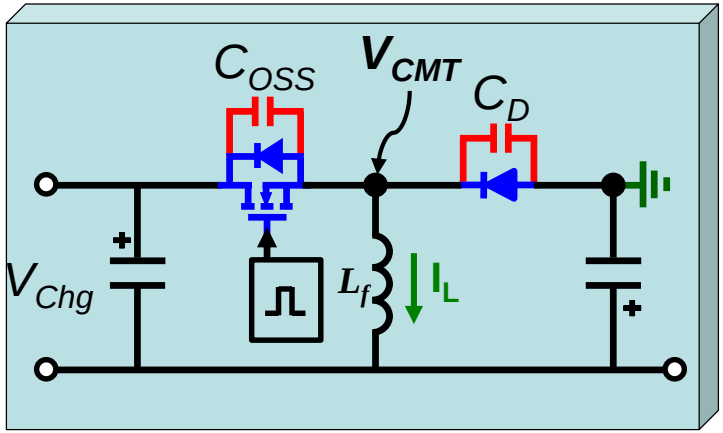


System Configuration for Rising Slew Rate

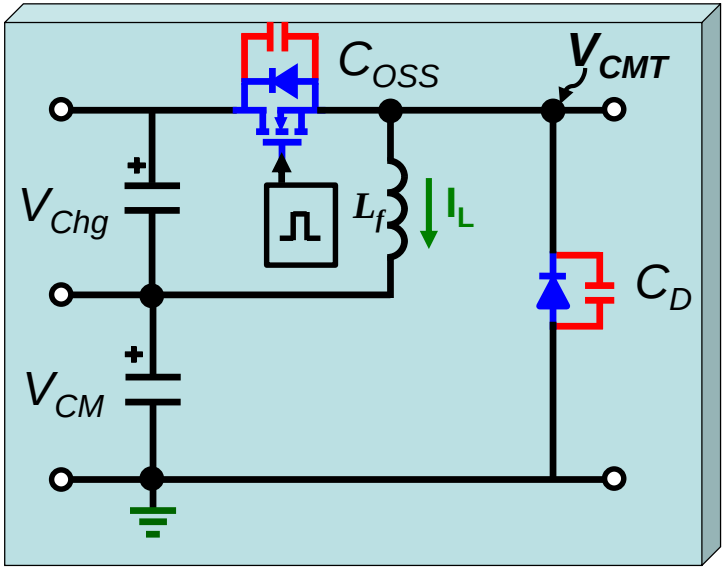


Passive Probe BW=1GHz

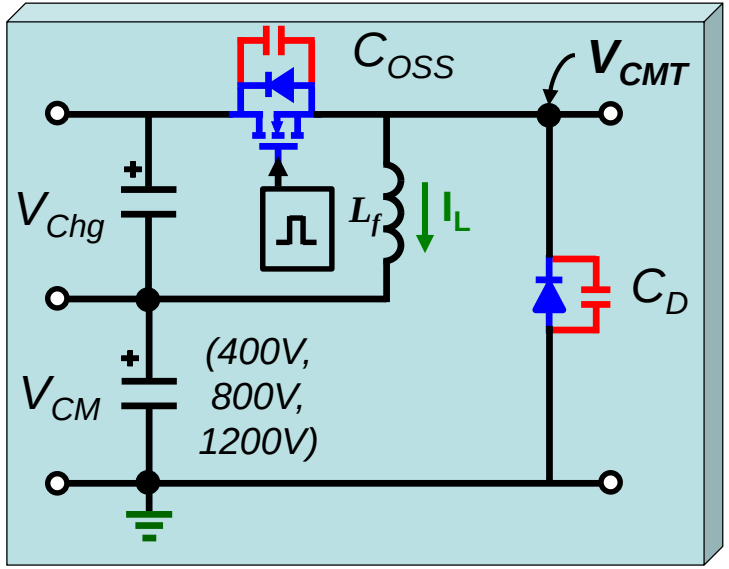
How to Generate Programmable CMTI Falling Slew Rate?



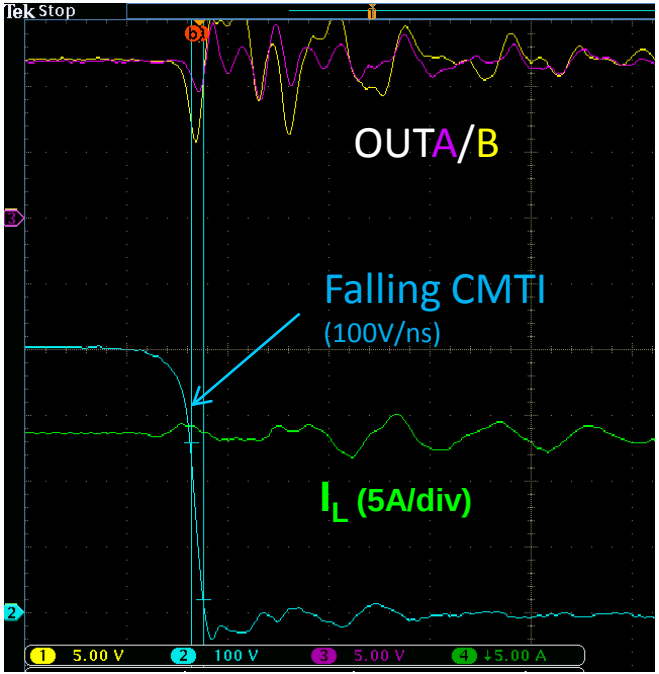
V_{CM}
(400V, 800V, 1200V)



How to Generate Programmable CMTI Falling Slew Rate?

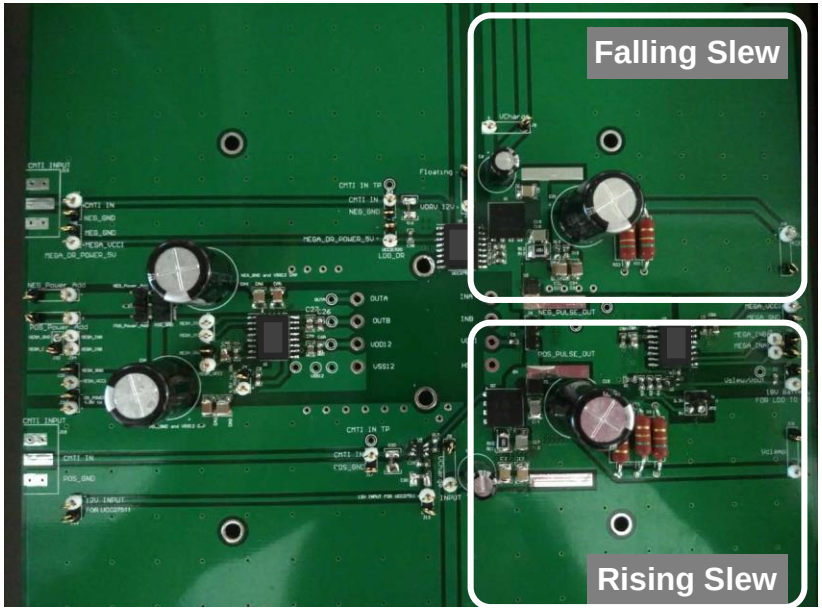


$$\frac{dV}{dt} \propto V_{Chg}\Big|_{T_{on},\, L_f = Const.}$$

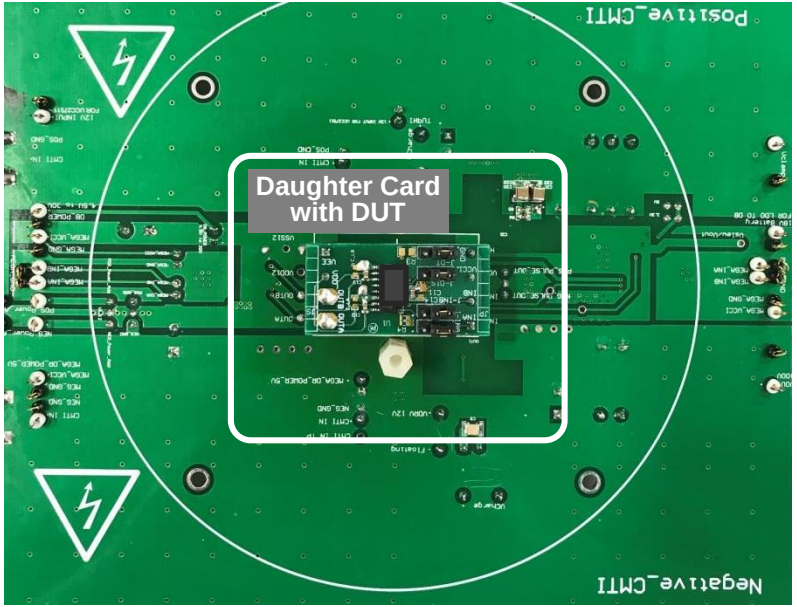


CMTI PCB Design

Bottom Layer



Top Layer

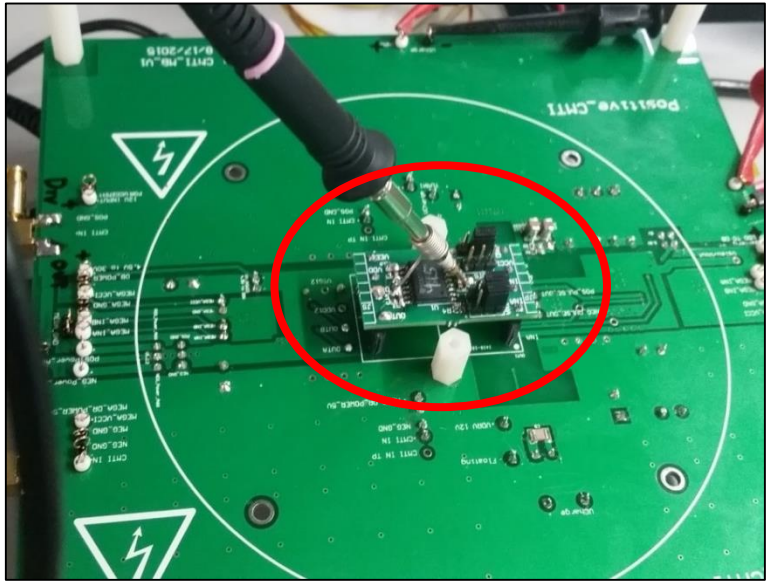


CMTI Hardware Design and Measurement Considerations

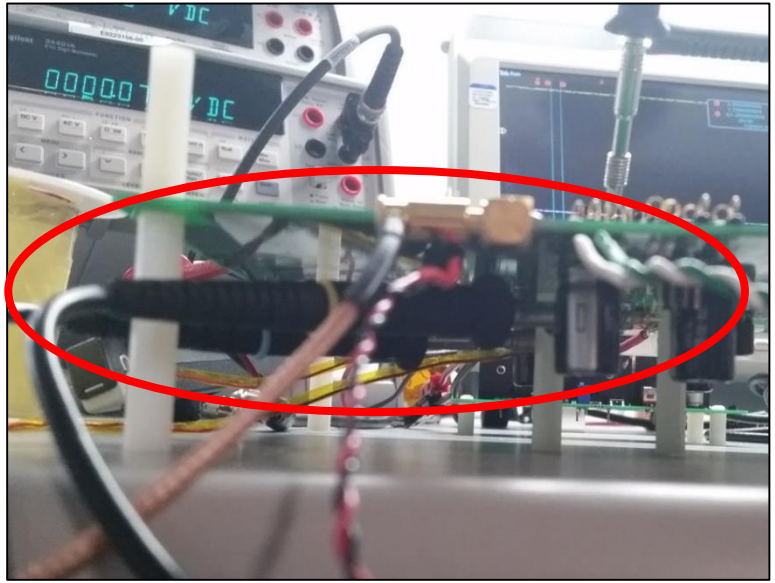
- MOSFET, SiC-MOSFET, or GaN with small C_{OSS};
- SiC Diode with small C_D;
- Air core inductor with small parasitic winding capacitance;
- Minimization of two separate ground capacitive coupling;
- Use floating battery to drive the high side switch for falling slew CMTI, instead of isolated power supply
- **Characterization on measurement location and DUT**

CMTI Measurement Location

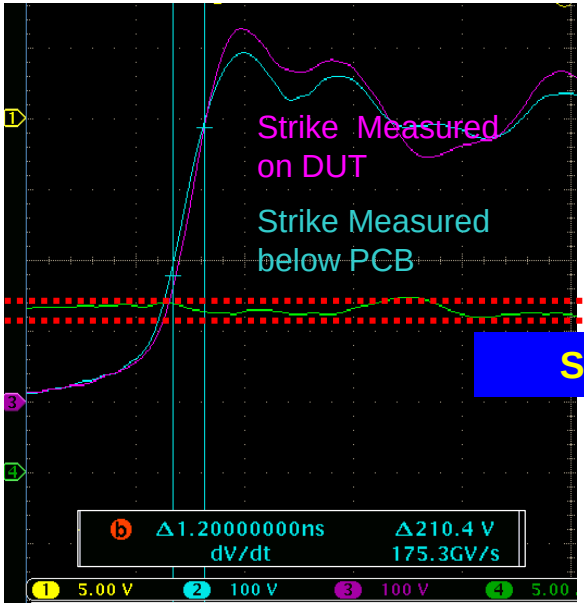
Right Next to DUT



Under PCB due to Thermal Stream

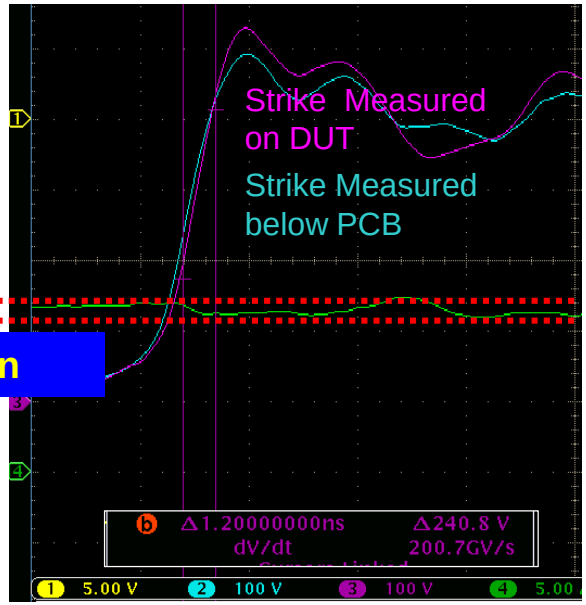


CMTI Test Setup Characterization



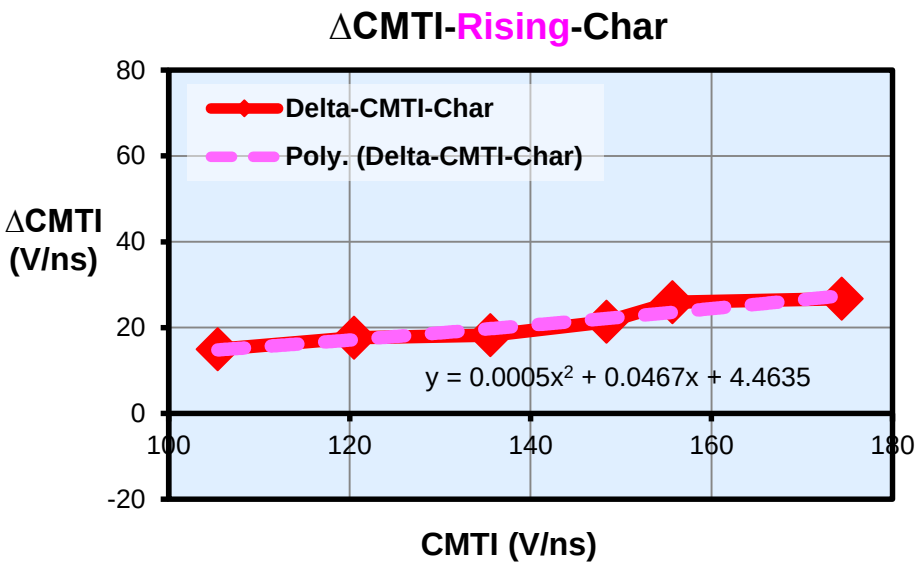
175V/ns

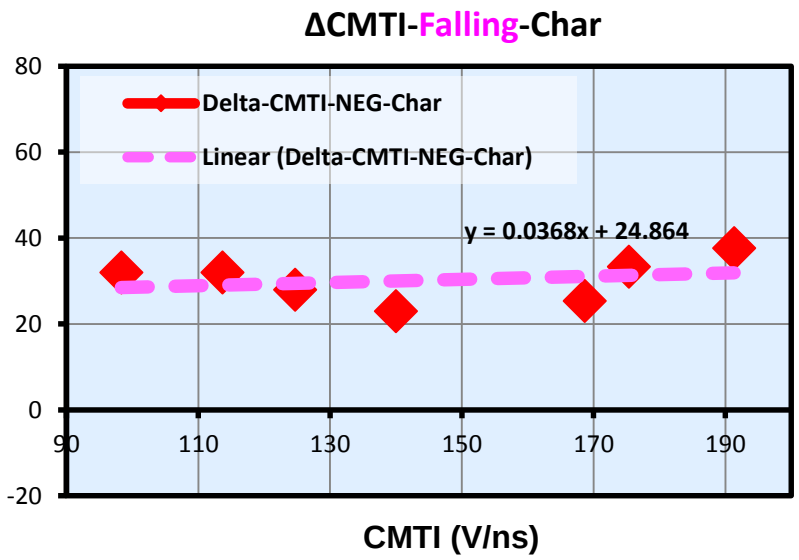
Same Test Condition



201V/ns

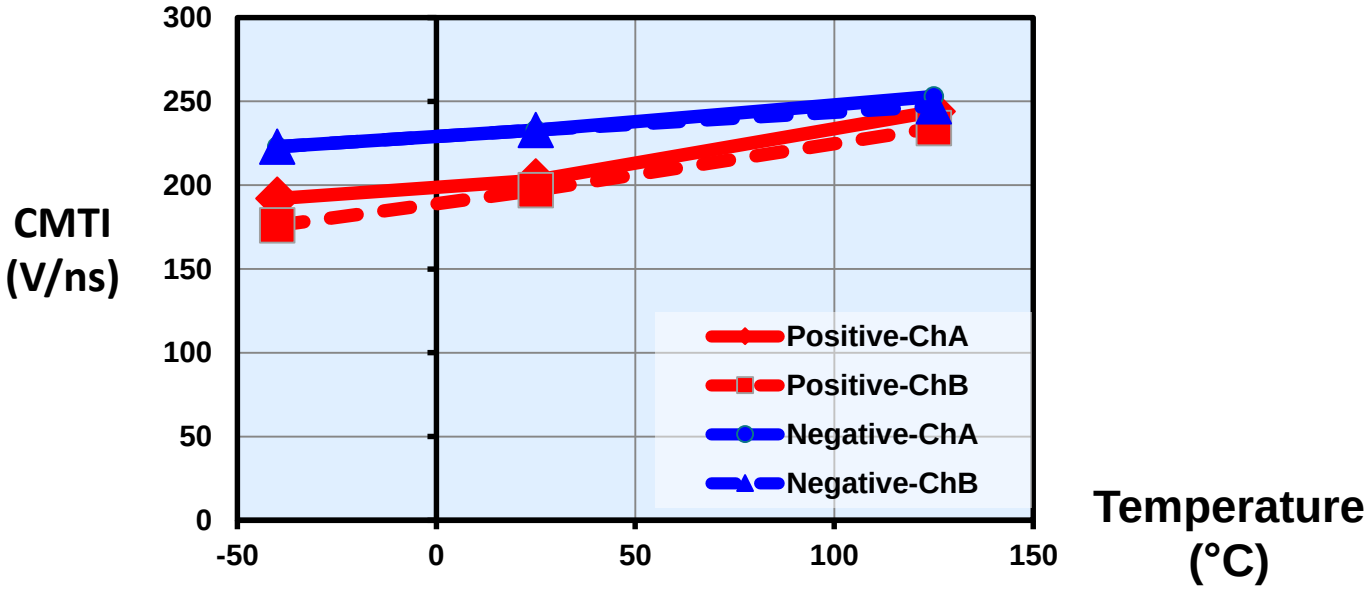
CMTI Test Setup Characterization





CMTI Measurement Data for UCC21520

- VCCI=12V, VDD=25V



Summary

- Isolation in gate driver
- Deep dive of common mode transient immunity (CMTI)
- Bench CMTI design, measurement and design considerations

THANK YOU