Gate Driver Timing Specification Requirements for WBG Devices

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Agenda

► Wide Bandgap Devices and Their Implications

► The Ideal “Gate Driver”

► Key Timing Metrics and Why They Matter
Wide Bandgap Devices

- Wide bandgap devices are named due to much higher bandgaps than traditional silicon.
- Above 4 eV is (usually) considered an insulator.

<table>
<thead>
<tr>
<th>Material</th>
<th>Bandgap Energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>1.1</td>
</tr>
<tr>
<td>Silicon Carbide</td>
<td>3.3</td>
</tr>
<tr>
<td>Gallium Nitride</td>
<td>3.4</td>
</tr>
</tbody>
</table>

[1] DOE 2013
Wide Bandgap Devices - Benefits

► Higher voltage blocking for lower on resistance
  ▪ Allows for a more efficient on state
    ▪ Lower conduction losses

► Faster switching edges
  ▪ Allows for smaller “IV triangle”
    ▪ Lower hard switching losses even at same switching frequencies

► Allows for faster frequencies
  ▪ Smaller passive components

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**Frequency Capability**

- Si IGBT
- Si MOSFET
- SiC MOSFET
- GaN MOSFET
Play Spaces

GaN exhibits a “diode like” action when reverse biased \cite{4}.

- “Diode drop” voltage is large (3-4 V).
- Voltage drop is present during hard switched deadtimes:
  - Leads to significant power loss.
- Significant even at higher bus voltages:
  - Due to efficiency targets.

\[ V_{bus} \]

\[ V_{ds} \]

\[ \text{Deadtime} \]

\[ \text{reverse bias} \]
The “Ideal” Gate Driver

- No timing disparity
- Level shifts control signal to power switch levels
- “Robust”
- (Example ignores EMI)
“Ideal” Gate Drivers in a Half-bridge

- No timing disparity
- Level shifts control signal to power switch levels
- Provides level translation

![Diagram of Ideal Gate Drivers in a Half-bridge](image-url)
Effect of Timing Mismatch

- **Single Switch Topologies:**
  - Open loop values could be off
  - Closed loop largely compensated out

- **Half-bridge legs:**
  - If both switches are off, efficiency could suffer
  - If both switches are on, shoot-through occurs
    - Could be catastrophic!
Key Timing Metrics

► Forward Path Metrics
  ▪ Propagation Delay
  ▪ Jitter
  ▪ Rise/Fall Time
  ▪ Pulse Width Distortion
  ▪ Propagation Delay Skew

► Protection Timing Metrics
  ▪ Reaction to overcurrent
Propagation Delay

- Delay from input to output of gate driver
- Must be much lower than controller bandwidth
- Theoretically can be compensated in controller
- Propagation delay, in itself, does not cause shoot-through
  - This assumes both channels have EXACTLY the same propagation delay

- Can be defined 50% to 50% or VIH/L to 10/90%
Jitter

- Cycle to cycle reproducibility of propagation delay on a single part, at one operating point
- Jitter metrics are folded into the min/max propagation delay, PWD, and skew
- Can produce small ripple on converter outputs, but jitter is usually small and can be ignored
Rise/Fall Time

- Rise and Fall time are gate drive strength metrics
- SiC and GaN has lower gate charges for comparable Si devices
- Rise and Fall times can be tuned by gate resistors in most drivers
Pulse Width Distortion

- Difference between rising and falling delays, usually on a single part
  - Causes duty cycle change
  - Can be dealt with in controller in most cases
Propagation Delay Skew

- Very important, but often ignored
- Difference between edges of two different channels reacting to the same input and operating conditions.
- Defined as per part (multiple channel), or part-to-part
- Skew is always smaller than total bounds of min/max propagation delay
Goal
- No shoot-through
- Shortest deadtime possible

- It is tempting to set deadtime based on min/max prop delay across all conditions
  - This is leaving performance unused

- Skew allows a much tighter deadtime to be set
  - Great advantage for GaN (reverse diode action)

- Pulse width distortion is NOT the same thing as skew
  - Setting deadtime based on PWD alone can lead to shoot-through
Short Circuit Withstand Times

► Typical short circuit withstand times for Si MOSFETs and IGBTs are typically specified at 10 µs.

► SiC MOSFET short circuit withstand times have been reported as low as 4 µs \[^5\]

► GaN normally off short circuit withstand times have been reported as low as 1.8 µs \[^5\]

\[^5\] Badawi et al. 2016
GaN and SiC promise great advantages to Si MOSFETs and IGBTs

GaN reverse diode characteristic necessitates shorter deadtimes

This drives “tighter” timing specs, not necessarily “faster” timing specs
- Propagation delay skew is the unsung hero, and sometimes isn’t even specified in datasheets

GaN and SiC shorter short circuit withstand times demand faster protection speeds
References


Thank you