PACKAGE AND PLATFORM VIEW OF INTEL’S FULLY INTEGRATED VOLTAGE REGULATORS (FIVR)

Edward (Ted) Burton
Ivy Bridge Platform

- Core VR: 0V-1.2V
- I/O VR: 1.0V
- Graphics VR: 0V-1.2V
- System agent VR
- DDR VR

Haswell Platform

- PLL VR: 1.8V
- Vcc_In VR: 0V-1.8V
- DDR VR

Haswell Processor

FIVR VRs:
- System
- I/O
- Analog
- Core 0
- Core 1
- Core 2
- Core 3
- Cache
- Graphics0
- Graphics1
- EDRAM
- OPIO

Logic
FIVR At a Glance

• 140MHz switching frequency
• Up to 16 phases per VR
• Up to 80MHz unity gain
• Non-magnetic package trace inductors
• MIM caps
• Silicon current density of 31 Amps/mm²
• Typical efficiency of 90% in turbo
FIVR Value Proposition

• Platform footprint, cost & thickness reduction
  – Smaller XYZ ➞ more features, thinner handhelds

• Platform power component cost reduction, while doubling graphics, adding EDRAM, doubling vector hardware…

• Battery life improvement
  – Reports of over 50% increase vs prior generation

• Graphics power-perf improvement
  – Tens of % improvement in constrained form-factors
Volume Scales ~1/Frequency

One 30A VR phase, prior generation Ultrabook
300kHz Switcher
800mm$^2$

CPU and PCH chips plus 7 multi-phase FIVRs
140MHz Switchers
495mm$^2$

466x Frequency
111x area shrink
~4x thickness shrink
FIVR Photo - Package Underside
FIVR Cutaway View

Package Trace
Inductors

Power FETs
and Control
XRAY View – FIVR Inductors
Future Scaling Issue & Solution

Don Gardner - Intel Corp on-die magnetic inductors
Typical Package Cap vs MIM

- Reverse geometry 0204 1uF cap impedance curve
- Package cap inductance raises HF Z (70 milliohm @140MHz)
- Needs high frequency parallel die capacitance
- No inductance for uniformly distributed MIM capacitor & uniformly distributed load, so no high frequency increase in Z
- Nonuniform loads get “complicated”
- Real loads and real phases are nonuniform
Real Behavior “Complicated”

Ripple Voltage (X,Y,time)
FIVR ➔ Thinner Handhelds

Ivy Bridge
Backside all power

Big inductors, butterfly mounted through board

Haswell
Backside bare

Small inductors & caps & 75% fewer

2mm thinner – cheaper - 10% larger battery
FIVR ➔ More Platform Features

Ivy Bridge
- SATA
- Analog audio
- IR remote
- One USB3.0
- Two USB2.0
- LAN or Thunderbolt

Haswell
- SATA
- Analog audio
- IR remote
- Four USB3.0
- LAN and Thunderbolt
- 2x graphics
- Free space to add more features
- ~$5 Saved in power BOM

Intel NUC Platform
High UGB, Fast Transitions
A Fringe benefit of miniaturization

<table>
<thead>
<tr>
<th></th>
<th>Typical prior generation VR</th>
<th>FIVR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unity Gain Bandwidth</td>
<td>( \leq 80kHz )</td>
<td>( \leq 80MHz )</td>
</tr>
<tr>
<td>Core and Graphics voltage max transition times</td>
<td>100’s of microseconds</td>
<td>100’s of nanoseconds</td>
</tr>
</tbody>
</table>
# Power States – 2.6-122x Lower

<table>
<thead>
<tr>
<th>Package State</th>
<th>Actions taken in various Package States</th>
<th>Ivy Bridge CPU power (W)</th>
<th>Haswell CPU power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0</td>
<td>Cores, Graphics active</td>
<td>17 W (TDP)</td>
<td>15 W (TDP)</td>
</tr>
<tr>
<td>C6</td>
<td>Core’s and Graphics FIVRs off. DDR in self refresh</td>
<td>2.3</td>
<td>0.9 1/2.6</td>
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<tr>
<td>C7</td>
<td>System agent &amp; DDR IO gated off. CPU critical arrays on Sustain Rail.</td>
<td>2.2</td>
<td>0.85 1/2.6</td>
</tr>
<tr>
<td>C8</td>
<td>Display &amp; IO FIVRs off. LLC flushed System Agent gated off. Vin = 1.2V.</td>
<td>N/A</td>
<td>0.077 1/29</td>
</tr>
<tr>
<td>C9</td>
<td>Vin set to 0V</td>
<td>N/A</td>
<td>0.018 1/122</td>
</tr>
<tr>
<td>C10</td>
<td>Platform power target of 100mW or better.</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>
Small platform example:

- Old platform rails 1phase each:
  - Graphics: 30A inductor @ ~1V ➞ ~30W max
  - Cores: 30A inductor @ ~1.1V ➞ ~33W max

- FIVR platform’s input rail:
  - 2 30A inductors @ 1.7V ➞ 102W max (shared dynamically)
  - Core-only workloads: Triple the available turbo power
  - Graphics workloads: Double the available turbo power for graphics

More Turbo Power Headroom ➞ More Performance

- Higher burst frequency
- Larger graphics
- More cores
Graphics - 95% Lower Effective Z

Magnitude Z (Ohms)

- IVB B0 GT
- HSW A0 GT0 (Loc Mai)
- HSW 2 GT Rails Parallel Impedance

Frequency (MHz)

Negligible Stimulus

ATD Power Delivery
Graphics Power Reduction (Typical Example)

Same Part, Same Application, Same Freq, & Same minimum Vcc

Lower power

200mV (20%)

Mostly high Voltage ➔ V^2 power tax

FIVR

Graphics Vcc DCR mode
Graphics Speedup (Cut/Pasted Prior Example)

Could match max-Vcc (process-limited) for ~20% more speed
Lower Power, Higher Speed

Graphics Frequency

Graphics Power

Non-FIVR

FIVR

Less power

More speed

Vmax &/OR I_max exceeded

Summary

• 140MHz switching enables integrated output filters
  ➔ On-die MIM capacitors; package trace inductors
  ➔ Thinner platforms, with more features
  ➔ Reduced power component cost, while doubling graphics and core vector hardware and adding EDRAM

• Battery Increased life by upwards of 50% on many platforms
  • Quickly ramped input and output rails to support new sleep states
  • Set every rail to its optimal voltage

• Improved graphics power-perf 10’s of %
Supporting Slides
90% Efficiency at Full Vout

![Graph showing efficiency at different load currents for various numbers of phases. The graph indicates that the efficiency remains above 90% across a wide range of load currents, with the composite line showing the highest overall efficiency.](image-url)