Significant Developments and Trends in 3D Packaging with Focus on Embedded Substrate Technologies

Presented by PSMA Packaging Committee Brian Narveson and Ernie Parker, Co-Chairmen



Technology Report Commissioned

- Why: Phase 1 Technology Report on 3D Power Packaging determined the power industry was interested in and beginning to manufacture Embedded Substrate power products
- Methodology: Ltec Corporation commissioned to create Technology Report:
 - Researched 740 published articles from industry, government and academia
 - Interviewed 30 Industry and Academic Experts
 - Attended 10 trade shows, conferences and seminars
- Purpose: To determine the availability of imbedded substrate technology usable by the Power Industry





What is 3D Power Packaging

- Power supply products derived from the use of the z axis
- Incorporation of a variety of technologies to reduce footprint
- Solutions that increase power density (W/cm³)
- Manufacturing solutions that can print or construct interconnects or circuit layers



What is Embedded Substrate Technology

- A 3D Embedded Power Module is a "systems that use a combination of at least one controller/driver IC, at least one active component in the power train, and associated interconnect means, embedded in a single package."
- Component embedding is "the inclusion of at least one active or passive electrical component within the top and bottom conductive layers of a substrate."
- A *substrate* is defined for this study as "a planar structure having multiple conductive and insulating layers."





Embedded Power Market Drivers

- Digital functionality and power consumption increasing at a rate of "More than Moore"
 - CMOS has hit the wall, transistor efficiency is not increasing, and processor clock speeds are stagnating.
 - Advanced deep submicron semiconductor technology has hit a cost barrier
 - Barrier overcome with a paradigm shift in digital semiconductor packaging
 - Leading technologies are wafer thinning, through-silicon vias (TSV) and 2.5D and 3D integration
 - Power requirements increasing 2 to 5 times, within the same footprint, in one generation
- Power density and efficiency improvement with wide gallium-nitride (GaN), silicon-carbide (SiC), and gallium-arsenic (GaAs) are facing a "construction barrier"
 - Optimum performance can only be achieved with packaging free of bond wires
 - Embedded substrate technology is a disruptive technology that can lead to large increases in power density and efficiency



Why is Embedded 3D Packaging Important

• What you told us: Motivation for using embedded packaging.



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% of Available Score

At what Power Levels are you Interested in Embedded 3D Packaging

• What you told us:



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Technology Areas Studied

- PCB's and Inorganic Substrates
- High Temperature Die Attach, High-lead Solder Substitution
- Passives
 - -Resistors
 - -Capacitors
 - -Magnetics
- Interposers
- Packaging Technologies
- Thermal Management
- Additive Manufacturing
- The report is 10 Chapters, 336 pages, with 394 Publications cited and 172 links provided

Benefits of Embedded Substrate Technology

- Performance
- Reliability
- Ease of use
- Solution size
- Thermal management
- EMI shielding
- Reduced need for product-specific tooling
- Reduced need for additional packaging
- Fast time to market
- Cost?



Standards for Embedded Substrate Technology

- Substrates and Components
 - IPC-2316: Design Guide for Embedded Passive Device Printed Boards
 - IPC-4811: Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards
 - IPC-4821: Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards.
 - IPC-4101: Specification for Base Materials for Rigid and Multilayer Printed Boards
 - IPC-6012: Qualification and Performance Specification for Rigid Printed Boards
 - IPC-7092: Design and Assembly Process Implementation for Embedded Components (being written)
 - JCPA EB01-2013: Parts Built-in Electronic Circuit Board (Component Built-in Board) Data Format Design Guide – 2nd Edition

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 JPCA – EB02-2013: Standard on Device Embedded Substrate Terminology / Reliability / Test / Design Guide 4th Edition

Examples of Embedded Technology



AT&S Embedded Component Packaging (ECP[™]) Process Flow



GaN devices of GaN Systems Inc. embedded in AT&S (ECP[™]) process



TDK SESUB Process



General Electric's Power Overlay Technology

| IGBT DIODE DRIVER | | | | |
|--------------------|---|---|---|---|
| | ePOL | WPOL | POL-MCM | POL-kW |
| DESCRIPTION | Low-cost embedded package leveraging high volume PCB technologies | Fanout WLP using GE POL and component packaging technologies | MCM SIP & integrated passive SMT or leaded conectors with integrated DBC for thermals | Ultra high power module with leaded connectors and advanced thermal management |
| FEATURES, BENEFITS | Low I/O <300 single and SIP applications, with min. L/S 25/25um, 30+ Volt | Low to medium I/O, 400 single & MCM applications with min. L/S 10/10um 30+ Volt - Large sized POL frame processing, enabling excellent routing capability - Ultra thin, low | Medium Voltage ,1200V - Multiple pwr devices and ICs (10+) - Multiple passives (30+) - Low parasitics - Heterogeneous die integration combining both power and logic | Higher power 1200V+ - Lowest possible parasitics fast switching, low losses - Double sided cooling, superior thermal management |
| APPLICATIONS | Mobile, computing, telecom - Wireless - RF FEM - Power management | Mobile, computing, telecom - Wireless - RF FEM - power management | Computing, telecom, industrial - DC-DC converter - Intelligent power modules | Automotive, aerospace, - Motor drives - Renewables - High power conversion |



Infineon's DrBlade[™] 2 Package



Schweizer's P²-PAK approach





Semikron's Sintered SKiN™ PROCESS



Shinko Electric's Molded Core Embedded Package (MceP[®])



Embedded Components



Component Types and Processes



Challenges

- Electrical Test
- Yield
- Who owns the failure
- How do share the losses





- The digital world is going 3D to increase capability in the same footprint
- Digital 3D will greatly increase the need for power but not increase the available space to implement it
- Embedded Substrate technology is a viable path to increase power density
- Multiple substrate and semiconductor technologies are available at many power levels
- Both formed and inserted components are available from multiple suppliers
- Multiple power manufactures are shipping product utilizing embedded technology
- Less than 5% of the material in the report has been presented. Contact PSMA to find out how to get a copy.

Next Step?: Phase 3

- The Epilog of the Phase 2 report and recommendations in section 6.5.2 of the Phase 1 report recommend the "commissioning an embedded PSU demonstration project"
- The PSMA Packaging committee will be evaluating the feasibility of such a project over the next few months
- Please contact Brian Narveson or Ernie Parker the committee Cochairs if you are interested in participating



Proposed Schematic diagram of the demonstration Power SiP's



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Thank You

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