



12V PowerStage in Embedded Die System-in-Package

Greg J. Miller
Sr. VP – Engineering
Sarda Technologies, Inc.
gmillier@sardatech.com

Agenda

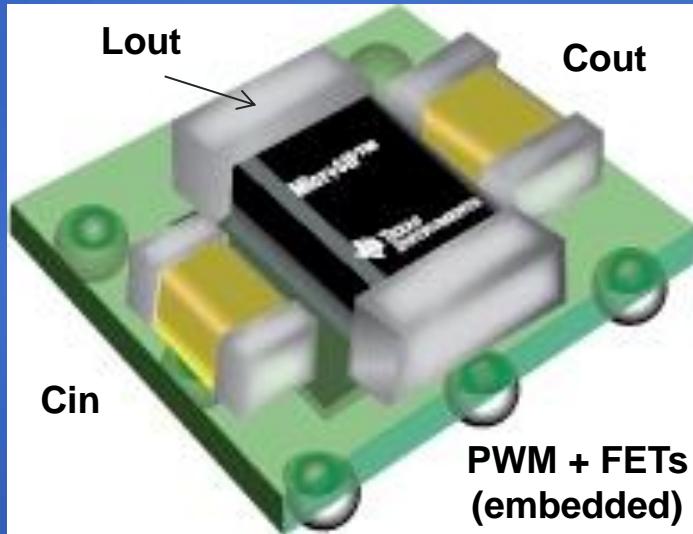
- **Introduction: 3D Power Packaging**
- **State-of-the-Art 12V input POL Solutions**
- **What if you need a higher power density solution?**
 - GaAs – an enabling high frequency FET
 - Multiphase – to shrink size of inductor
 - Integration – a requirement for multi-MHz switching
- **Embedded Die System-in-Package approach**
- **Summary**

3D Power Packaging is a Game Changer

using Embedded Die in Substrate Technology

In Production today

One Example: TI's MicroSIP™ Modules



Nice compact solution

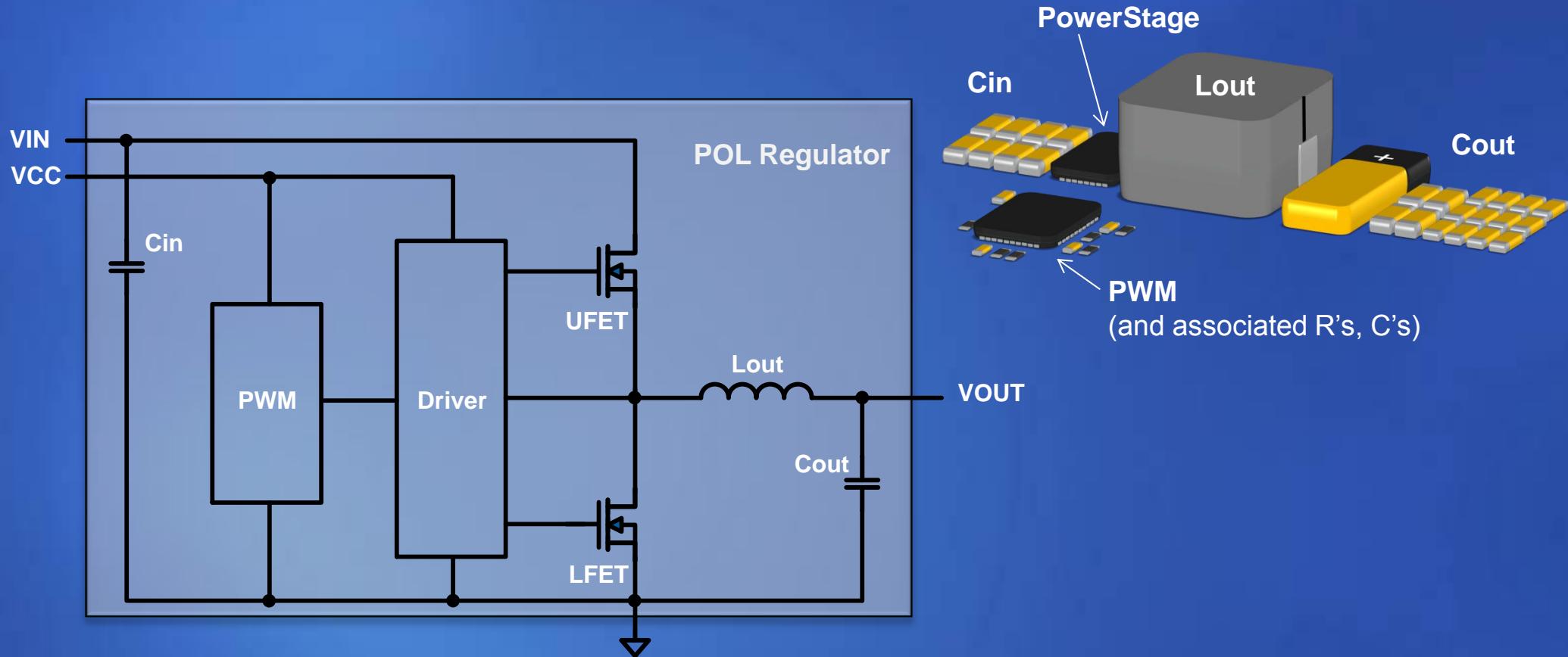
Low Input Voltage: 5V max

Low Output Current: ~2A max

*But what about higher voltages
and higher currents?*

*Does Embedded Die in Substrate
Technology add value there?*

12V Input Buck POL Regulator

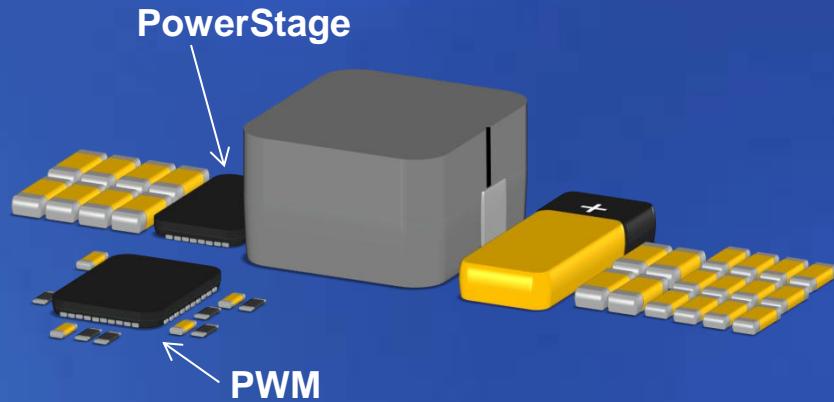
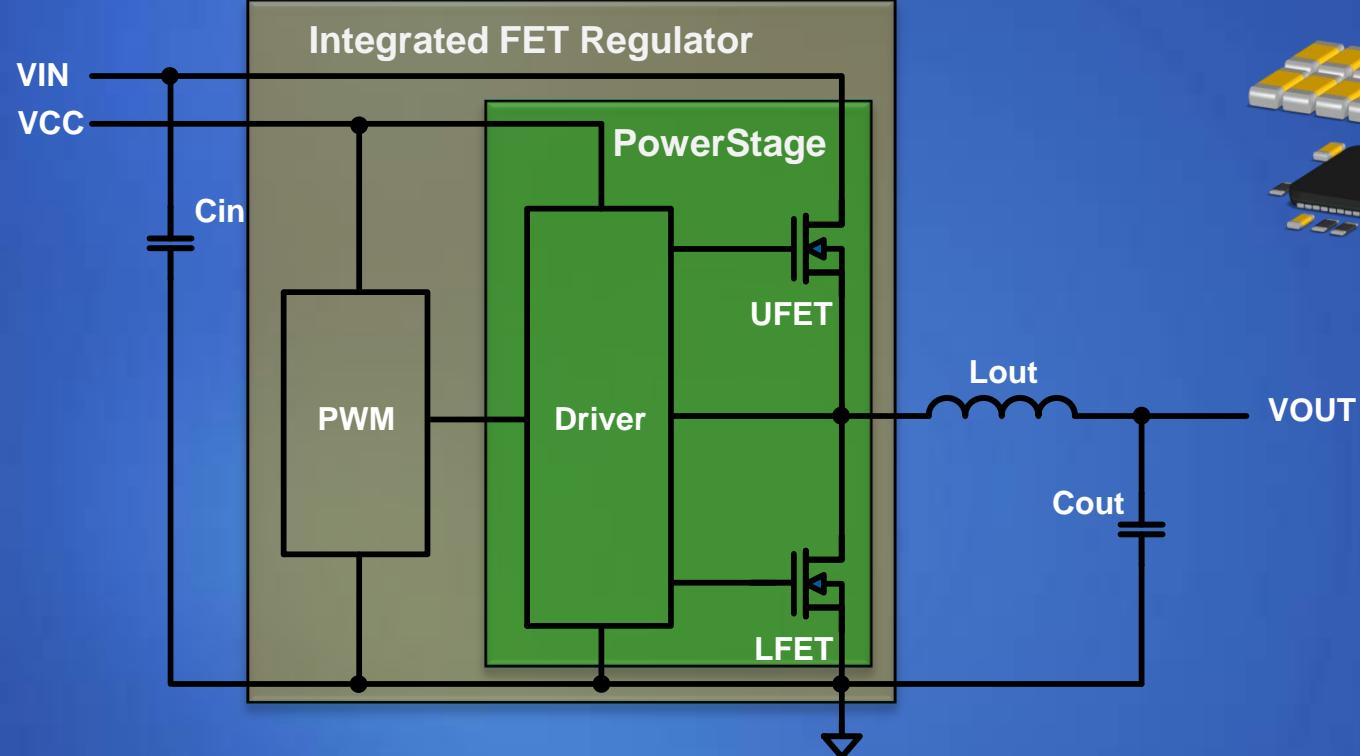


*Can Embedded Die in Substrate Technology add value in
12V input, high Output Current applications?*

*Answer: An emphatic Yes **

* In conjunction with Compound Semiconductor FETs, namely GaAs

Common Integration Approaches



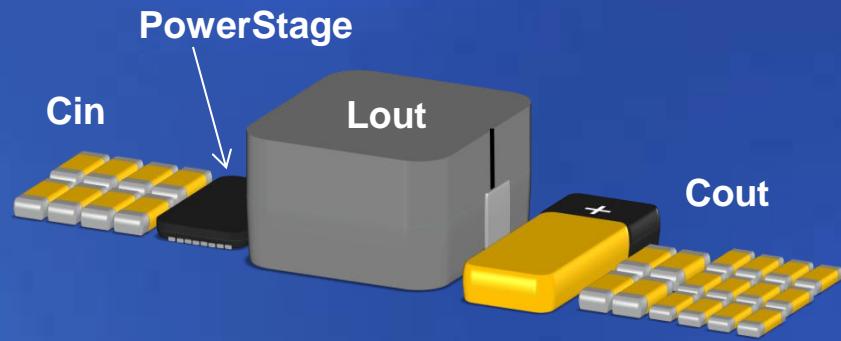
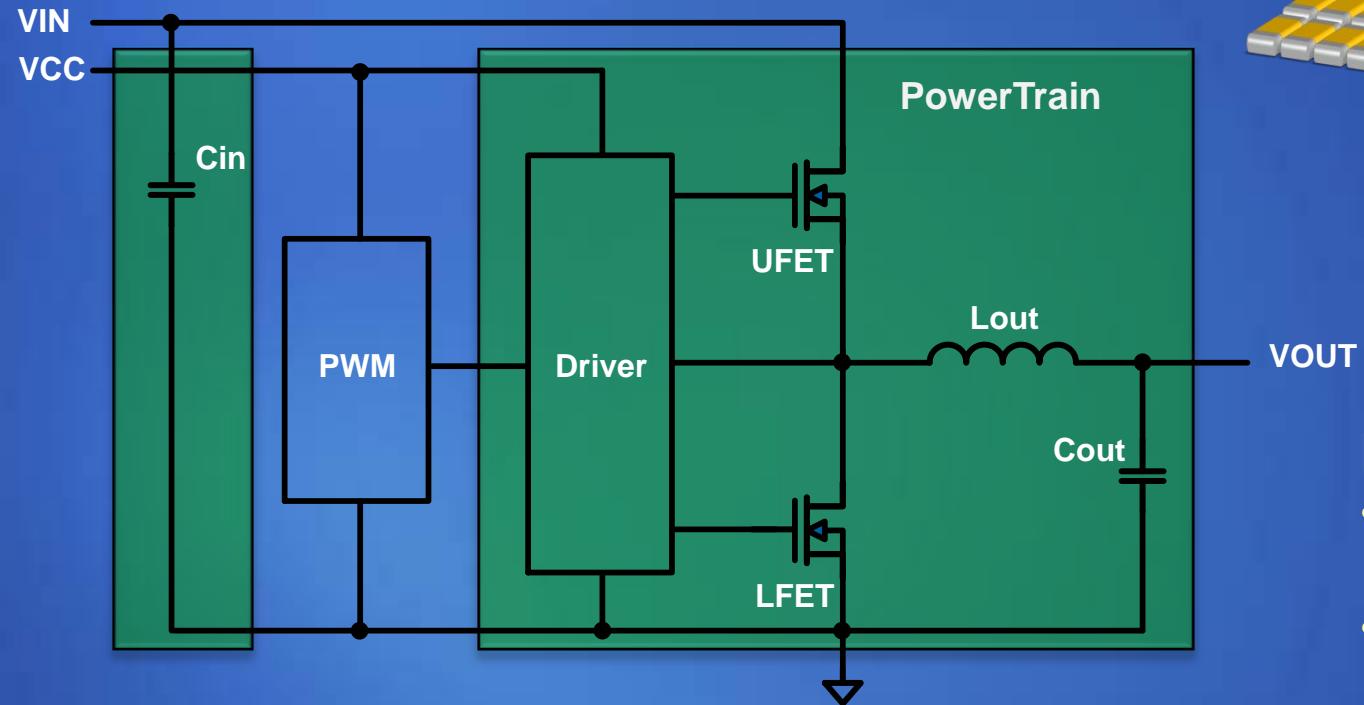
PowerStage

- Driver + FETs
- Typically multi-chip for high current applications ($>10A$)

Integrated FET Regulator

- PWM + Driver + FETs
- Typically monolithic for low current applications ($<10A$)
- Very common for low V_{in} ($<5V$)

For Benchmarking Purposes – Examine PowerTrain

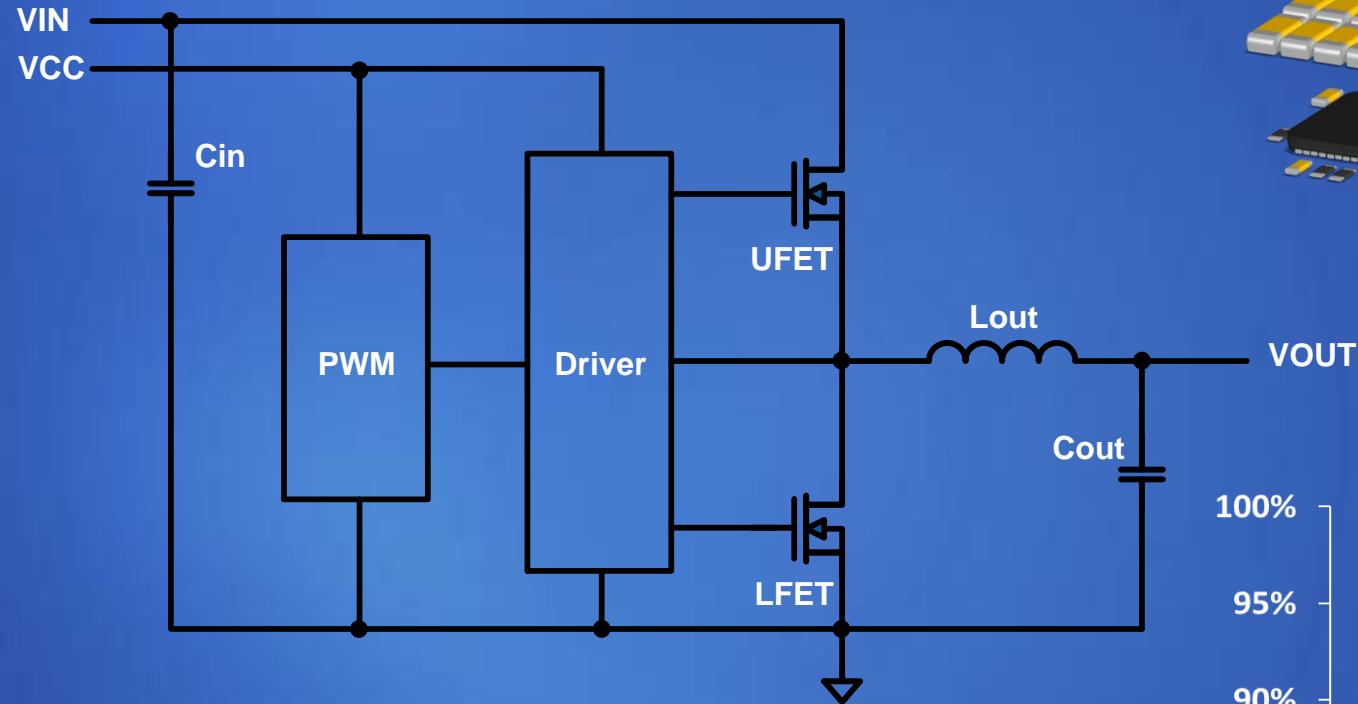


PowerTrain

- PowerStage + Output Filter + Input Cap
- Determines efficiency and majority of POL size

State-of-Art 12V input Buck POL Solution

30A output current example



Low Rdson MOSFETs

- 1mΩ LFET

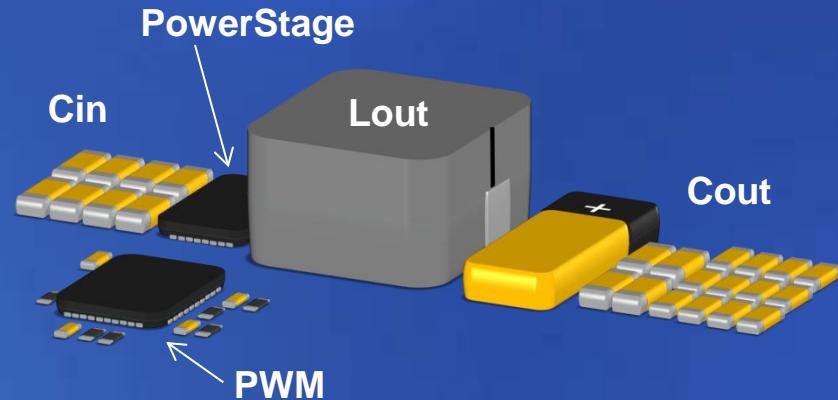
Low DCR Inductor

- 0.2mΩ

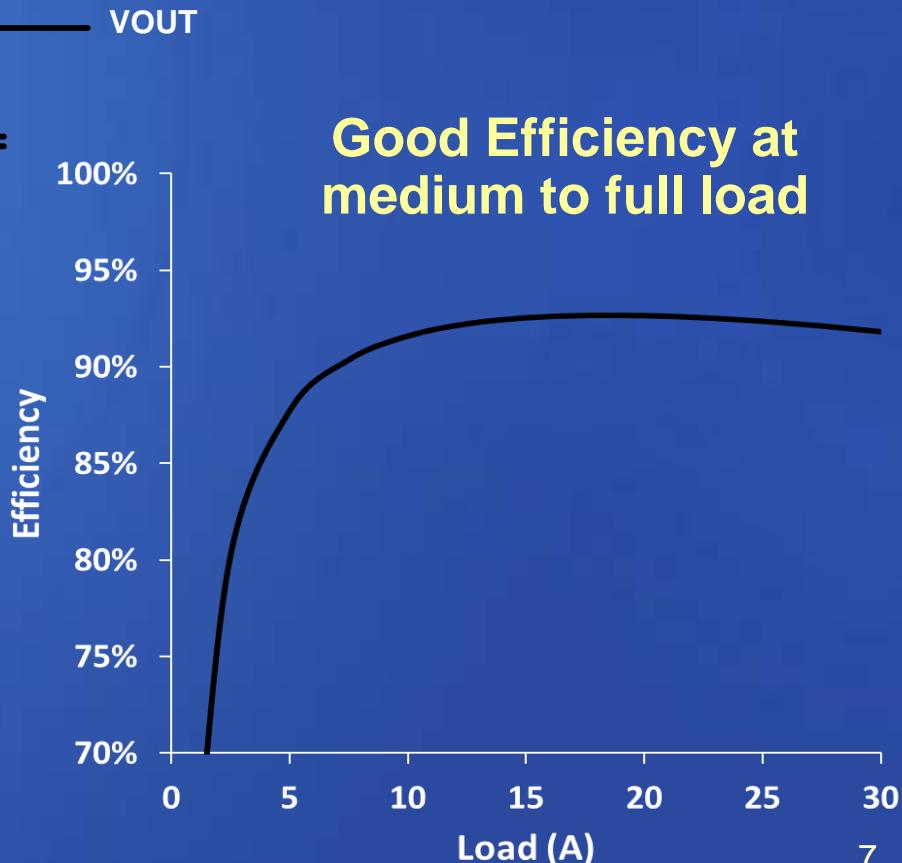
Low Switching Frequency

- 500-700kHz

Bulky – but if you have the room for these solutions, by all means use them



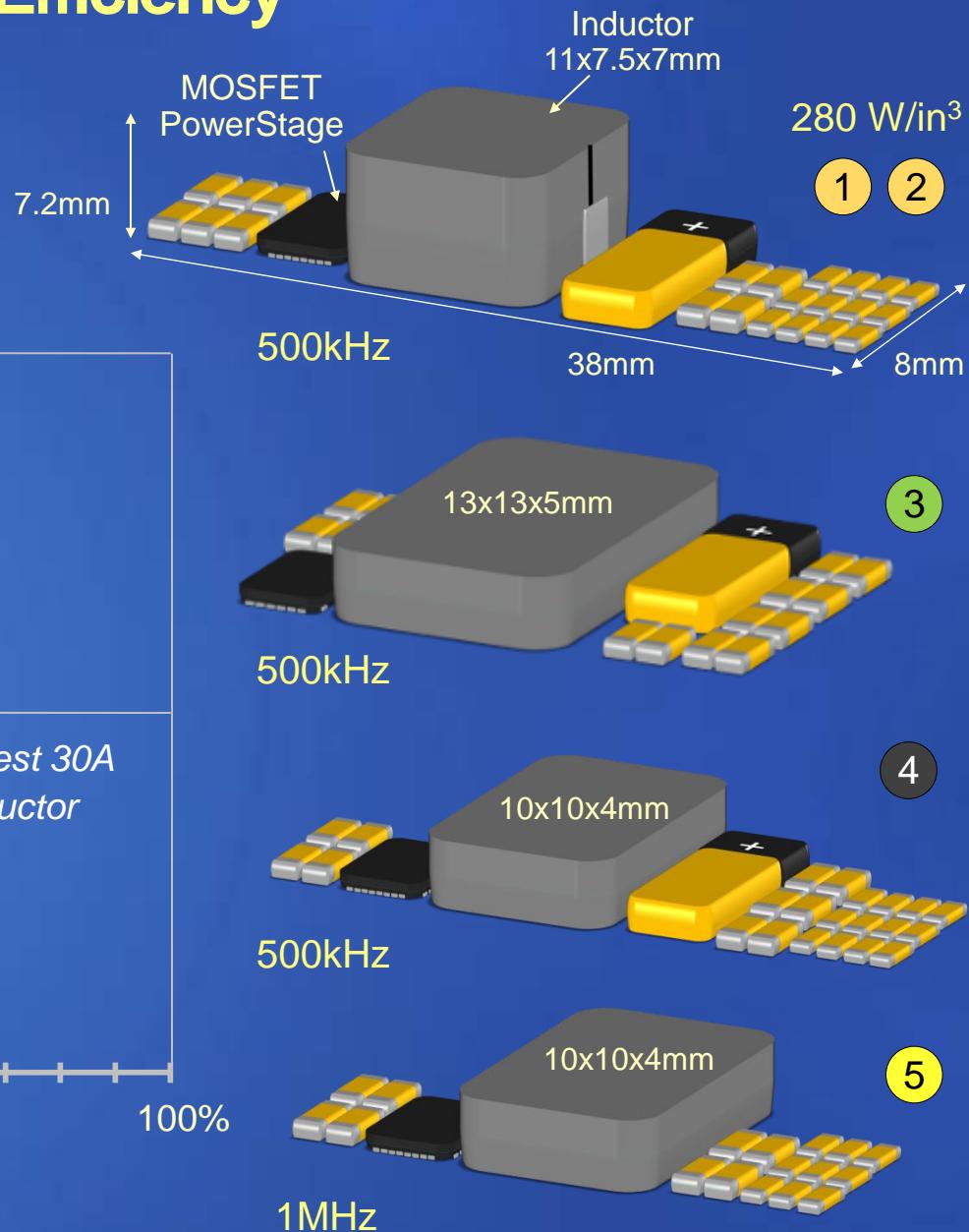
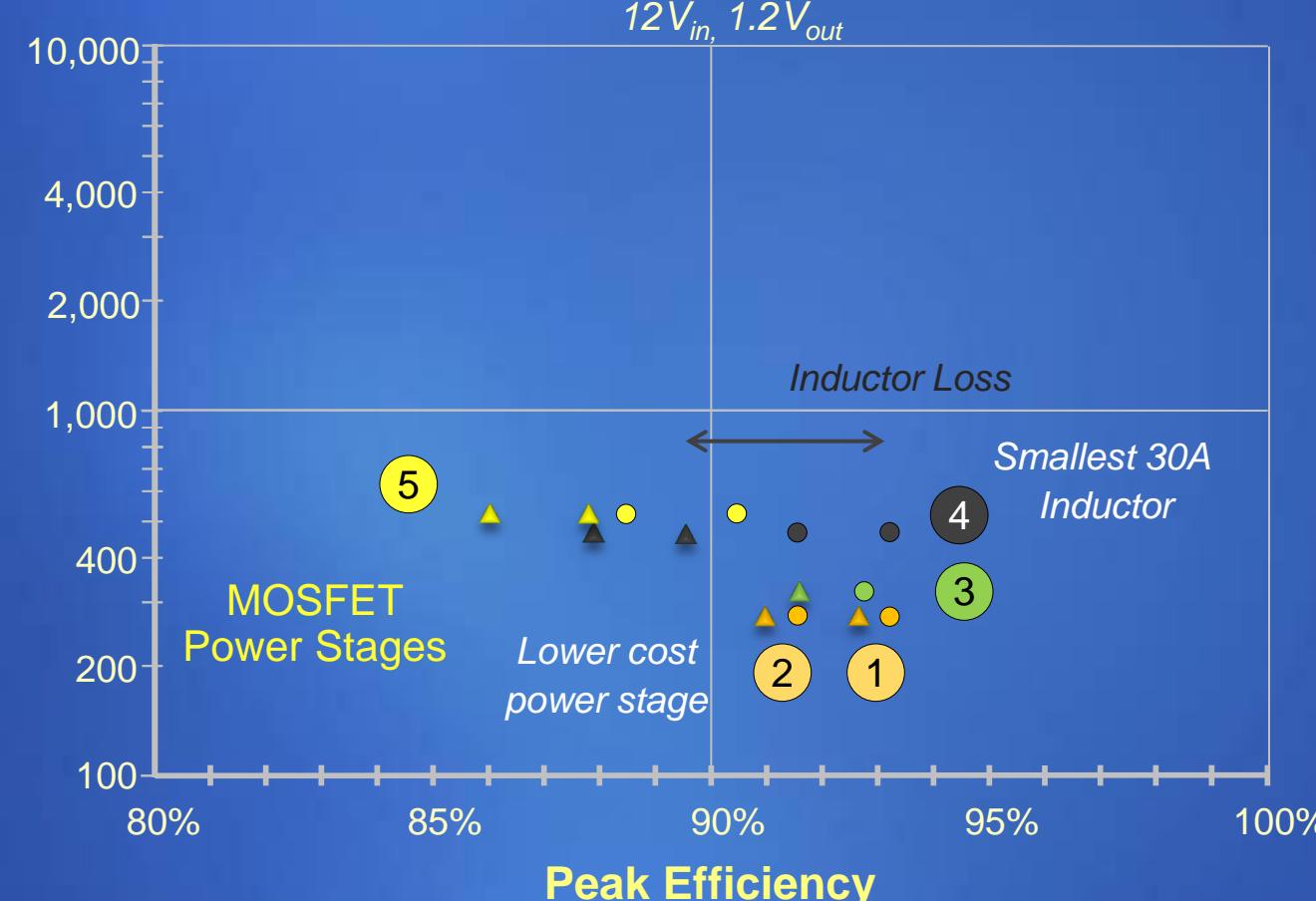
Good Efficiency at medium to full load



Key Metrics – Density (Size) and Efficiency

30A output current

Power Train
Density
(W/in³)

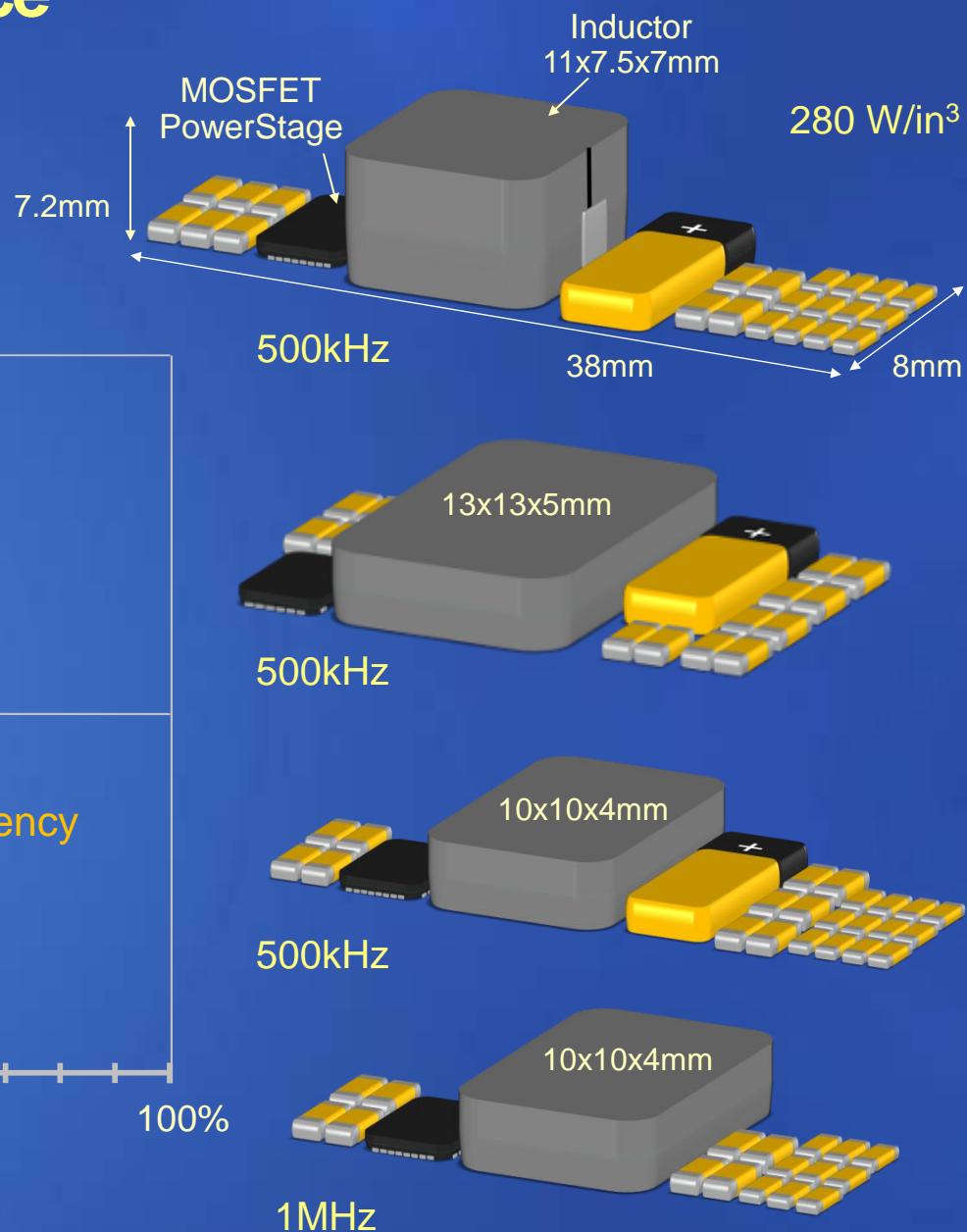
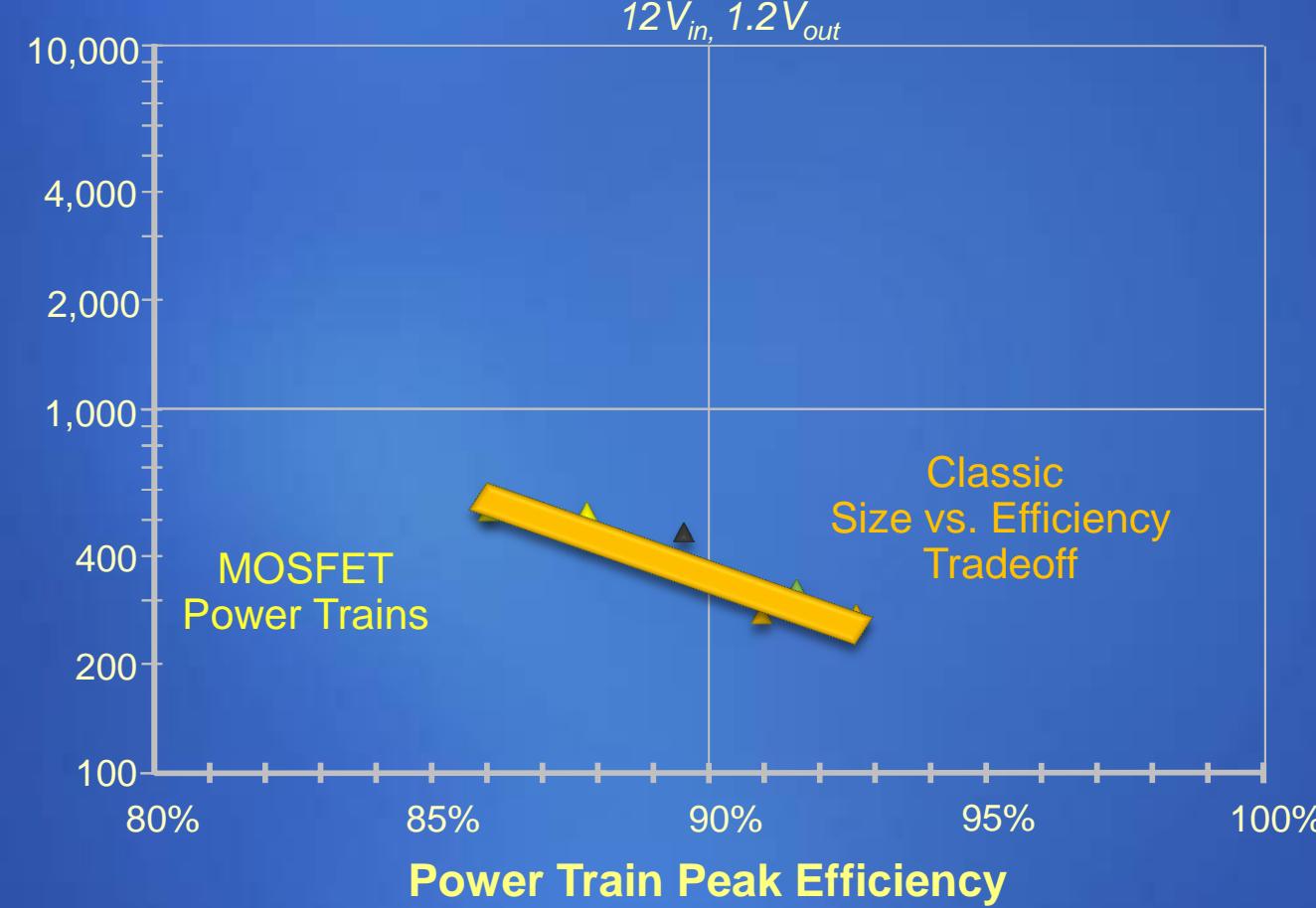


- Power Stage efficiency
- ▲ Power Train efficiency

MOSFET PowerTrain Performance

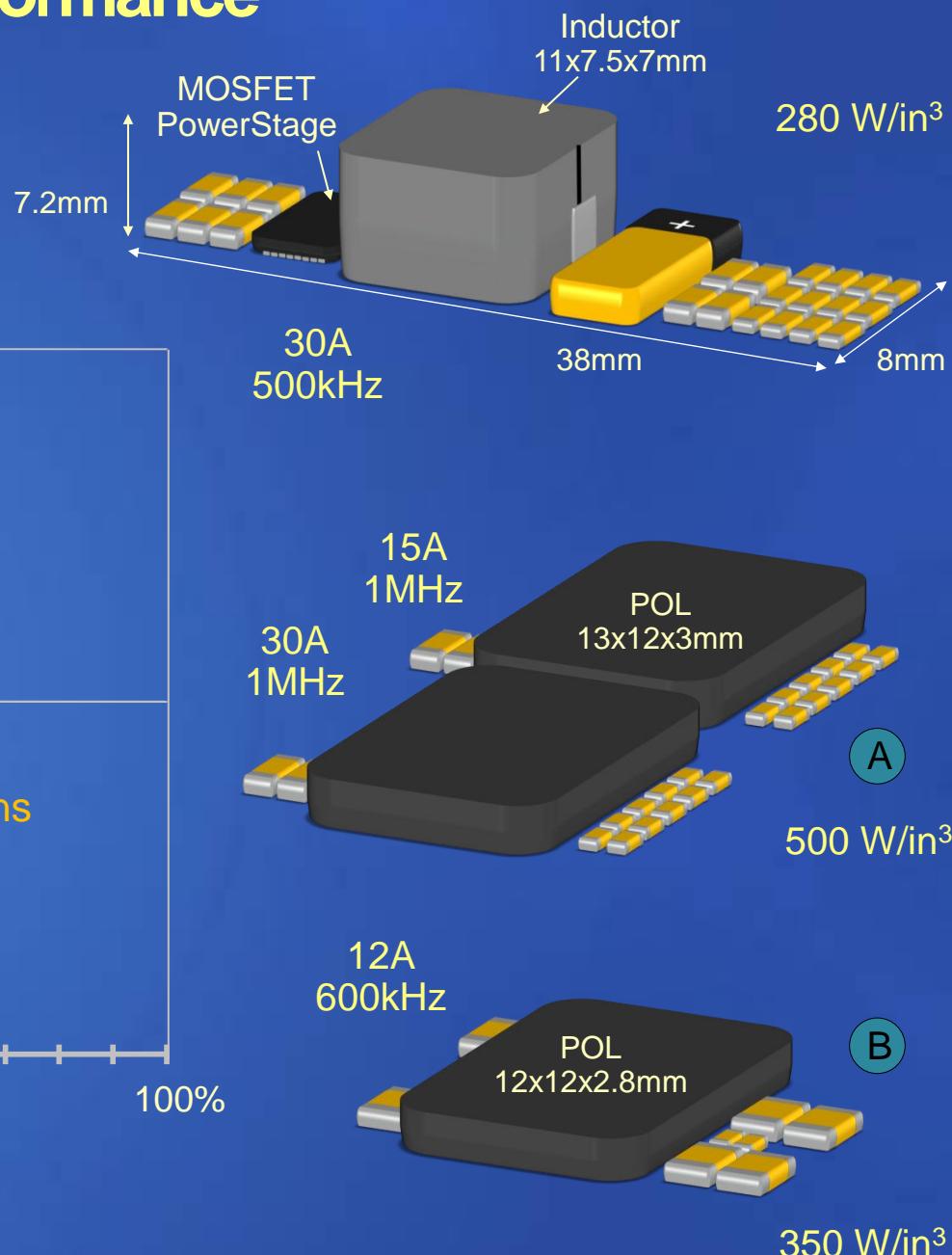
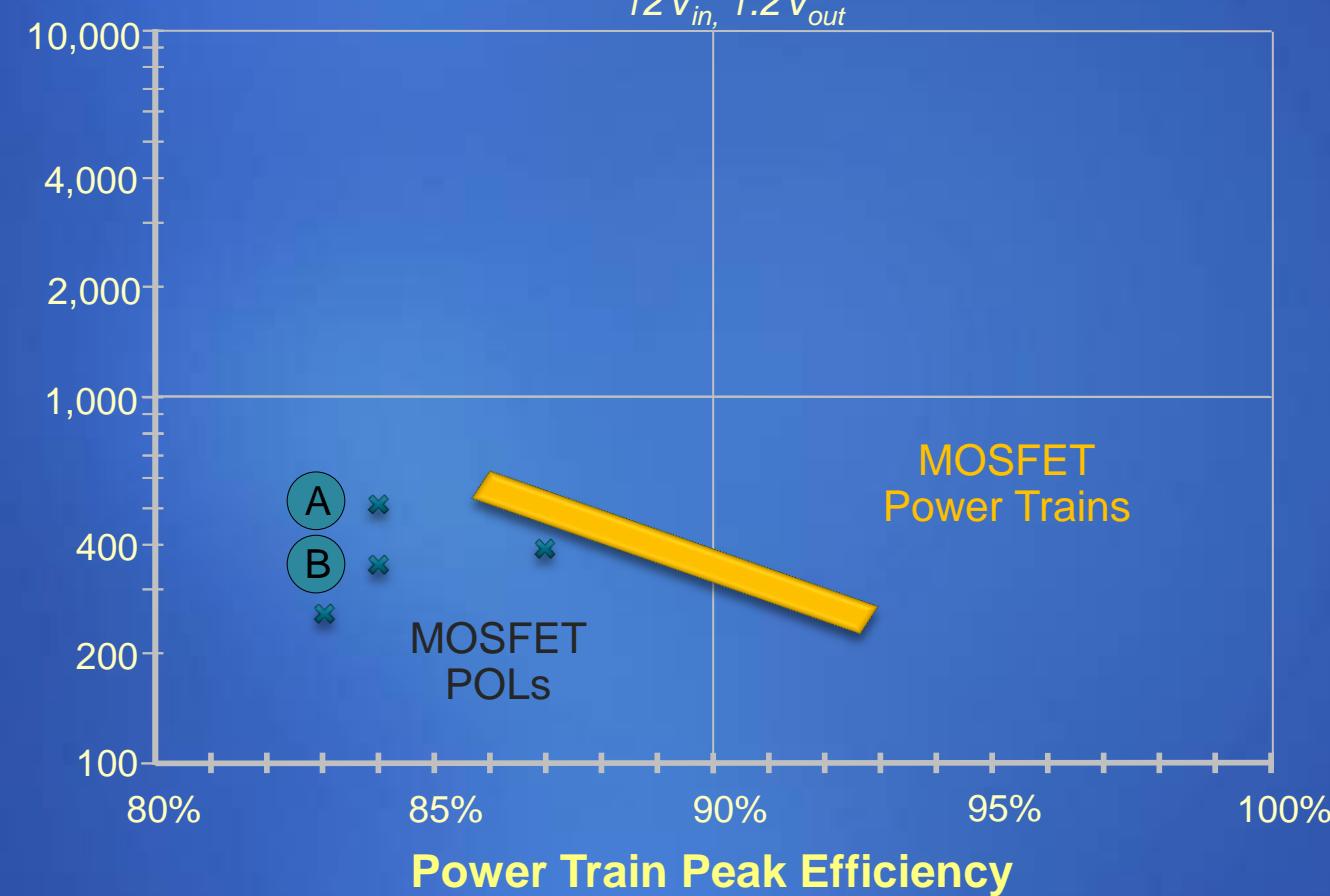
30A output current

Power Train
Density
(W/in³)



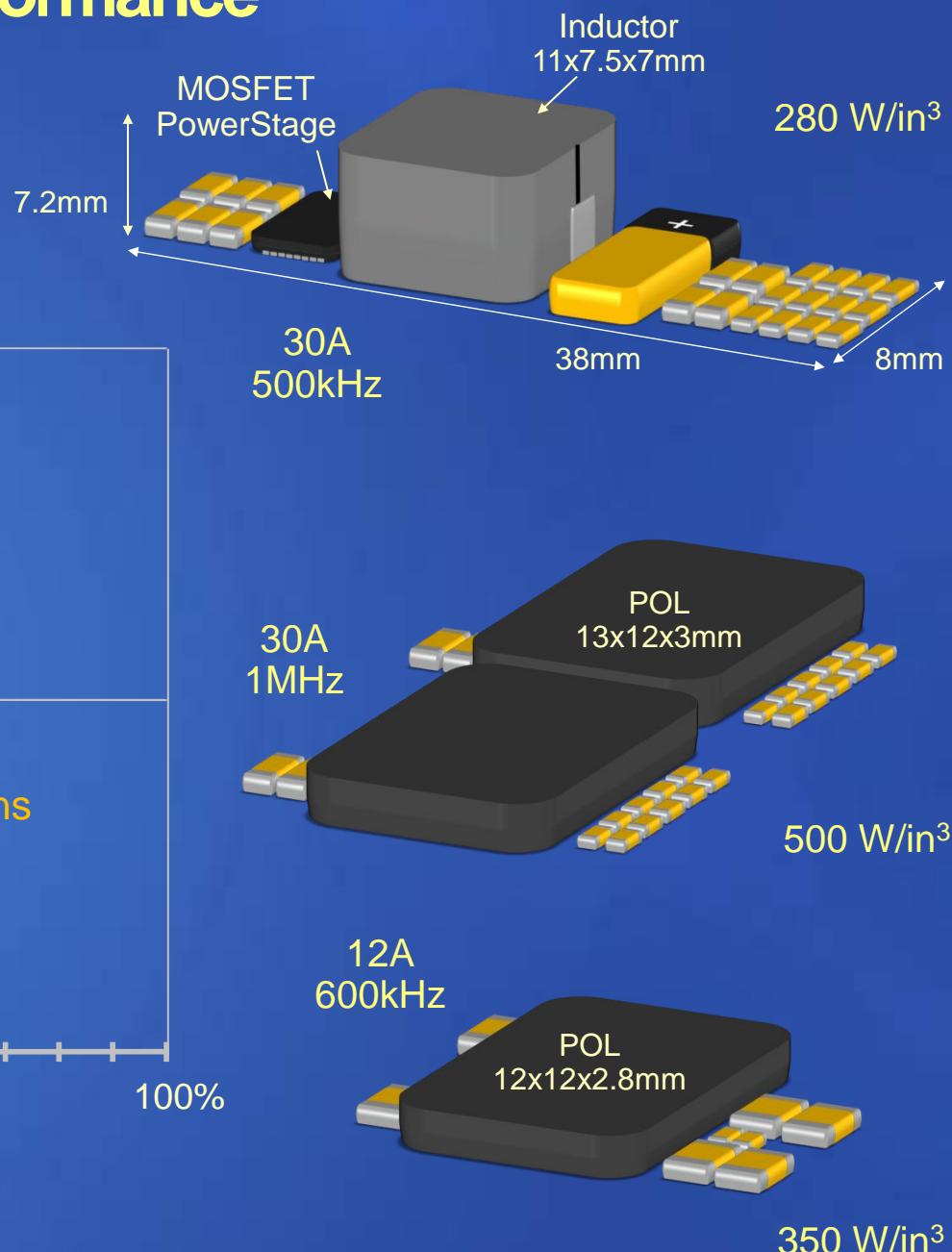
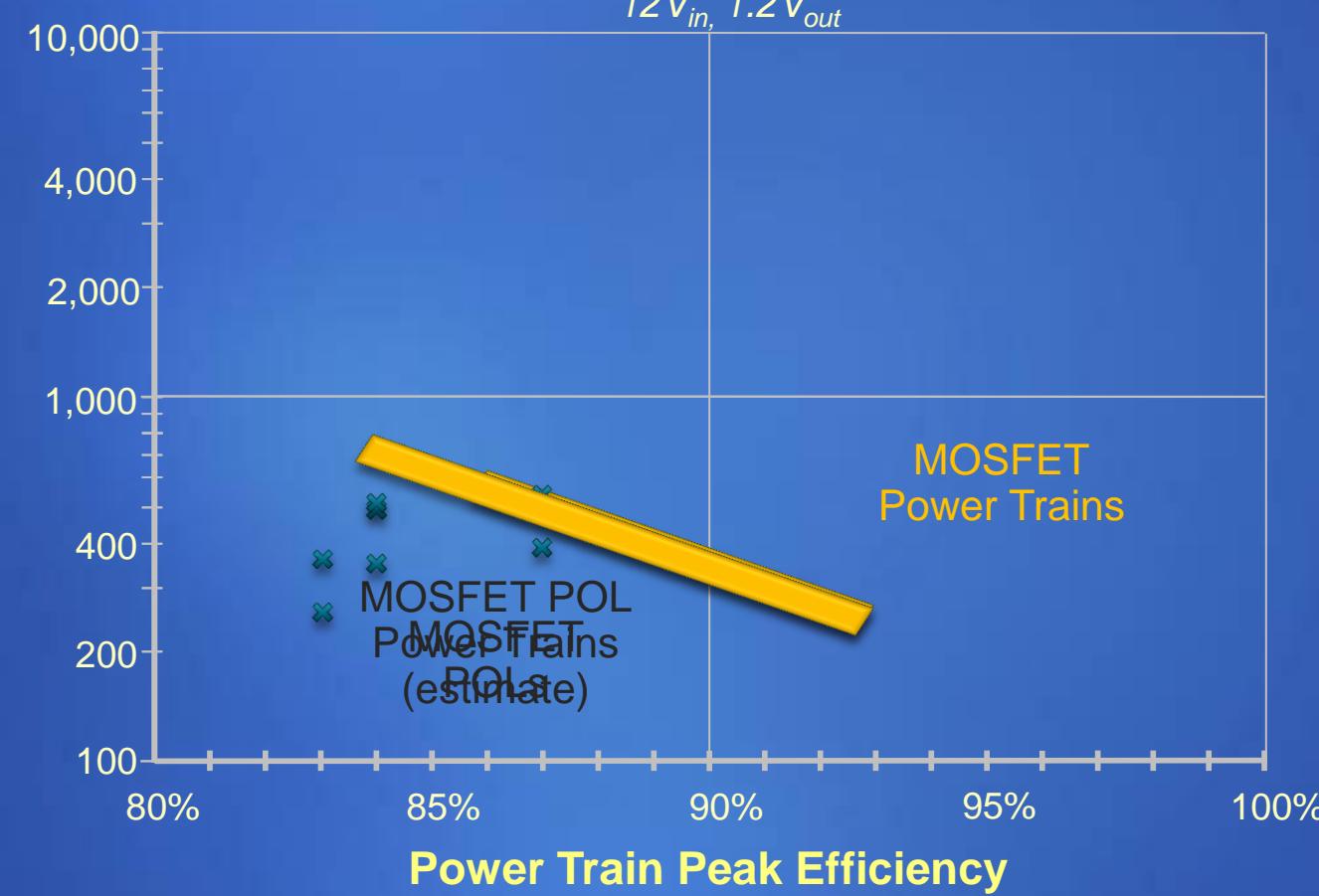
High Density POL Regulator Performance

Power Train
Density
(W/in³)



High Density POL Regulator Performance

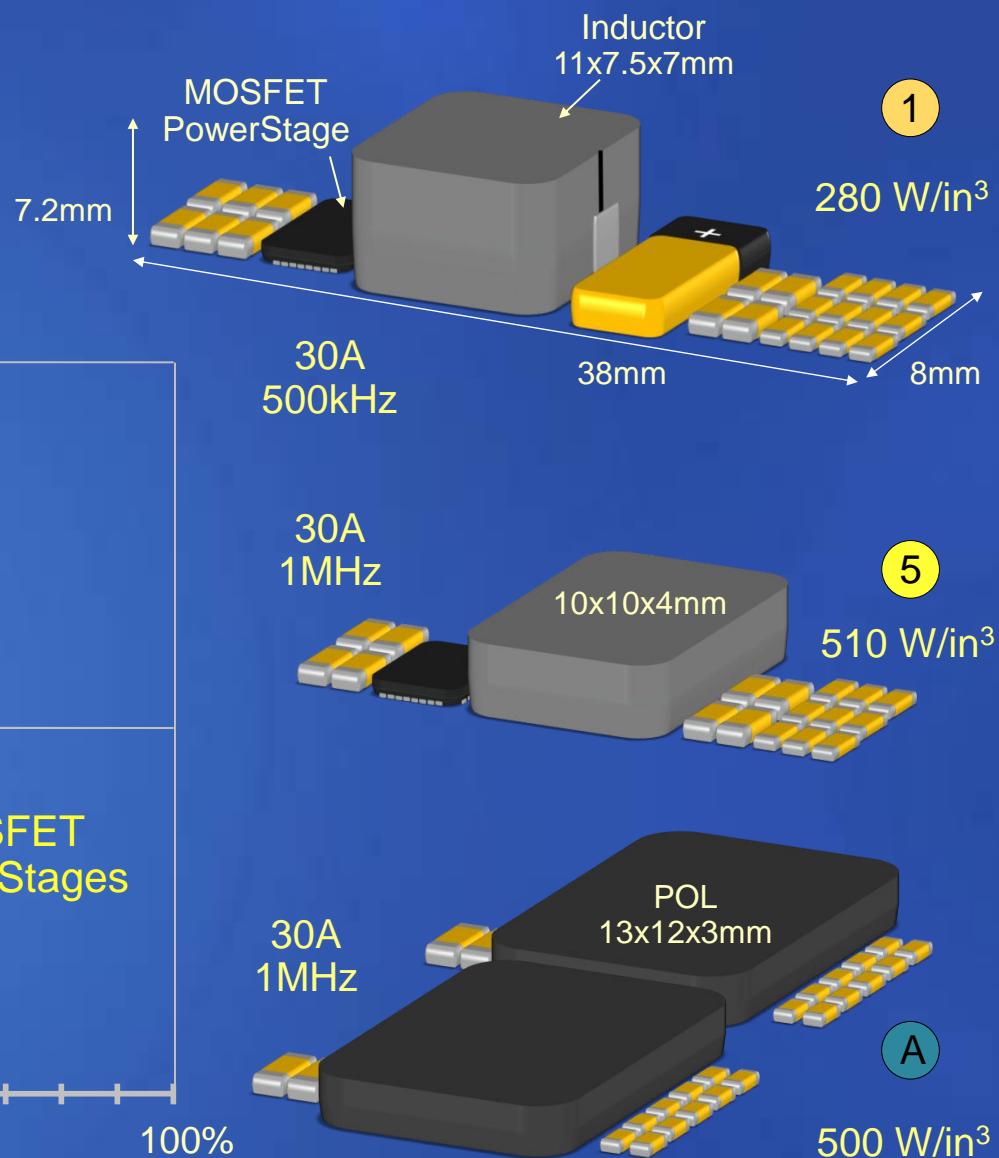
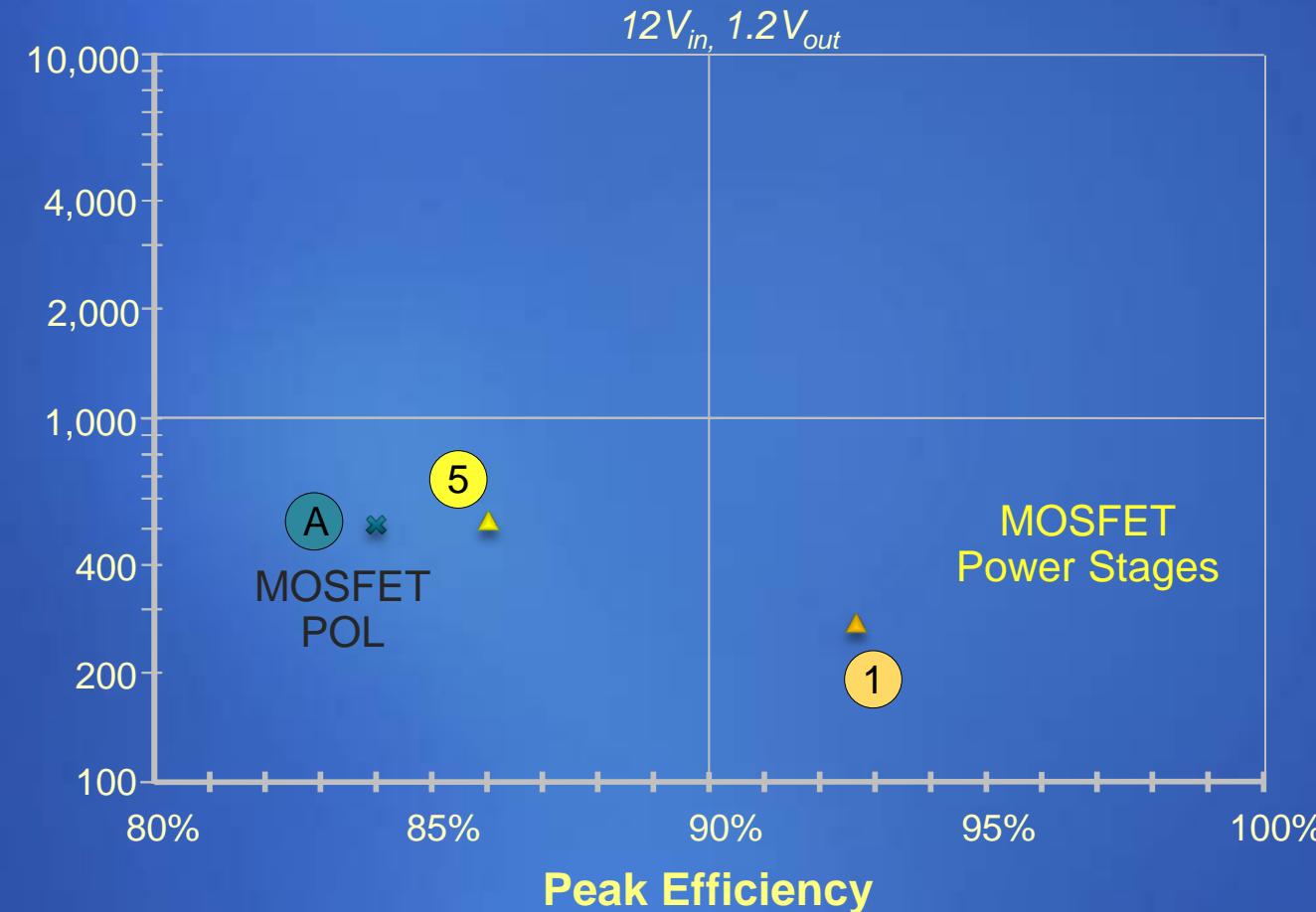
Power Train
Density
(W/in³)



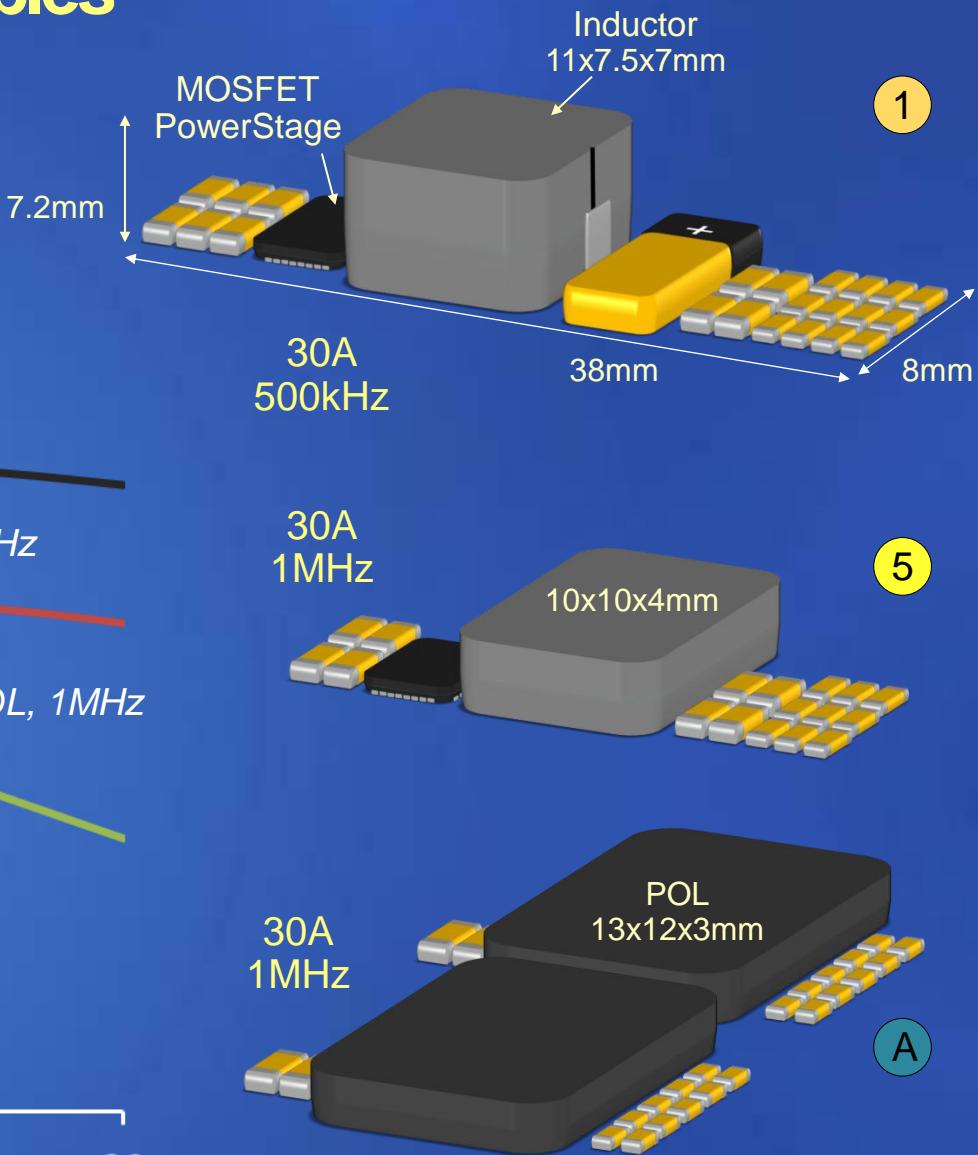
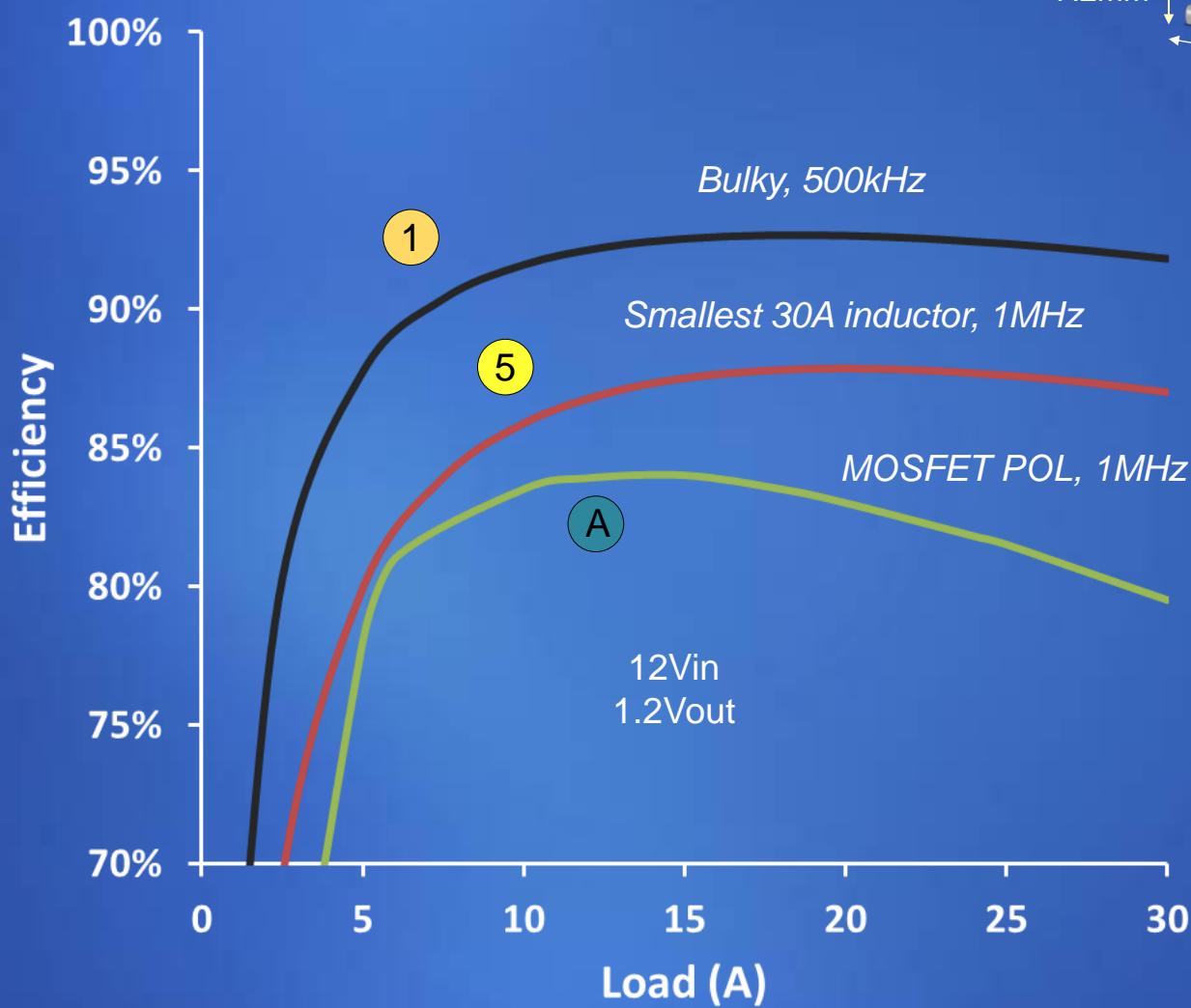
Closer Look at Three Examples

30A output current

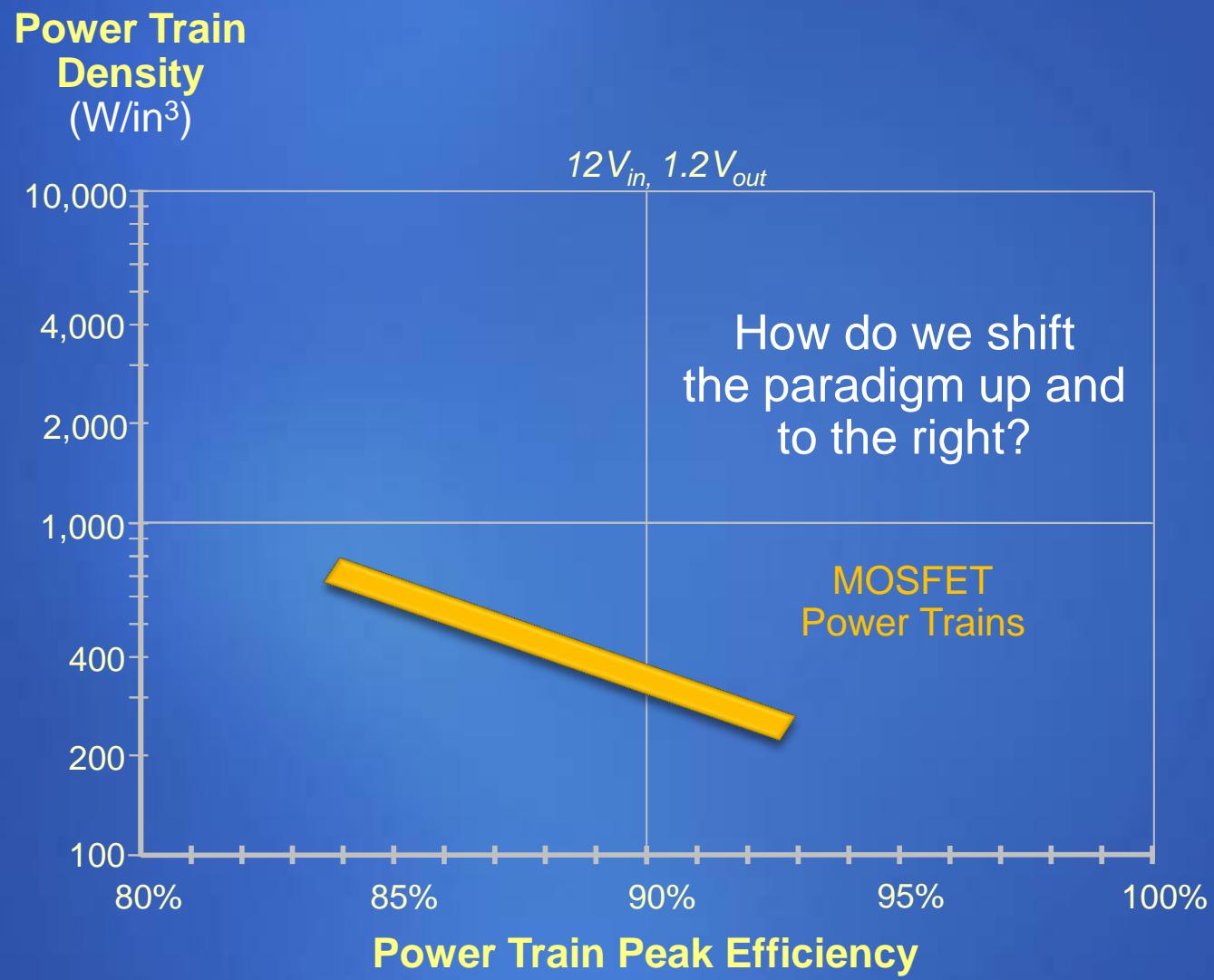
Power Train
Density
(W/in³)



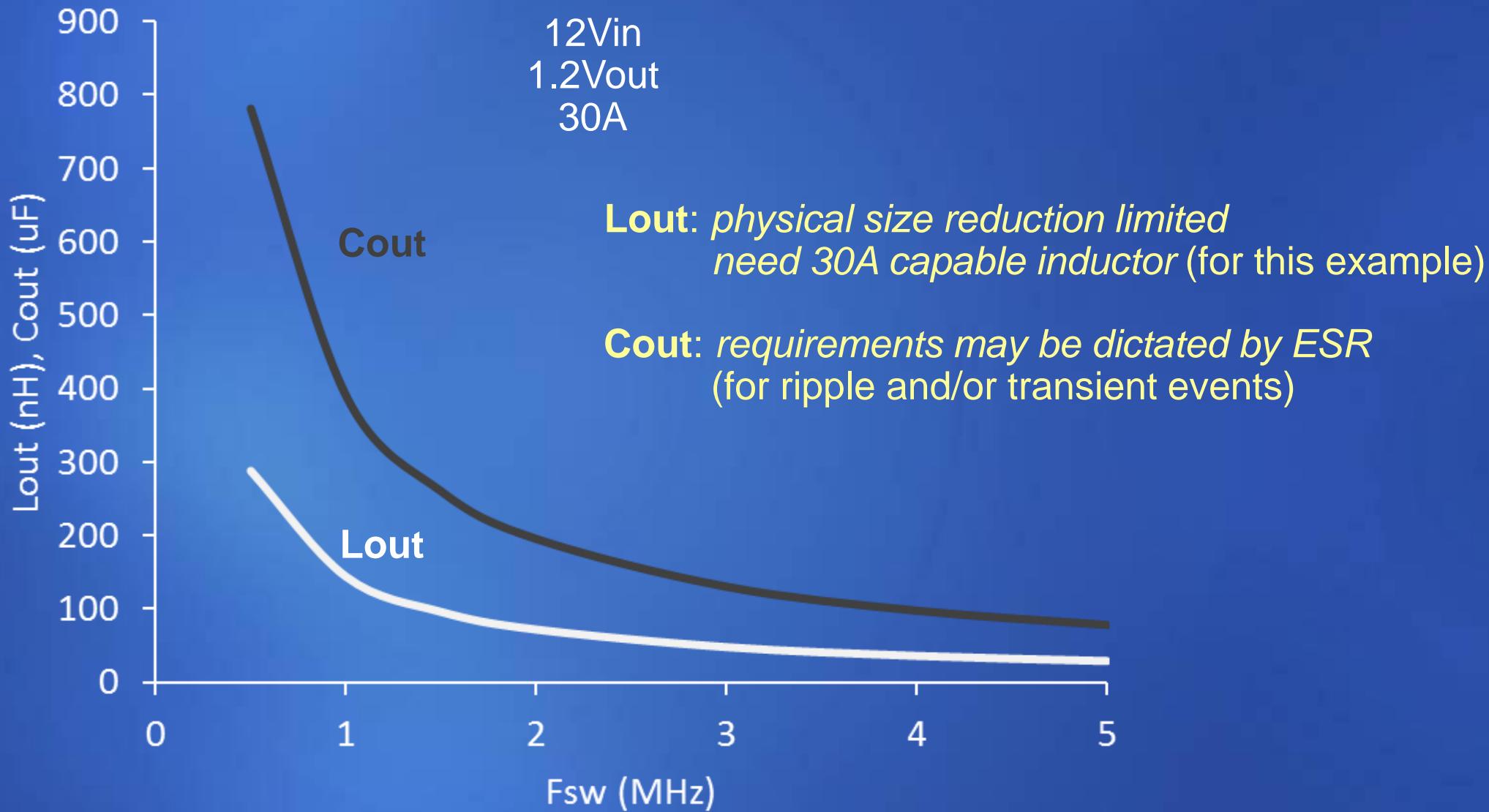
Efficiency Curves of Three Examples



High Density POL Regulator Performance



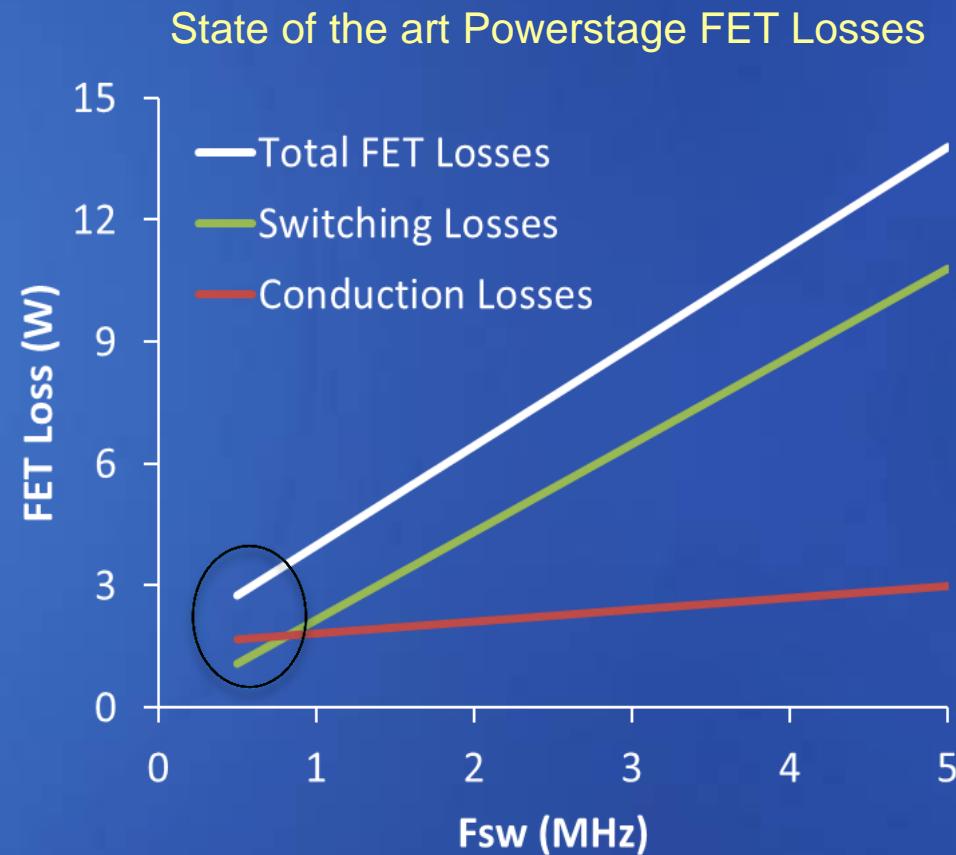
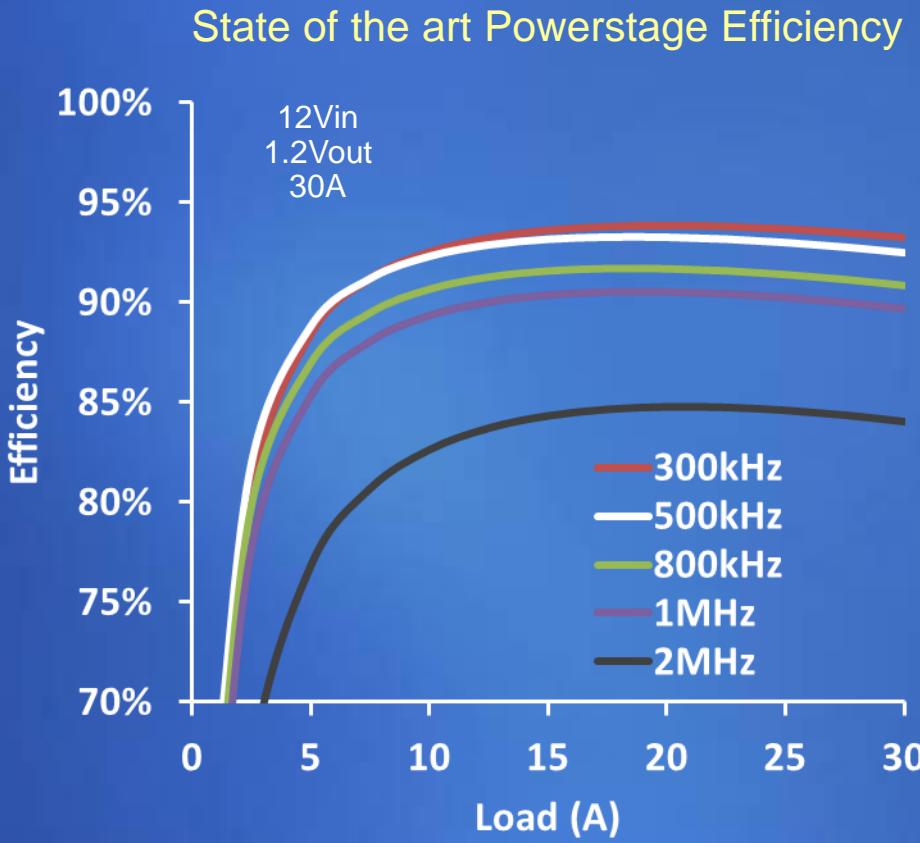
We need higher Switching Frequency to shrink the Output Filter



Challenges to Higher Density 12Vin POL solutions

(1) FET Switching Losses

MOSFETs are not up to the challenge of multi-MHz operation



Limited to less than ~1MHz

GaAs FET Advantages for 12Vinput POLs

	Vertical MOSFETs	GaN-on-Silicon FETs	GaAs FETs	Benefit
Electron Mobility (cm ² /Vs)	1,400	1,800	8,500	Fast Switching
R _{DS(on)} *Q _G (mΩ-nC)	~30	~25	Gen1 Gen2 12 → 6	Reduced Switching loss (ability to go to higher Fsw)
Body Diode	Yes	No	No	No Qrr loss
FET Structure	Vertical	Lateral	Lateral	Monolithic integration of UFET / LFET (reduced parasitics)

Green text: merit

Additional Information on Sarda's GaAs FET developments:

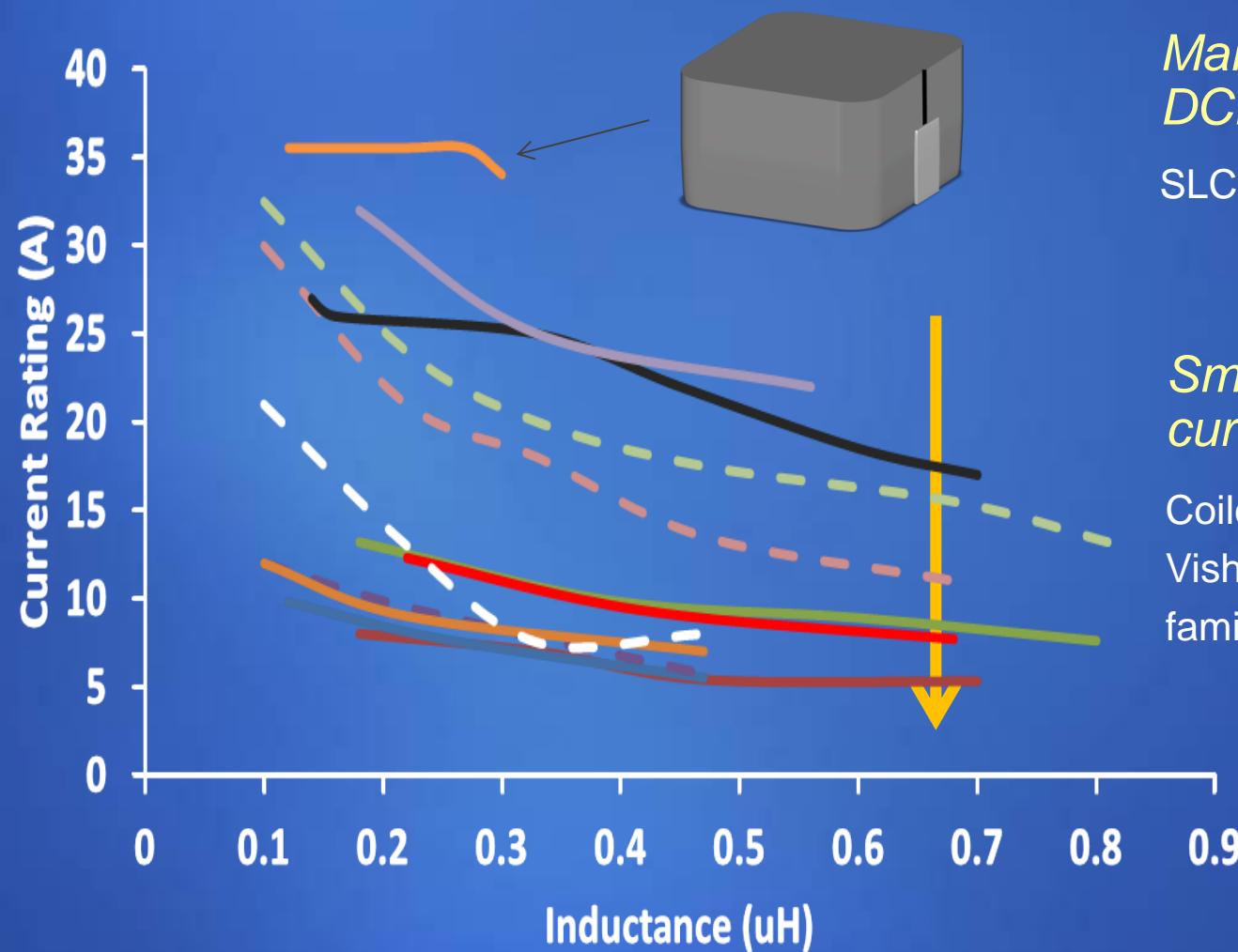
- APEC 2013: “**The gFET™ Switch: A New Low Voltage High Speed GaAs HEMT for Switching Applications**”, Robert White, et al.
- IMAPS 2013: “**A Highly-Integrated GaAs-based Module for DC-DC Regulators**”, Greg Miller, et al.
- APEC 2014: “**Recent Developments In GaAs Power Switching Devices Including Device Modeling**”, Robert White, et al.

Challenges to Higher Density 12Vin POL solutions

(1) FET Switching Losses

→ Sarda GaAs FET

(2) High current inductors are large



30A inductors are large

Many choices for low DCR, bulky Inductors

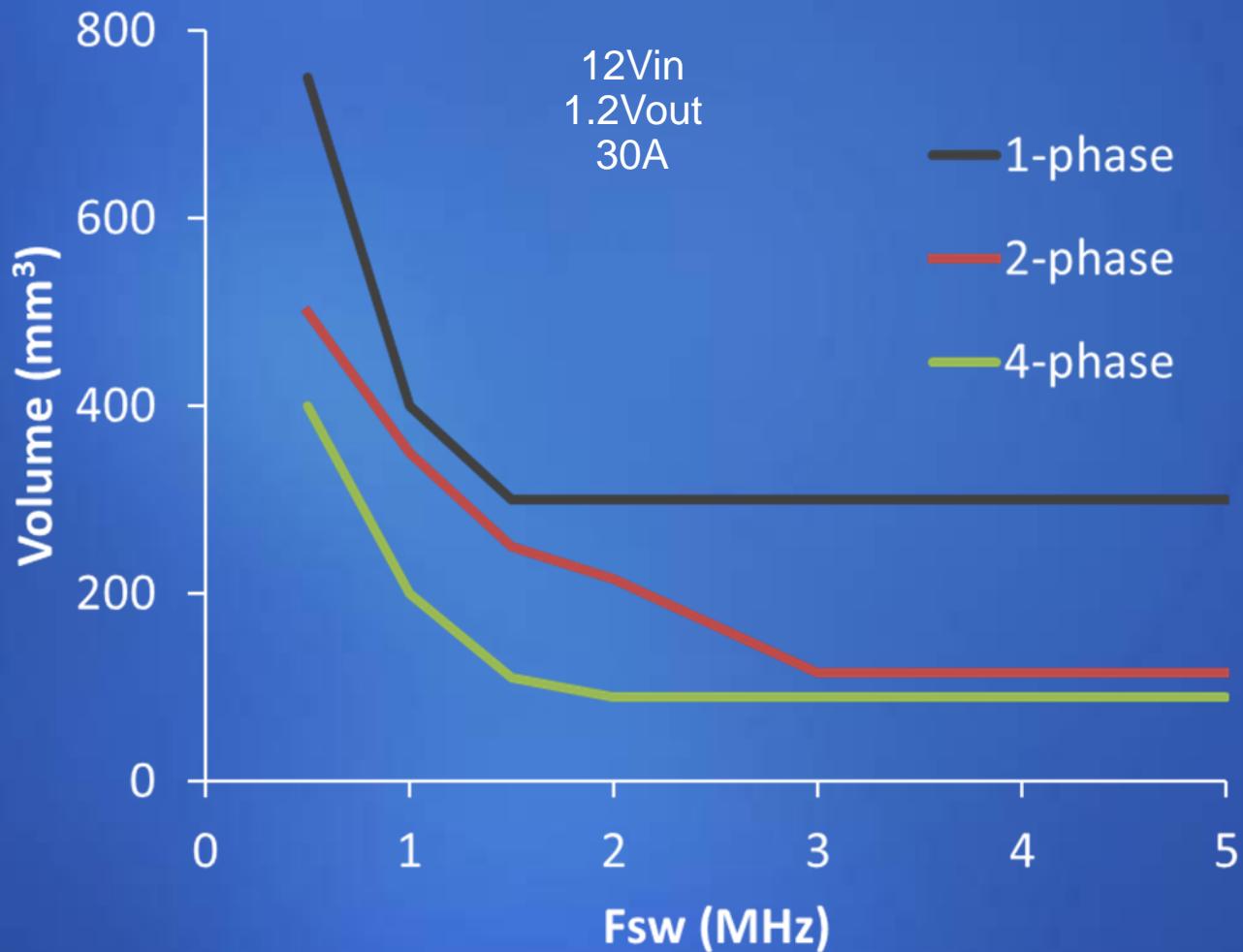
SLC1175 example

Smaller form-factor Inductors – current capability drops

Coilcraft XAL, XFL (solid lines),
Vishay IHLP (dashed lines)
families shown

Challenges to Higher Density 12Vin POL solutions

- (1) FET Switching Losses → Sarda GaAs FET
(2) High current inductors are large → Multiphase (lower I/phase)

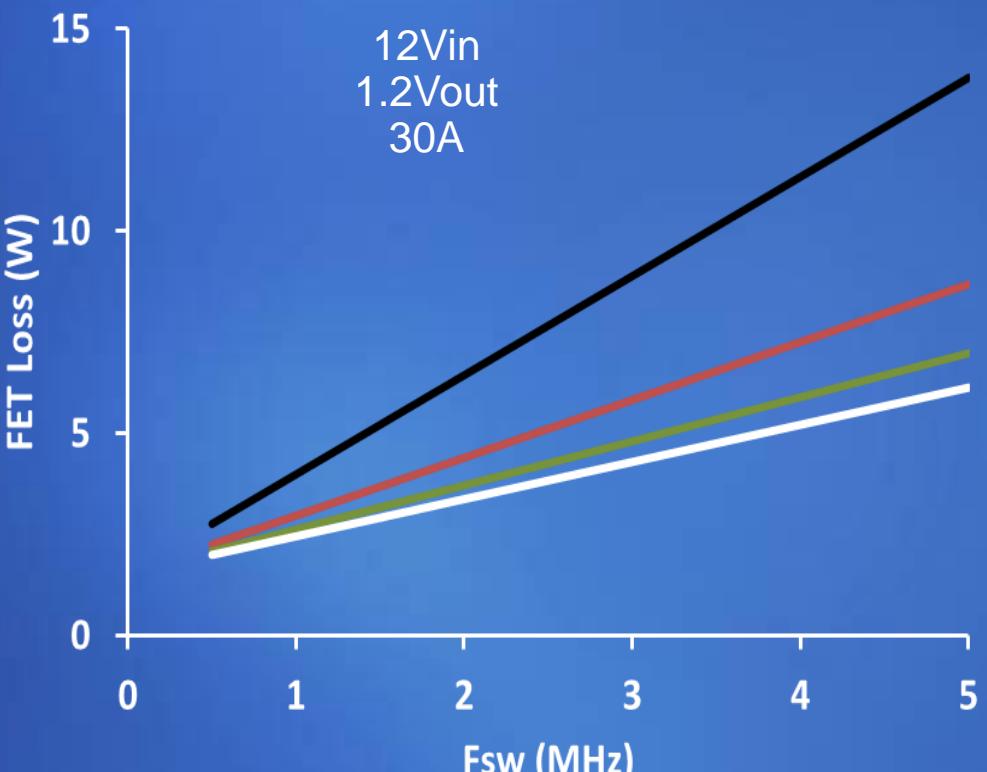


Inductor Volume decreases with higher Phase count

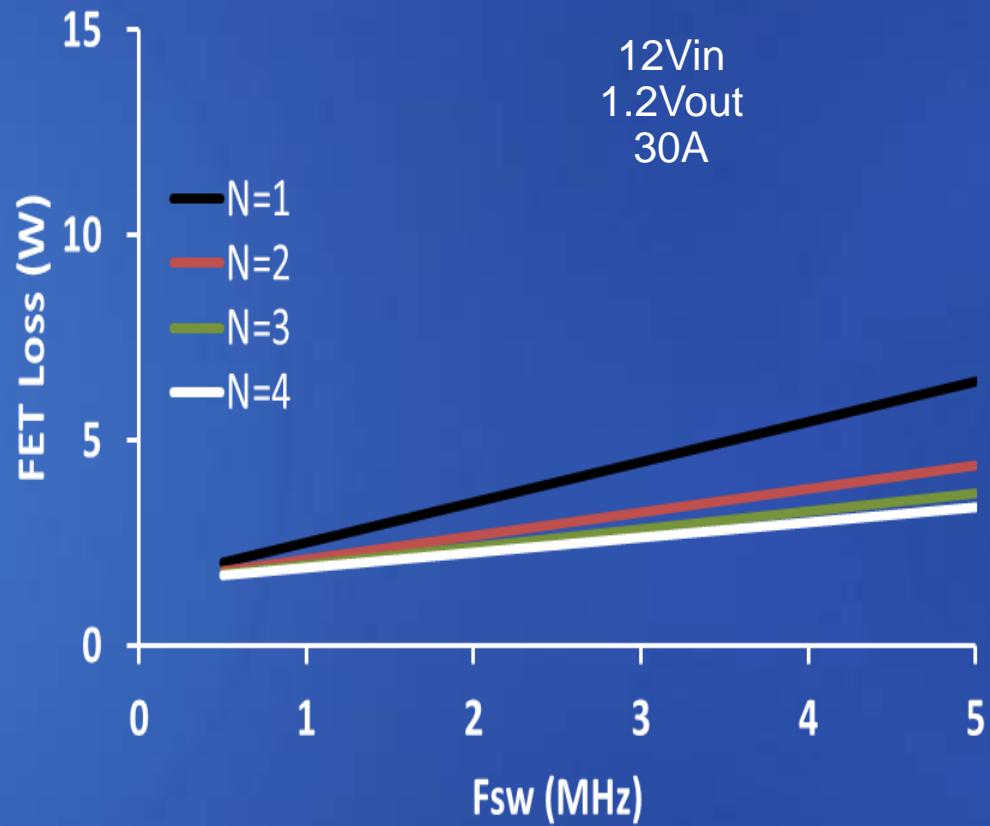
General example/trend
More than one inductor solution choice per conditions examined

Another Multiphase Benefit

FET switching losses reduced



MOSFETs

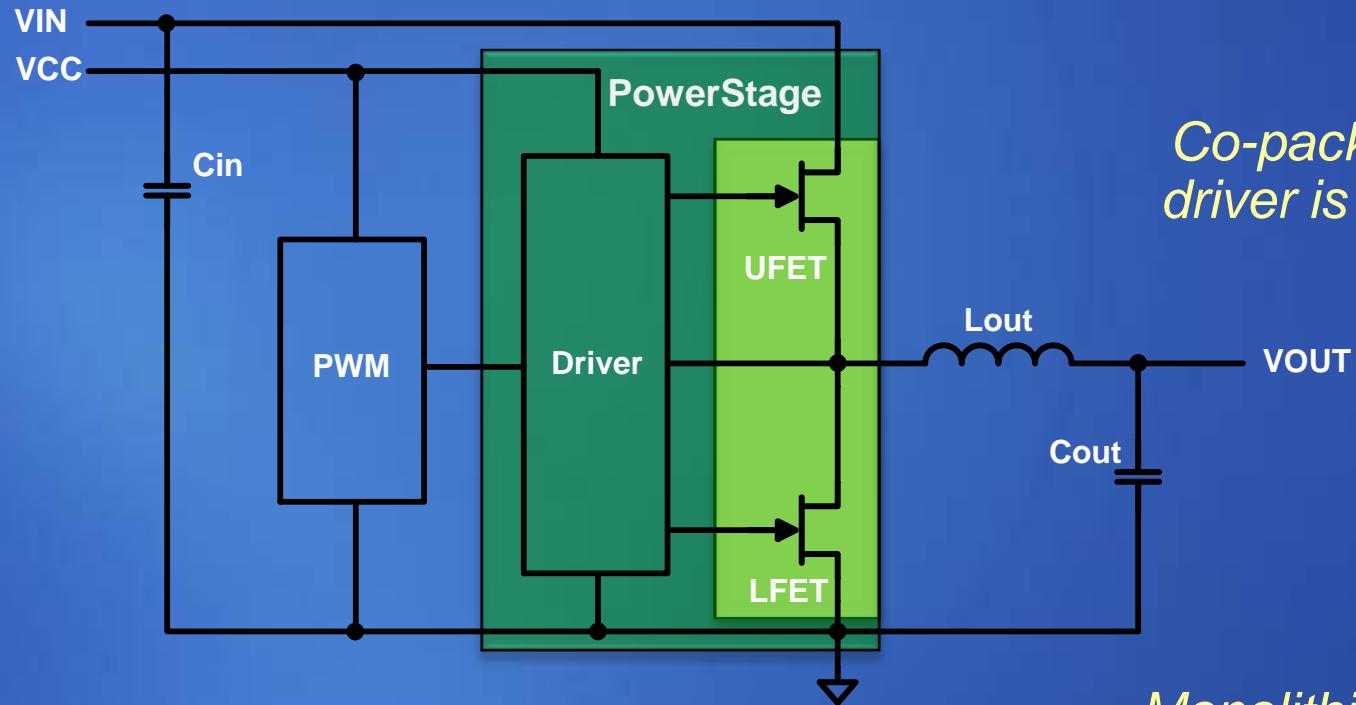


*Sarda GaAs FETs **

* In HIPS module (explained later)

Challenges to Higher Density 12Vin POL solutions

- (1) FET Switching Losses → **Sarda GaAs FET**
- (2) High current inductors are large → **Multiphase** (lower I/phase)
- (3) Parasitic Impedances

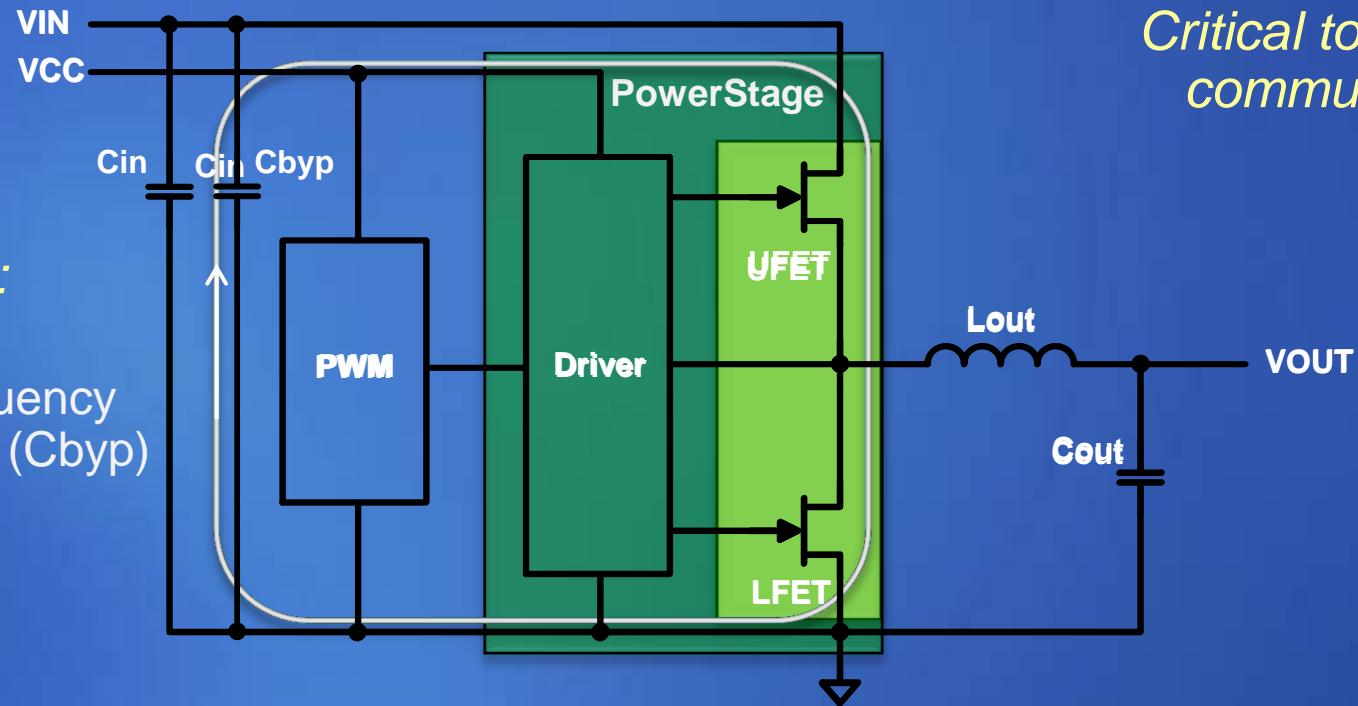


Co-packing FETs and driver is a requirement

Monolithic UFET / LFET minimizes critical common source inductance

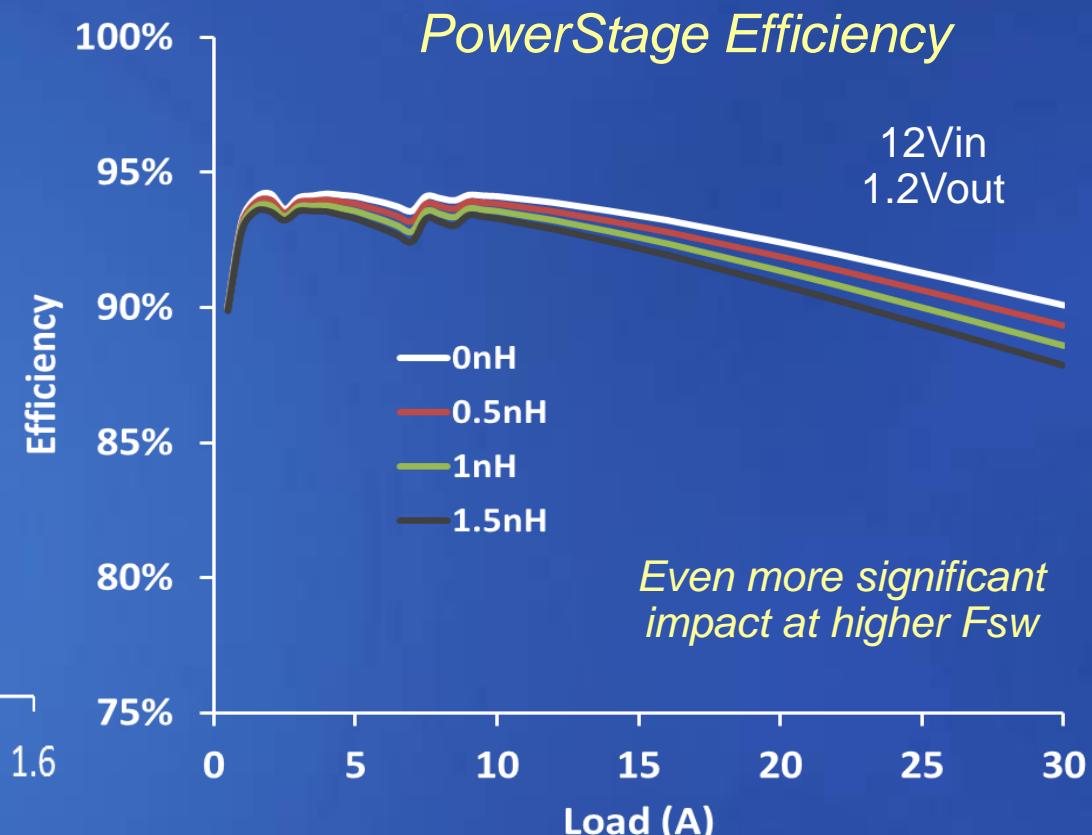
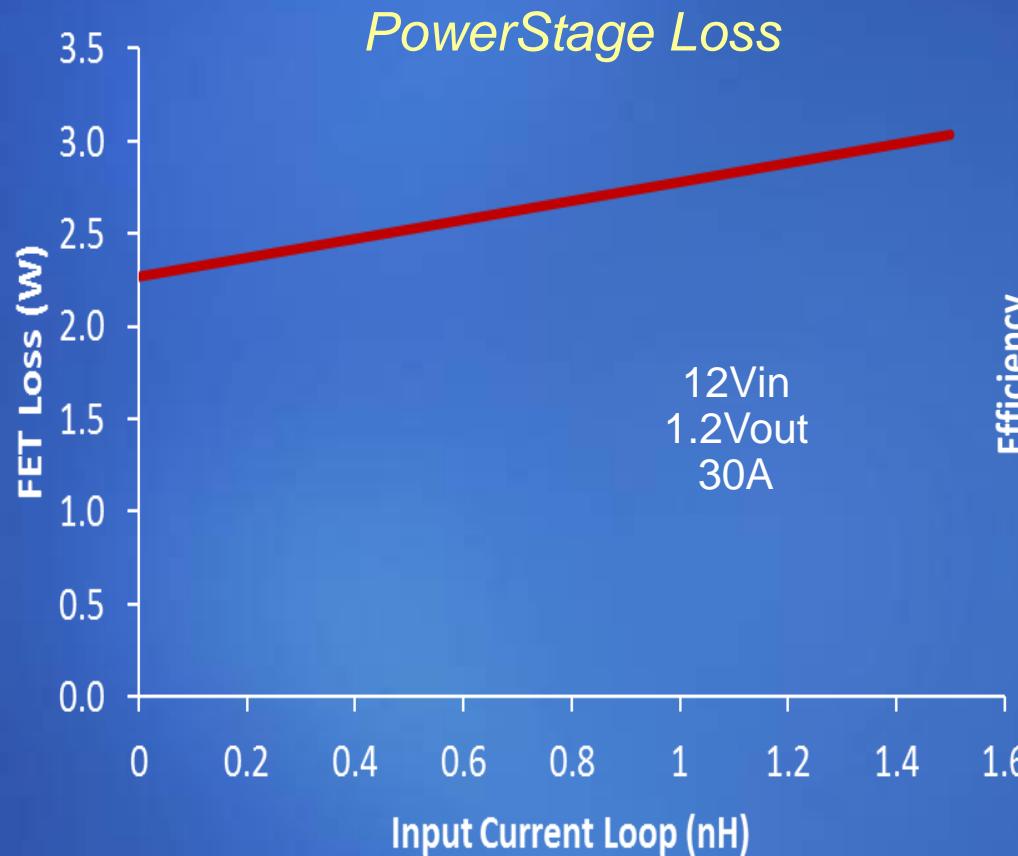
Challenges to Higher Density 12Vin POL solutions

- (1) FET Switching Losses → Sarda GaAs FET
- (2) High current inductors are large → Multiphase (lower I/phase)
- (3) Parasitic Impedances



Minimize Input Current Loop

Quantifying with Sarda Gen1 HIPS (4-phase, 2MHz)

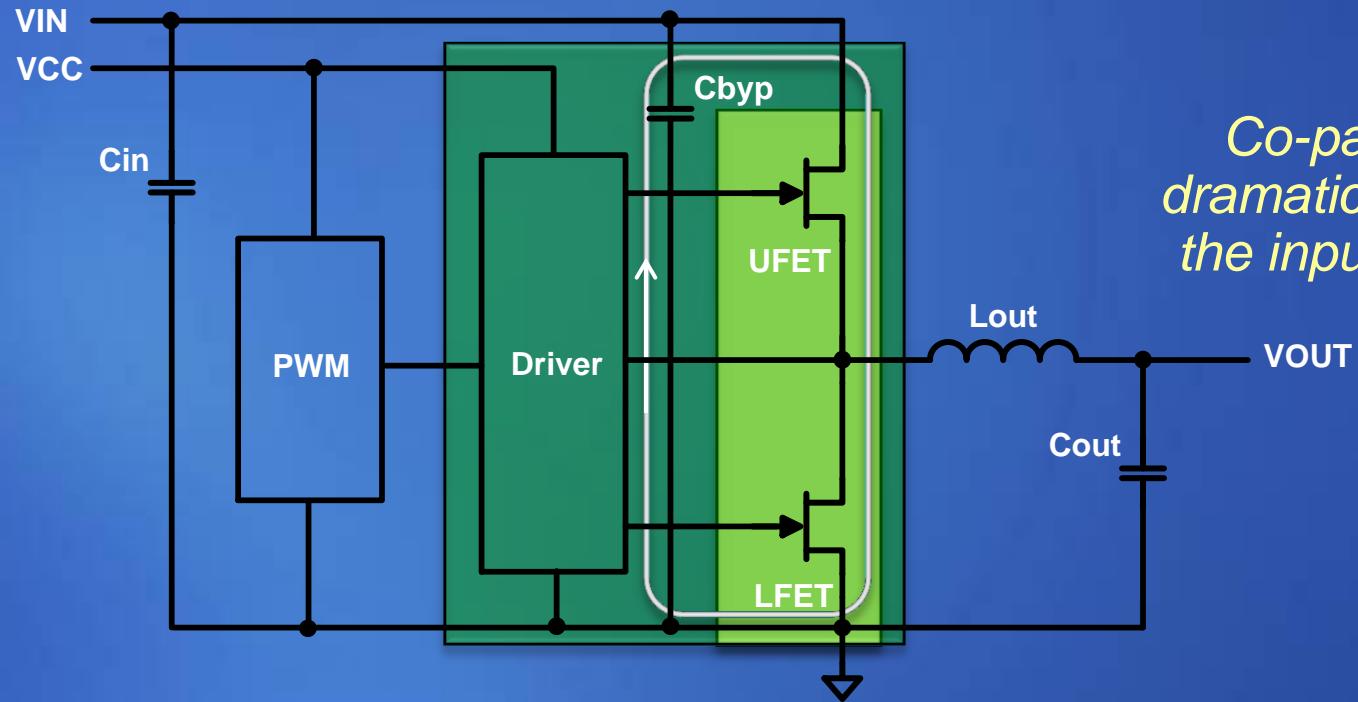


Additional Information on impact of Input Current Loop Inductance:

- APEC 2013: “**Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter**”, David Reusch, et al.
- IMAPS 2013: “**A Highly-Integrated GaAs-based Module for DC-DC Regulators**”, Greg Miller, et al.

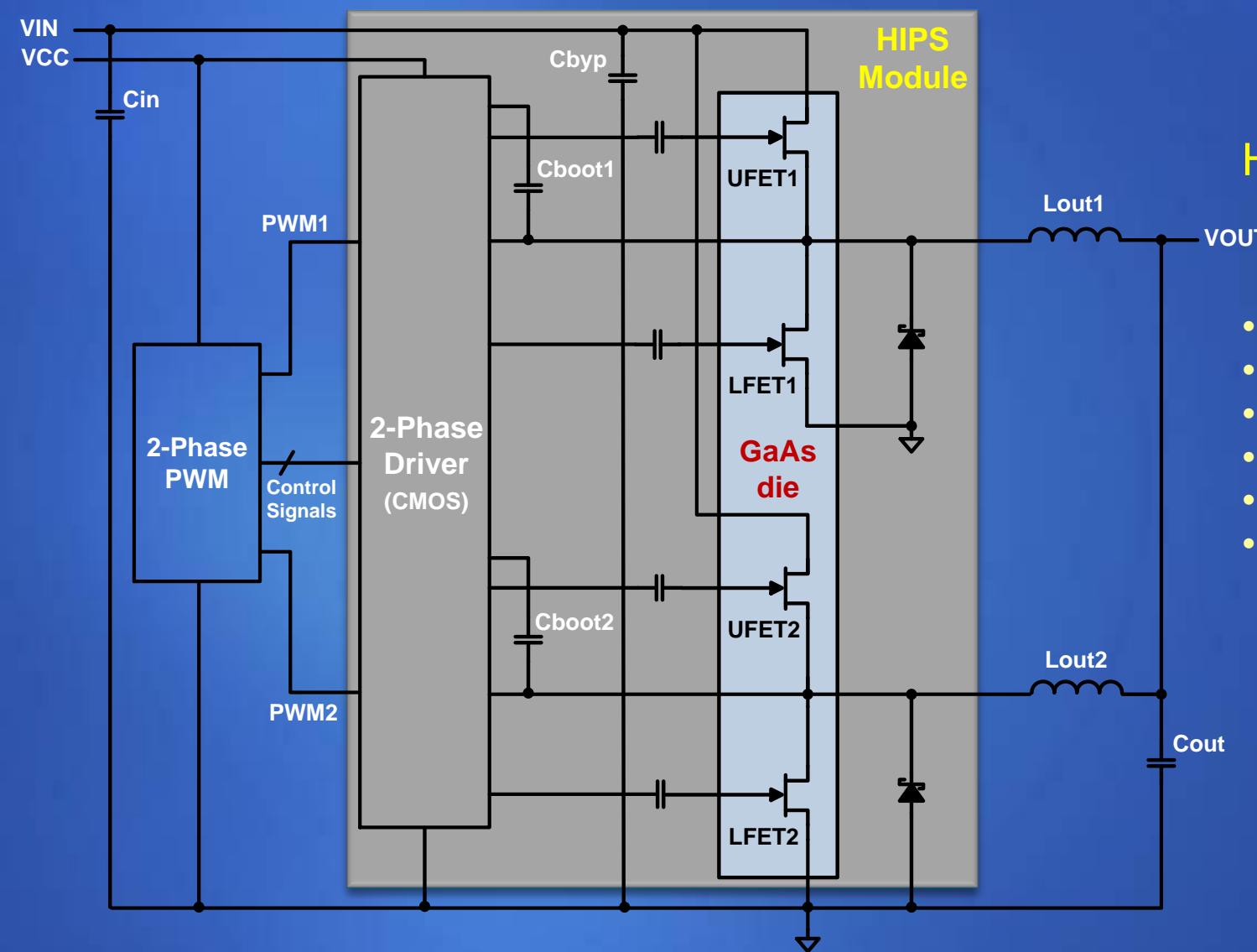
Challenges to Higher Density 12Vin POL solutions

- (1) FET Switching Losses → Sarda GaAs FET
- (2) High current inductors are large → Multiphase (lower I/phase)
- (3) Parasitic Impedances → Integrated Power Stage



*Co-packing Cbyp
dramatically minimizes
the input current loop*

Integrated Power Stage Approach: HIPS



HIPS: Heterogeneously Integrated Power Stage

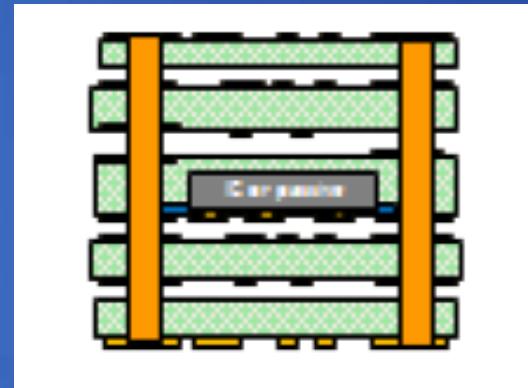
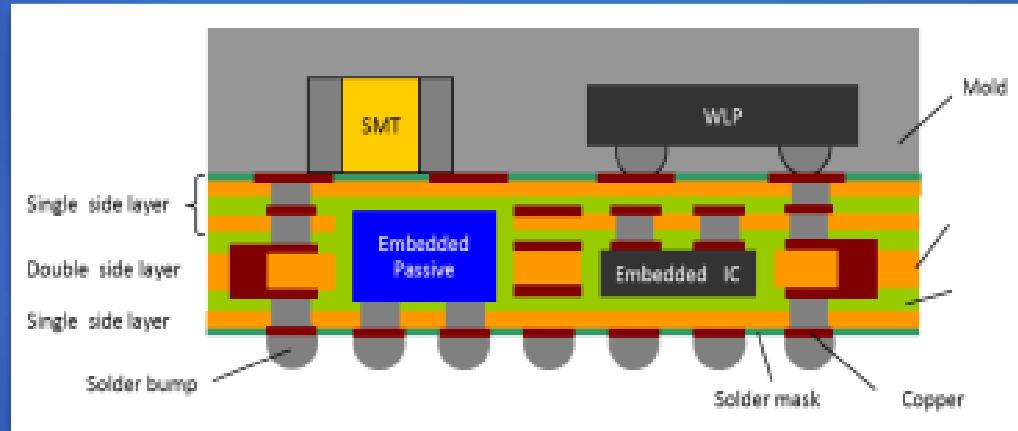
- Monolithic Quad GaAs die
- 2-phase CMOS driver
- C_{byp}
- Boot caps
- AC-coupled gate caps
- Schottky diodes (for diode emulation)

Integrates performance-critical components

HIPS Module

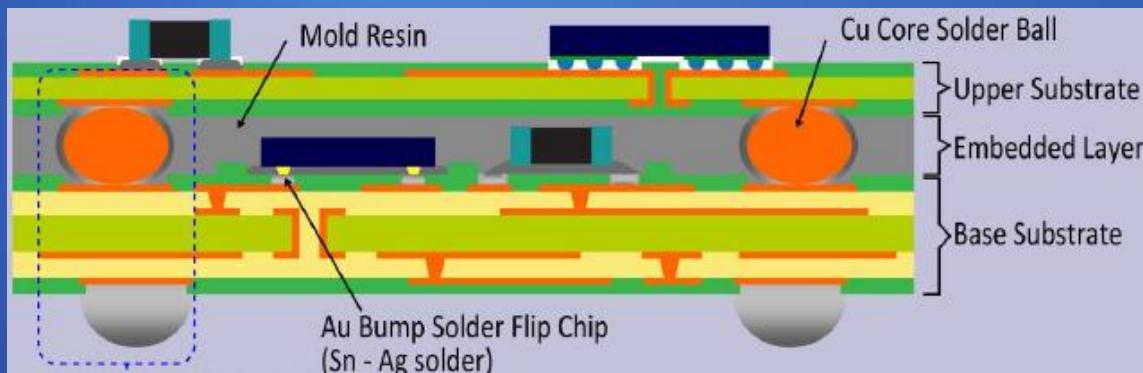
Available technology to enable compact multi-chip HIPS module:
Embedded Die in Substrate

- Two motivations: (1) Performance (*minimize parasitics for multi-MHz operation*)
(2) PowerStage package size



ECP®
Technology
from AT&S

ChipsetT™ Technology from FCI and Fujikura



MCeP® Technology from Shinko Electric



SESUB Technology
from TDK

HIPS Approach

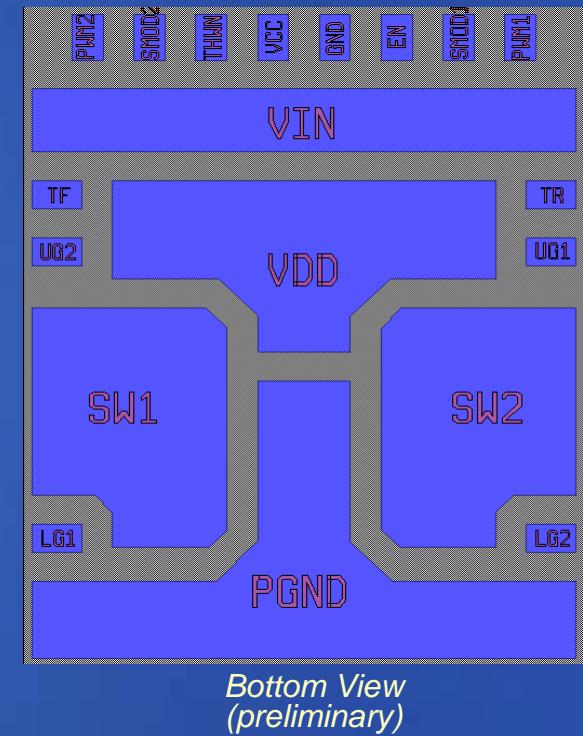
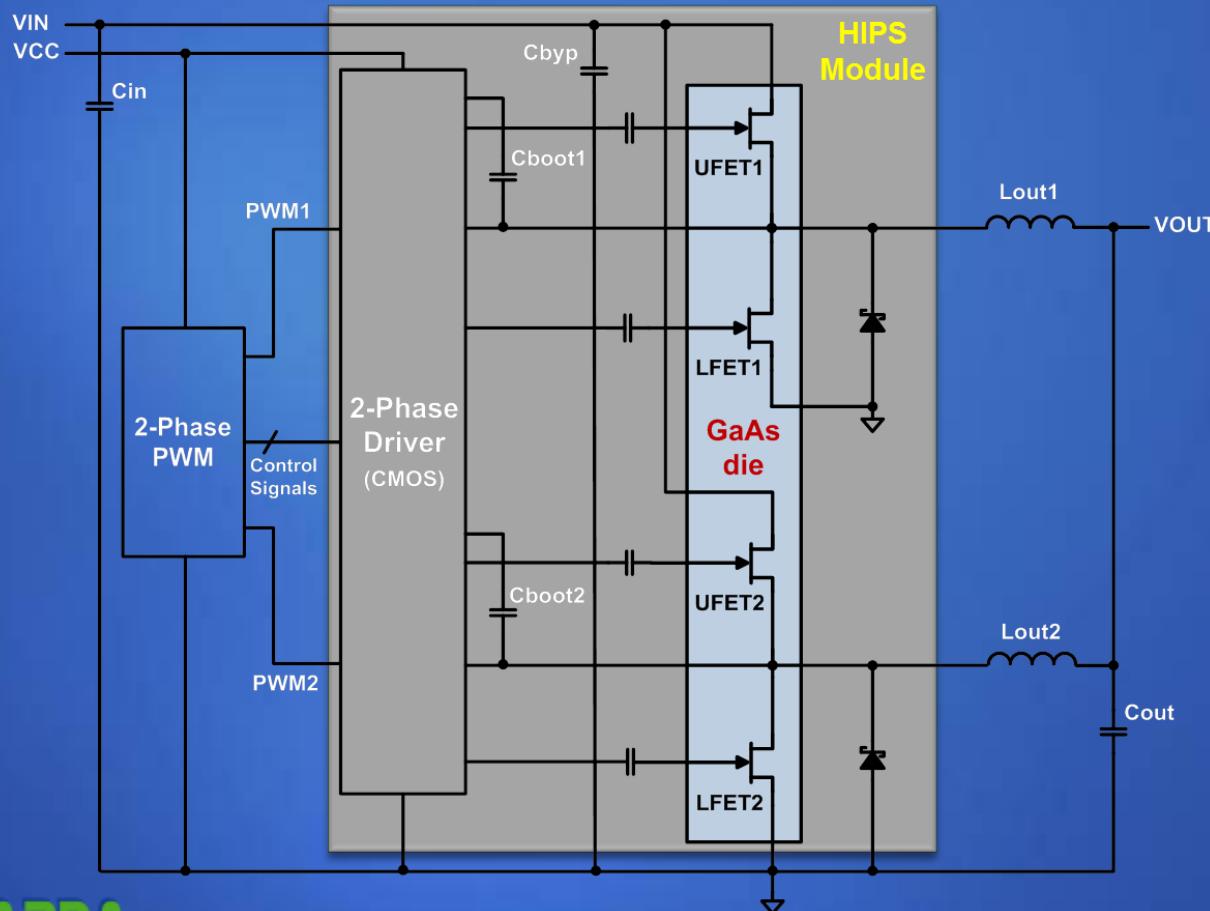
- Embed Active components

- Quad GaAs FET die
- CMOS 2-phase driver



- Integrate performance-critical components

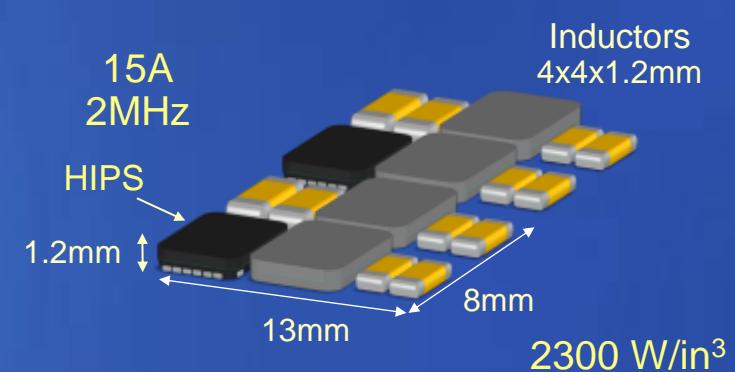
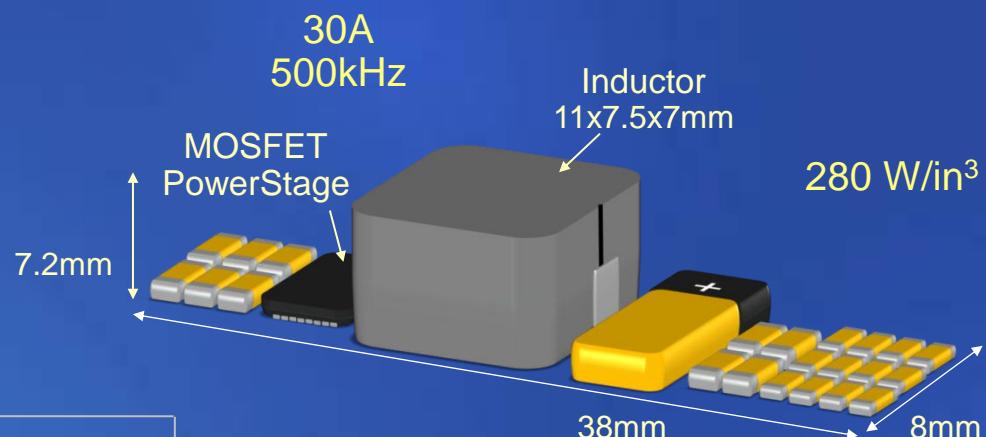
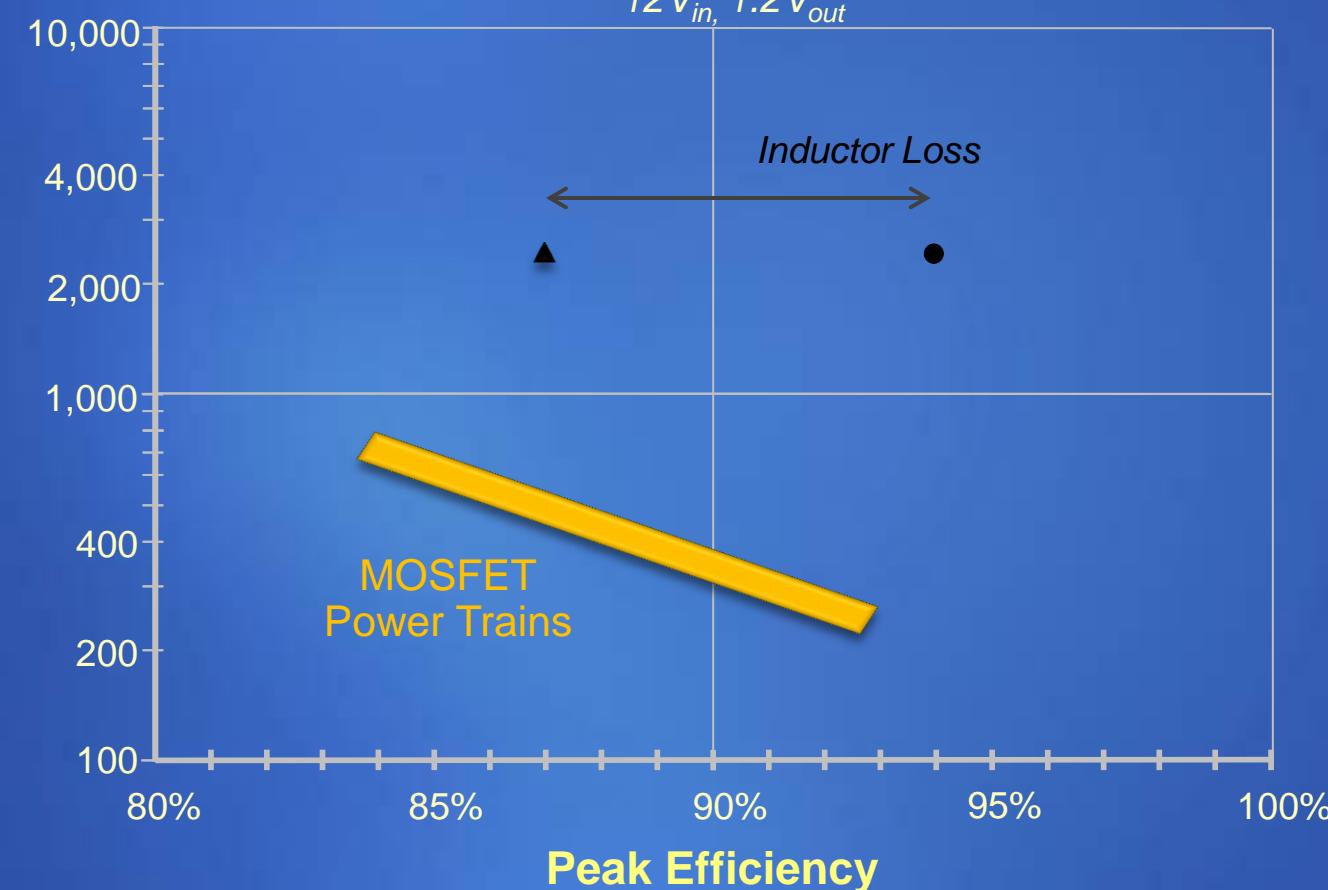
- Driver & FET
- Cbyp, Boot caps, gate caps, Schottky's



5x4x1mm QFN package
15A capability
1-5MHz

HIPS Performance

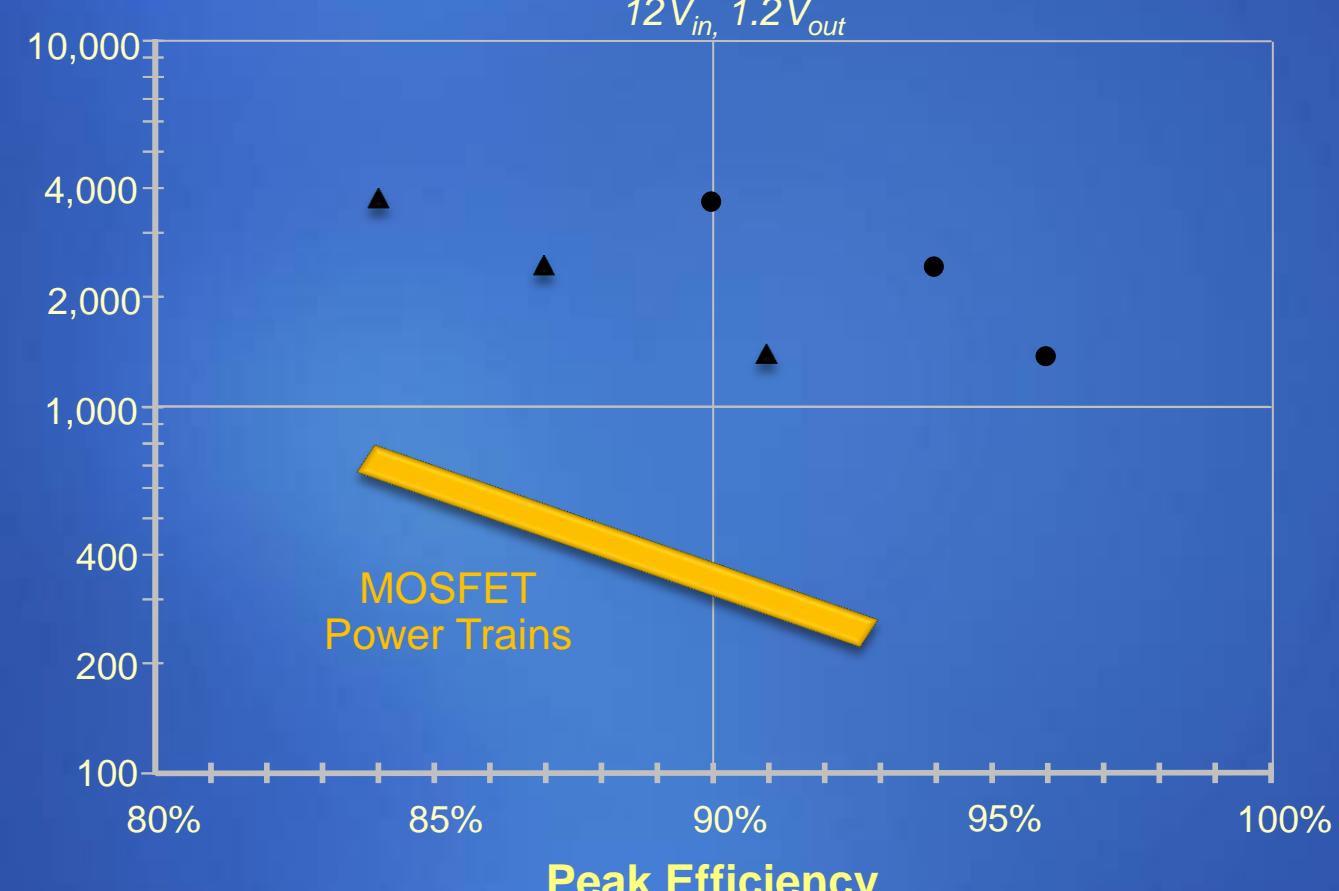
Power Train Density
(W/in³)



- Power Stage efficiency
- ▲ Power Train efficiency

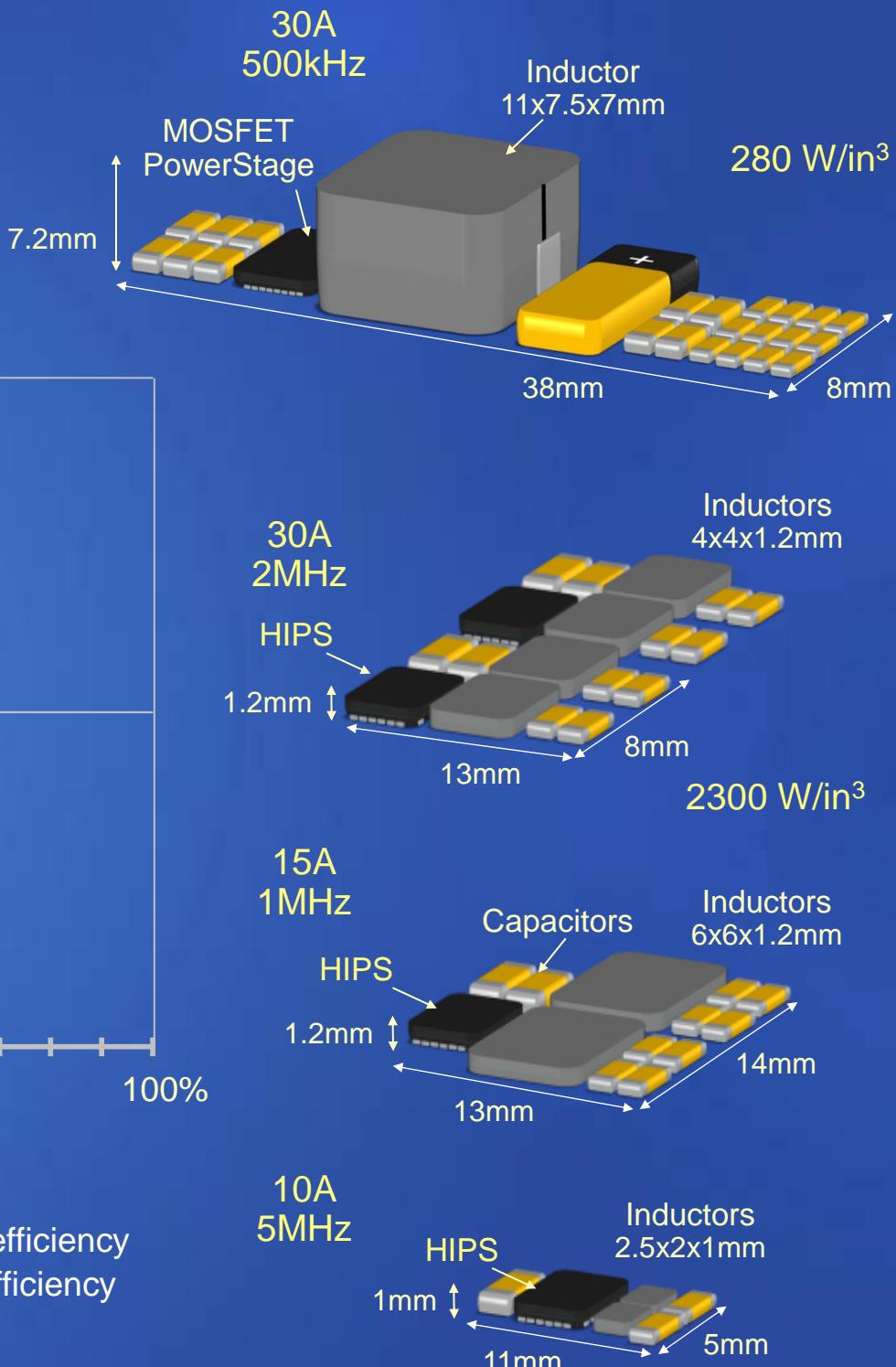
HIPS Performance

Power Train Density
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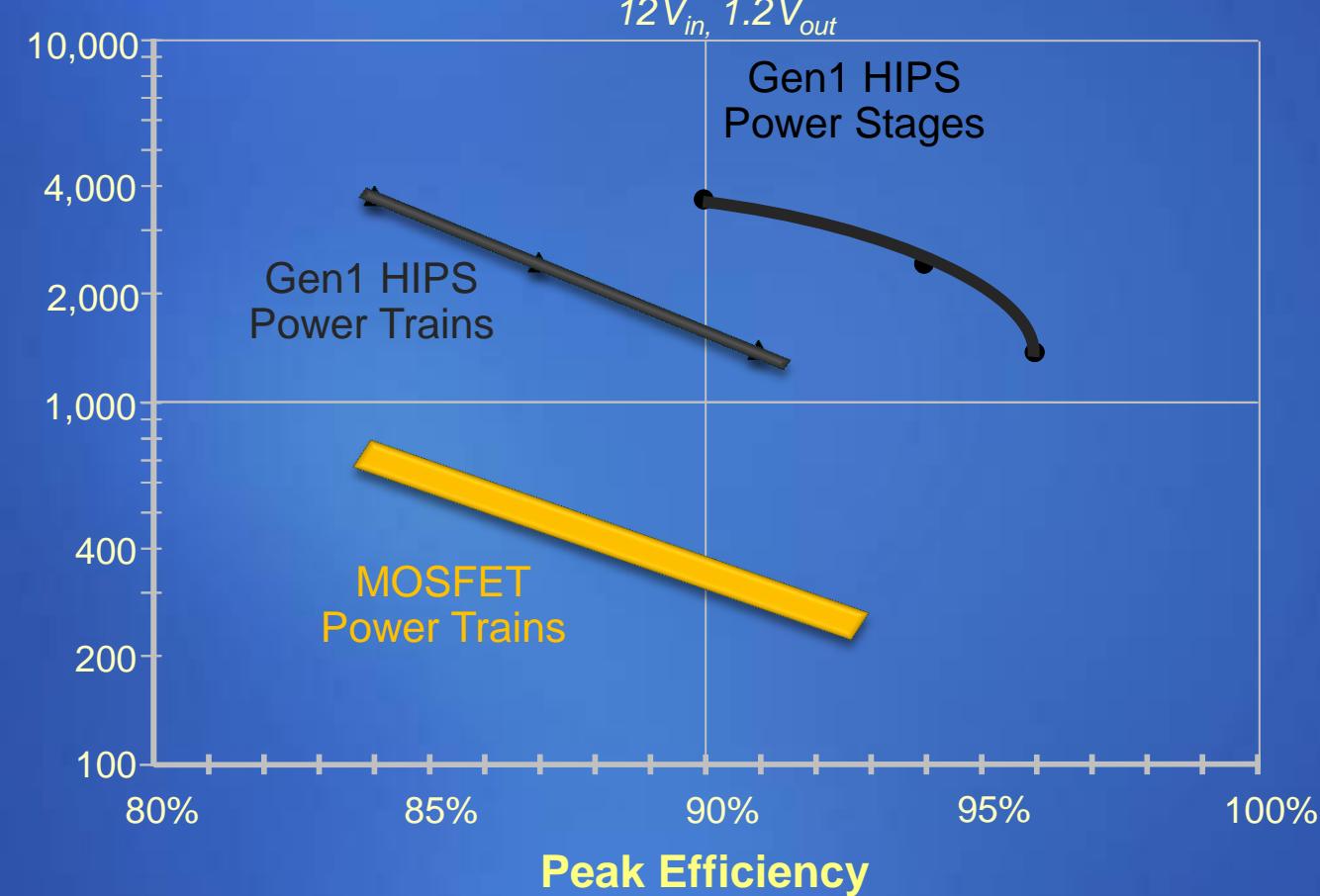
- Power Stage efficiency
- ▲ Power Train efficiency

APEC 2015

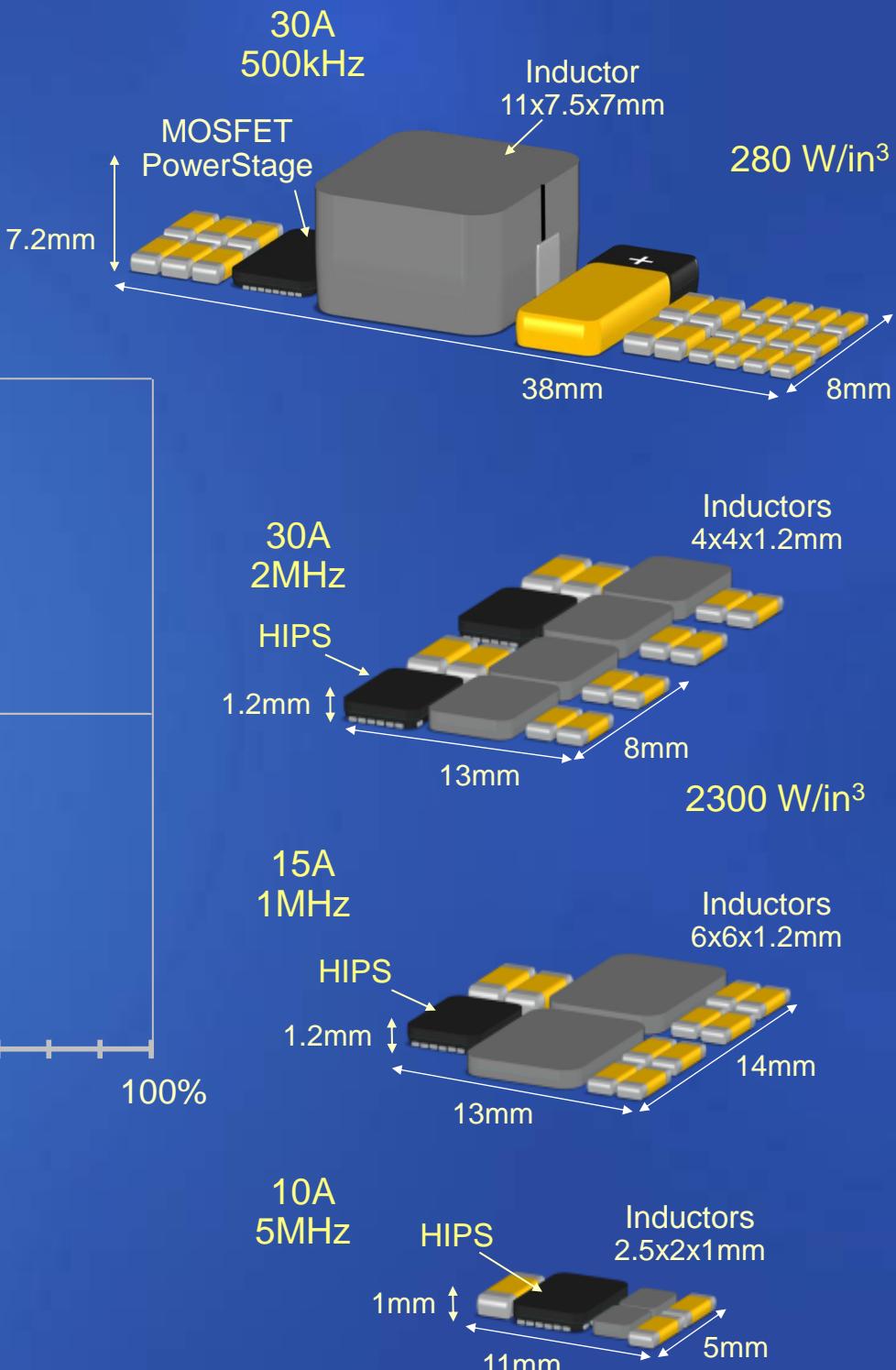


HIPS Performance

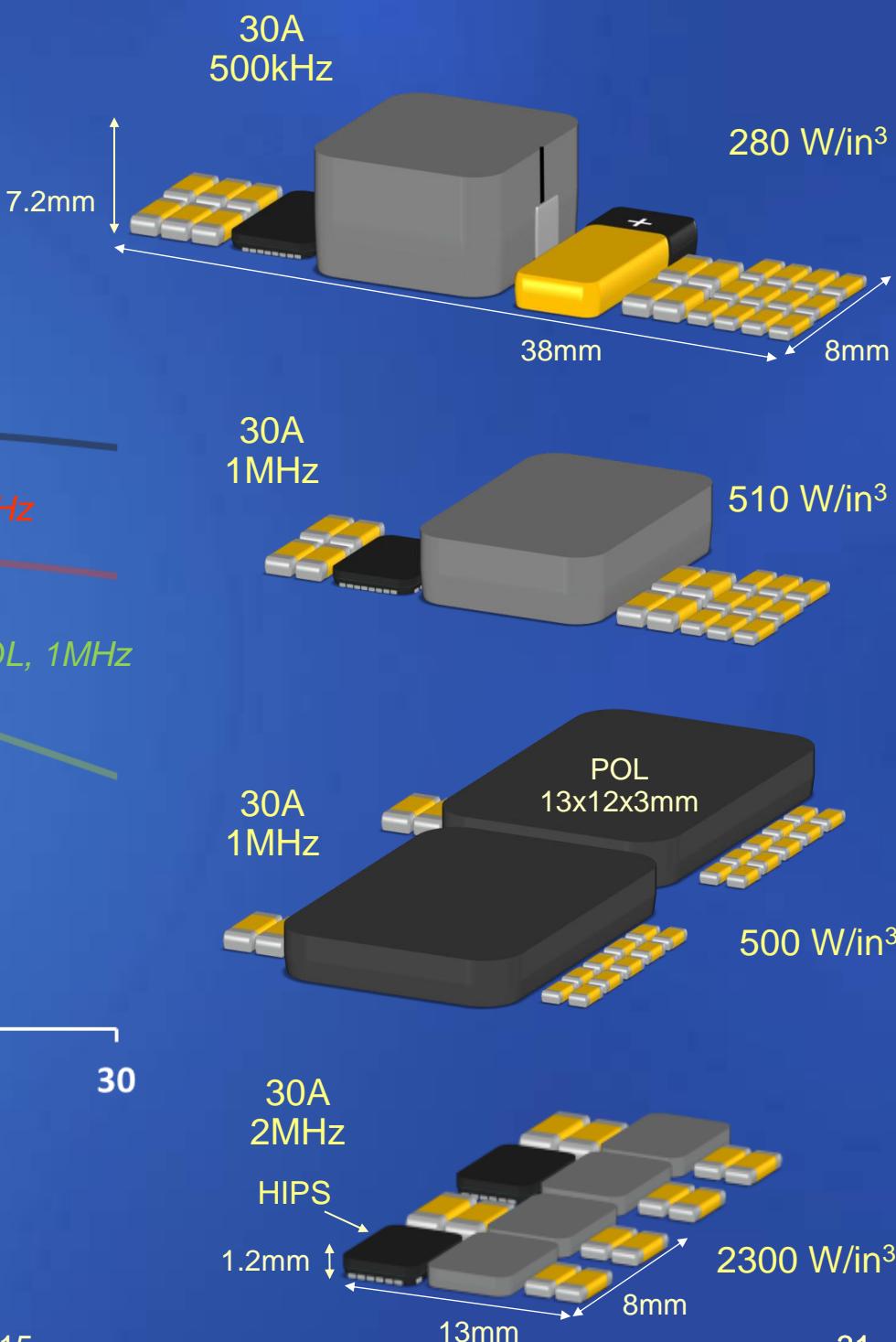
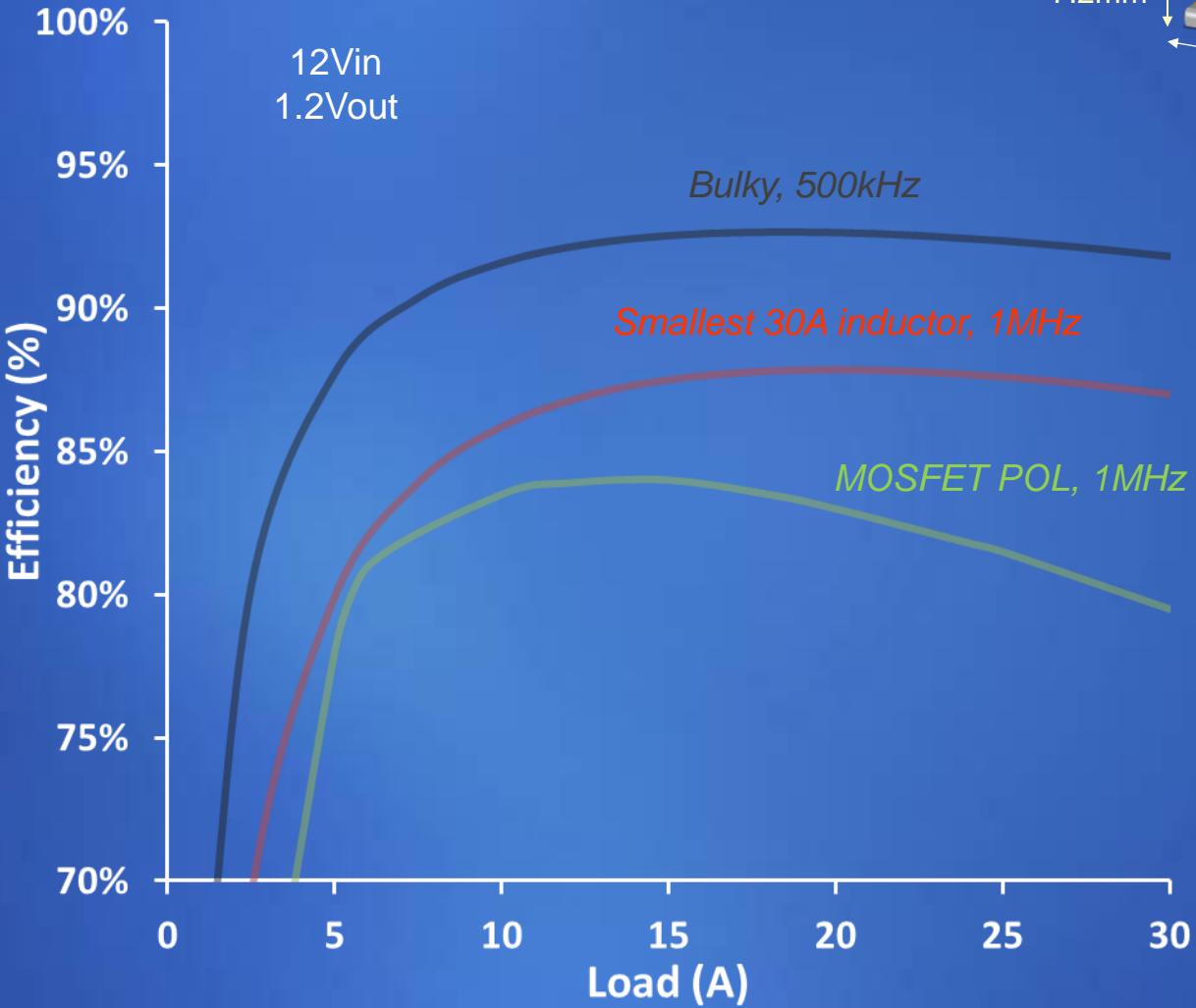
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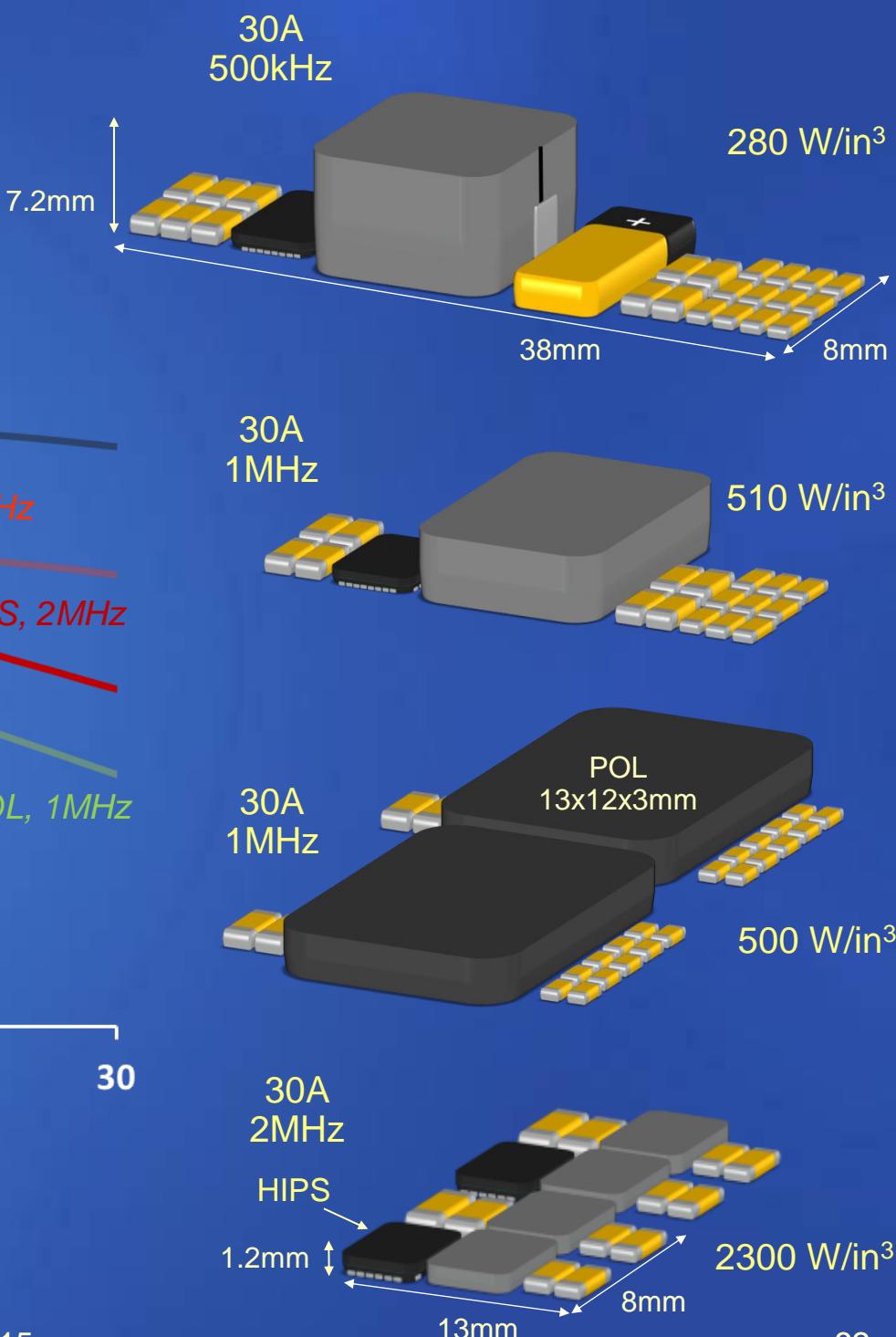
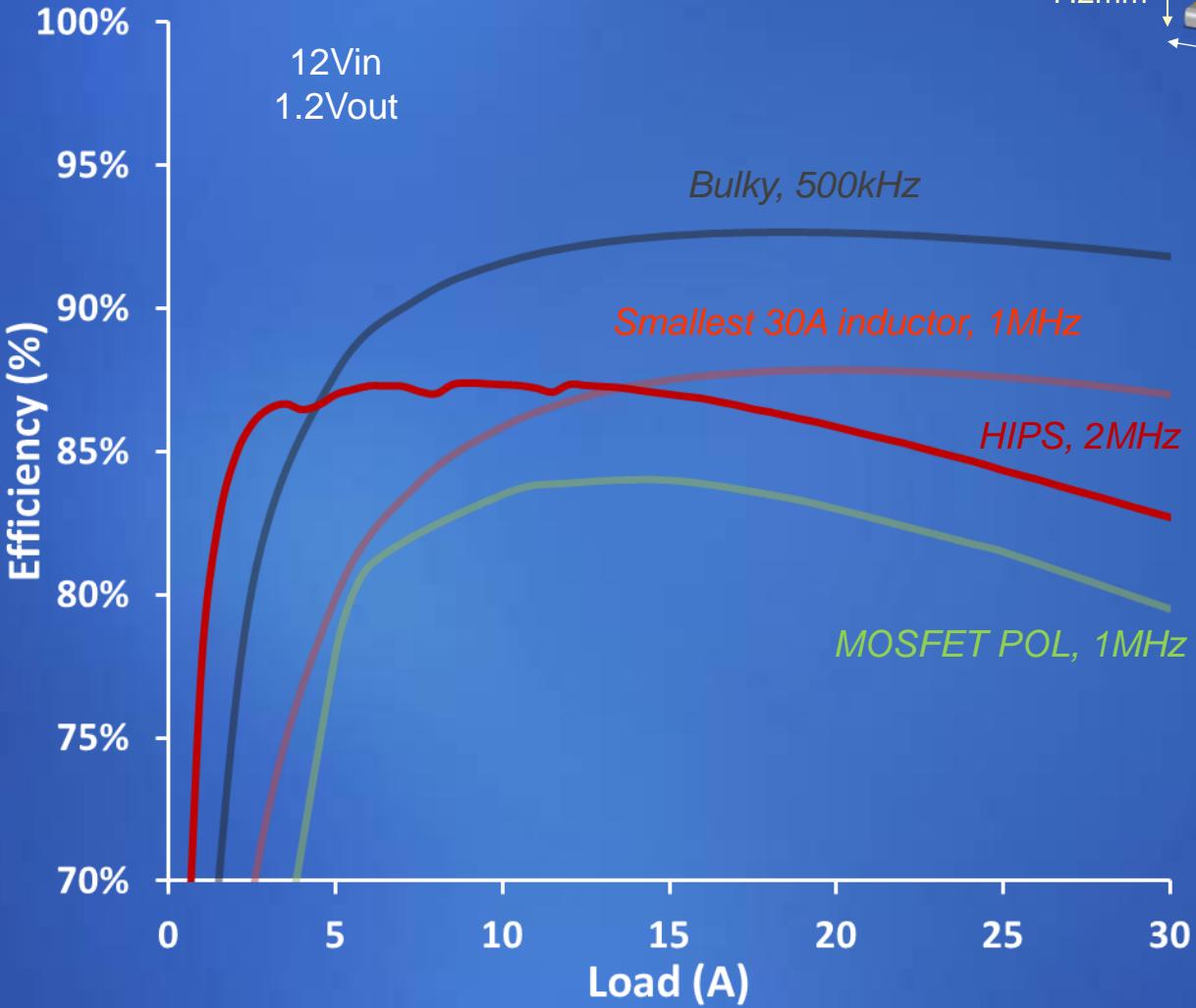
APEC 2015



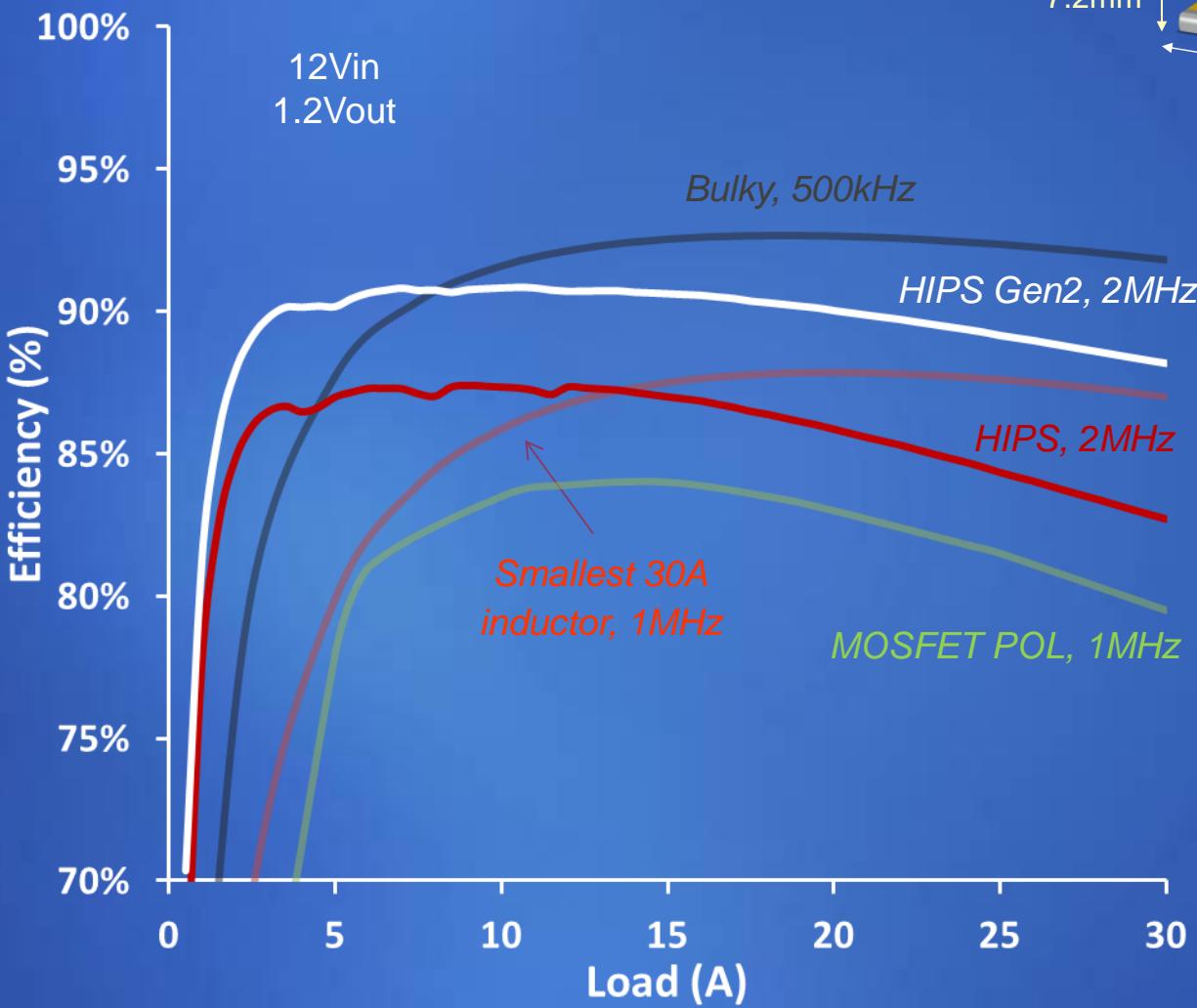
Efficiency Examination



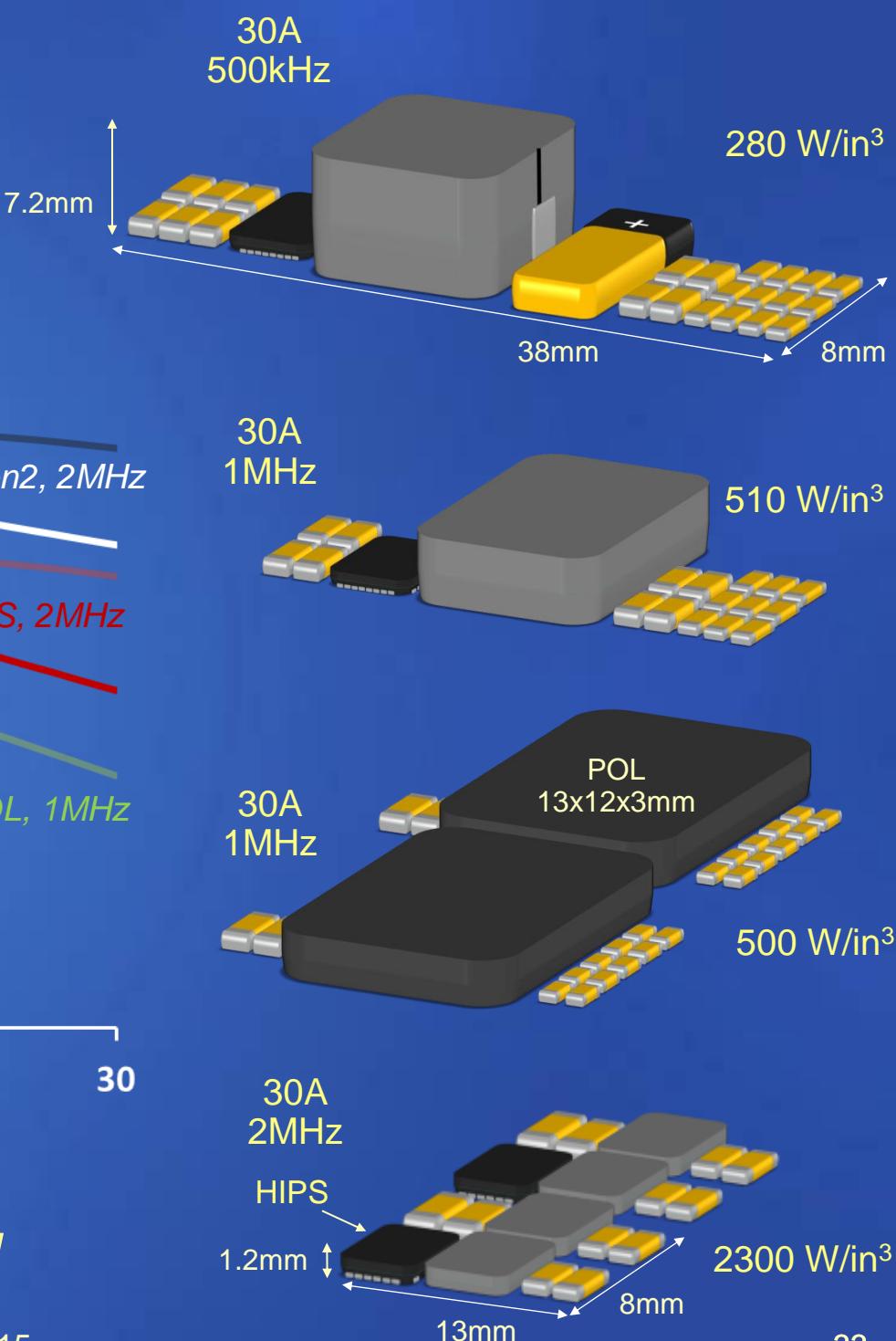
Efficiency Examination



Efficiency Examination

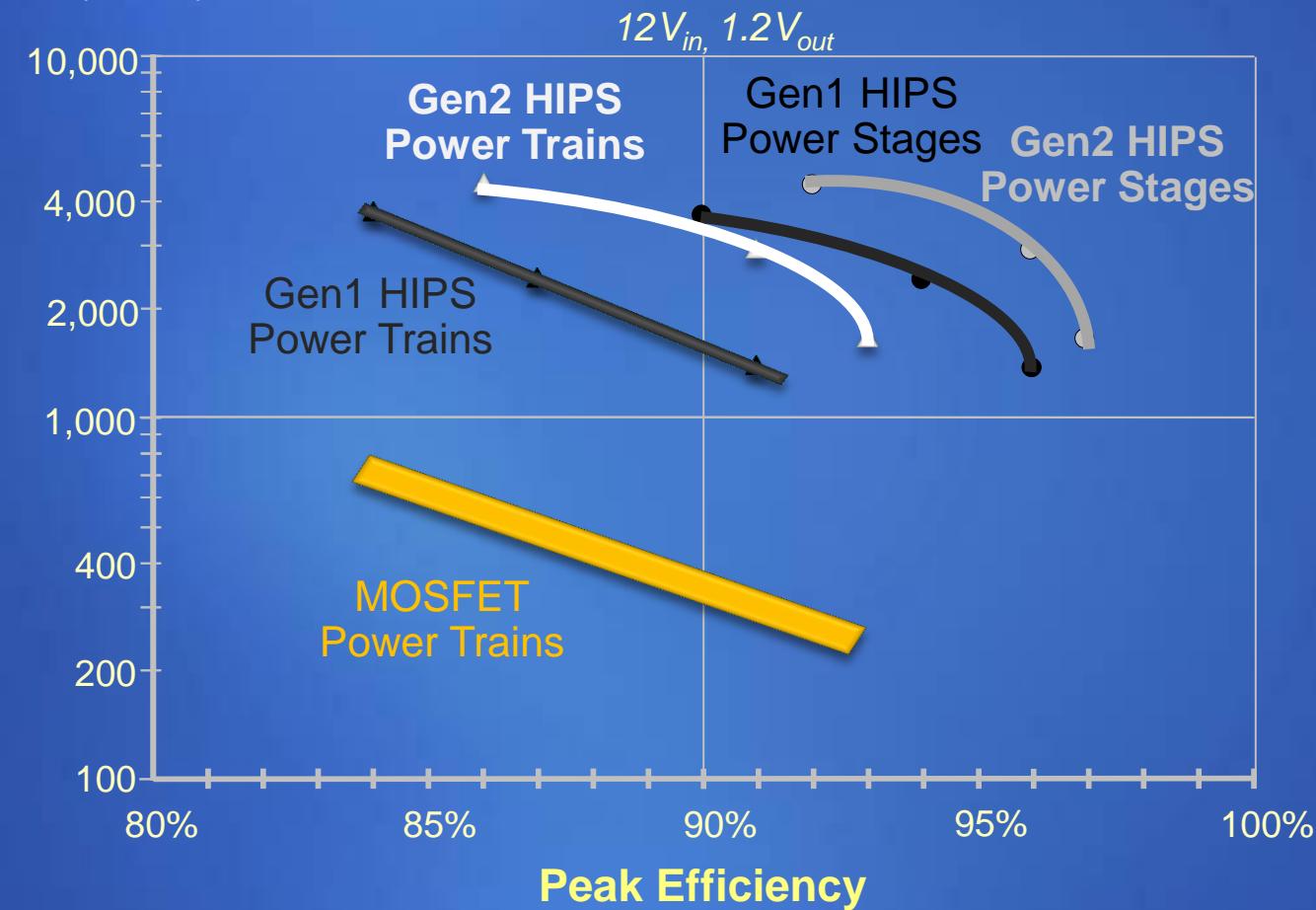


Gen2: Ron-A FOM halved
R_{dson}-Q_g FOM halved

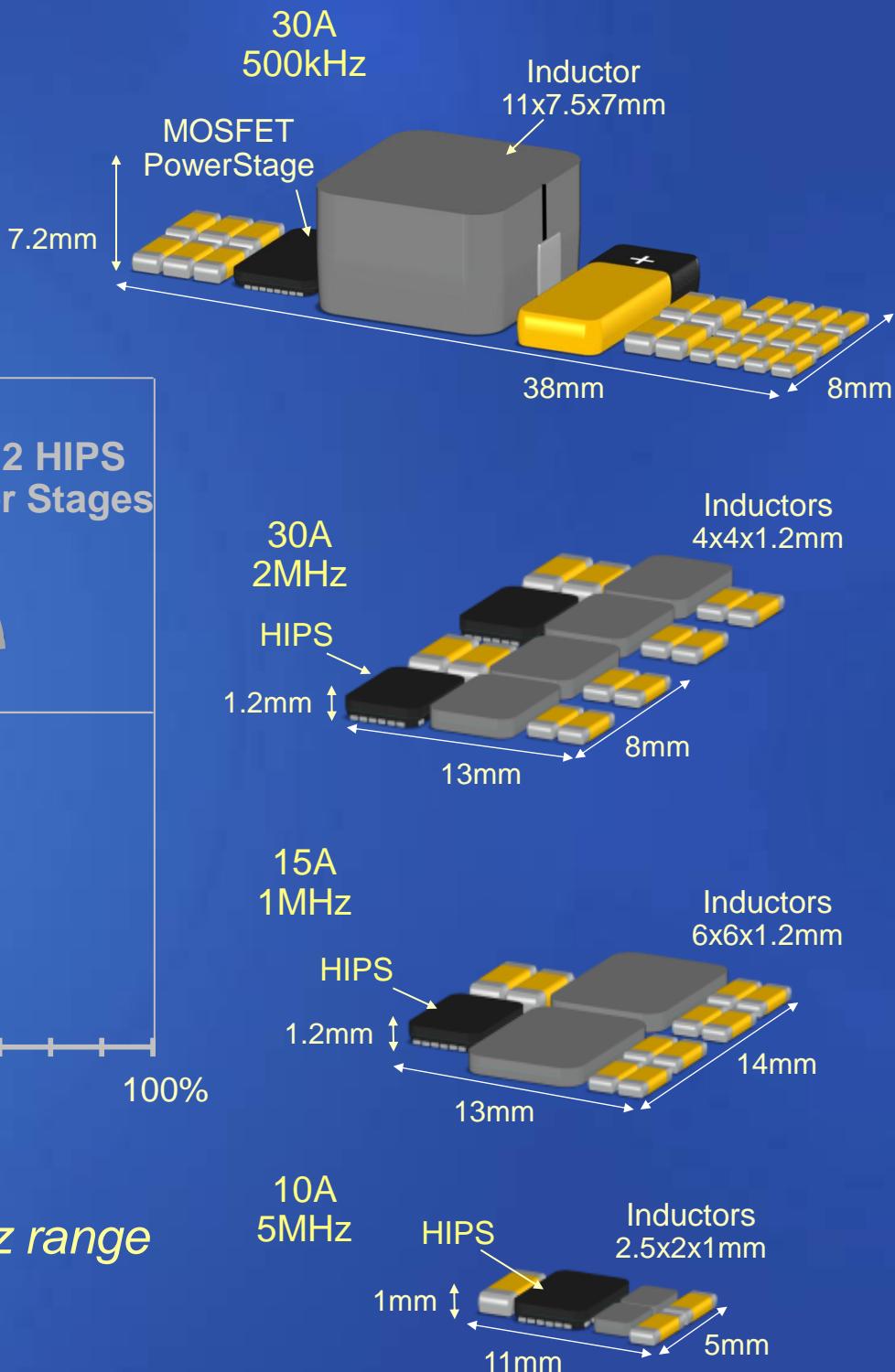


Gen2 HIPS Performance

Power Train Density
(W/in³)



*Examines Gen2 performance in 1-5MHz range
Can push to higher Fsw also*



Summary

- **HIPS Module**

- Integrate performance-critical components
- Dramatically increase Fsw to shrink the output filter

- **Embedded Die in Substrate (3D Packaging) can enable new levels of power density in 12Vin POLs**

- **Compound semiconductors required to fully realize benefits**

- GaAs is ideal for 12V input

- **Enable higher switching frequencies**

- Up to 5MHz is only a starting point → HIPS roadmap to 10's of MHz