Power Integration in Circuit Board

APEC 2015

AT&S

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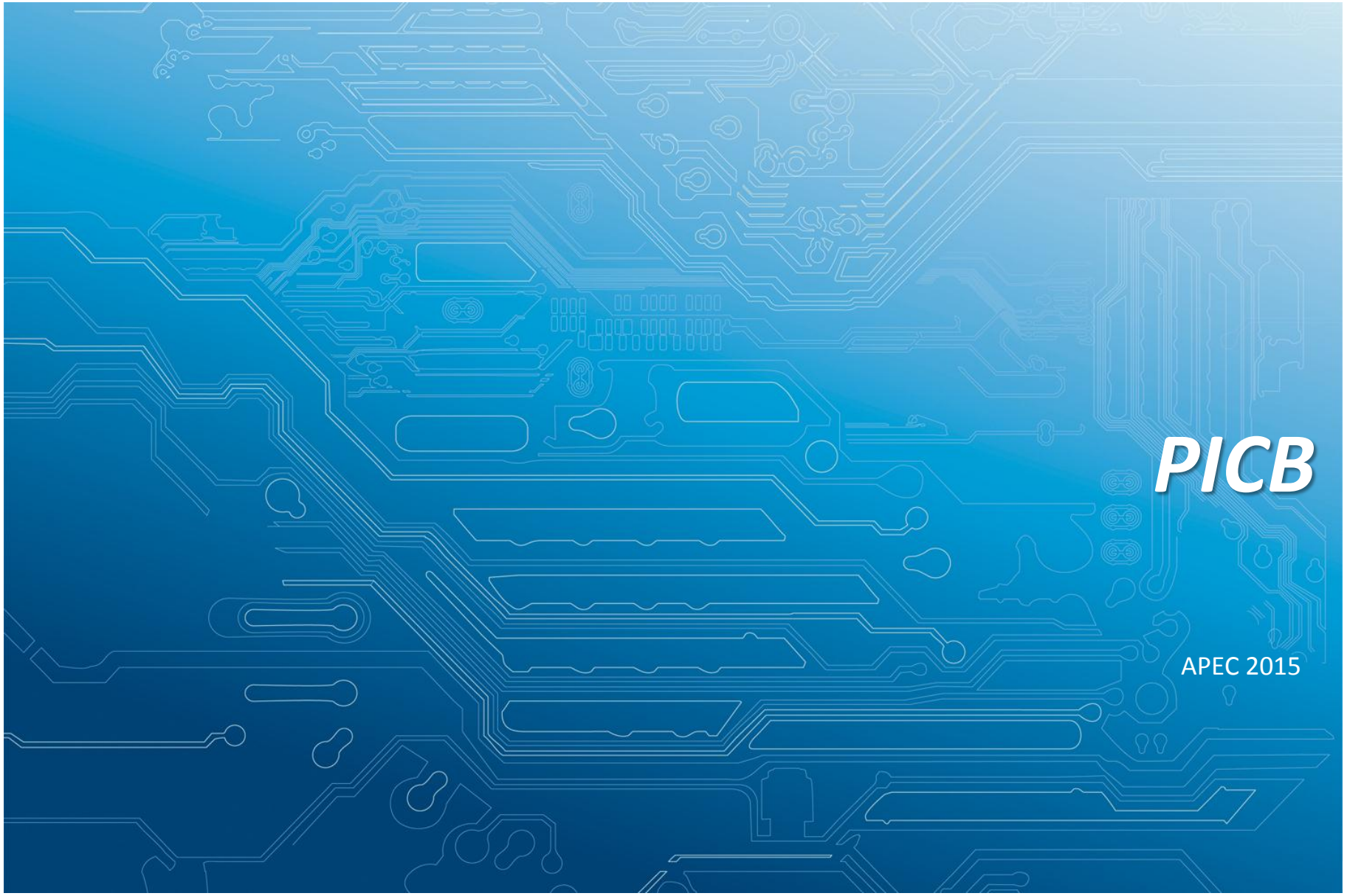

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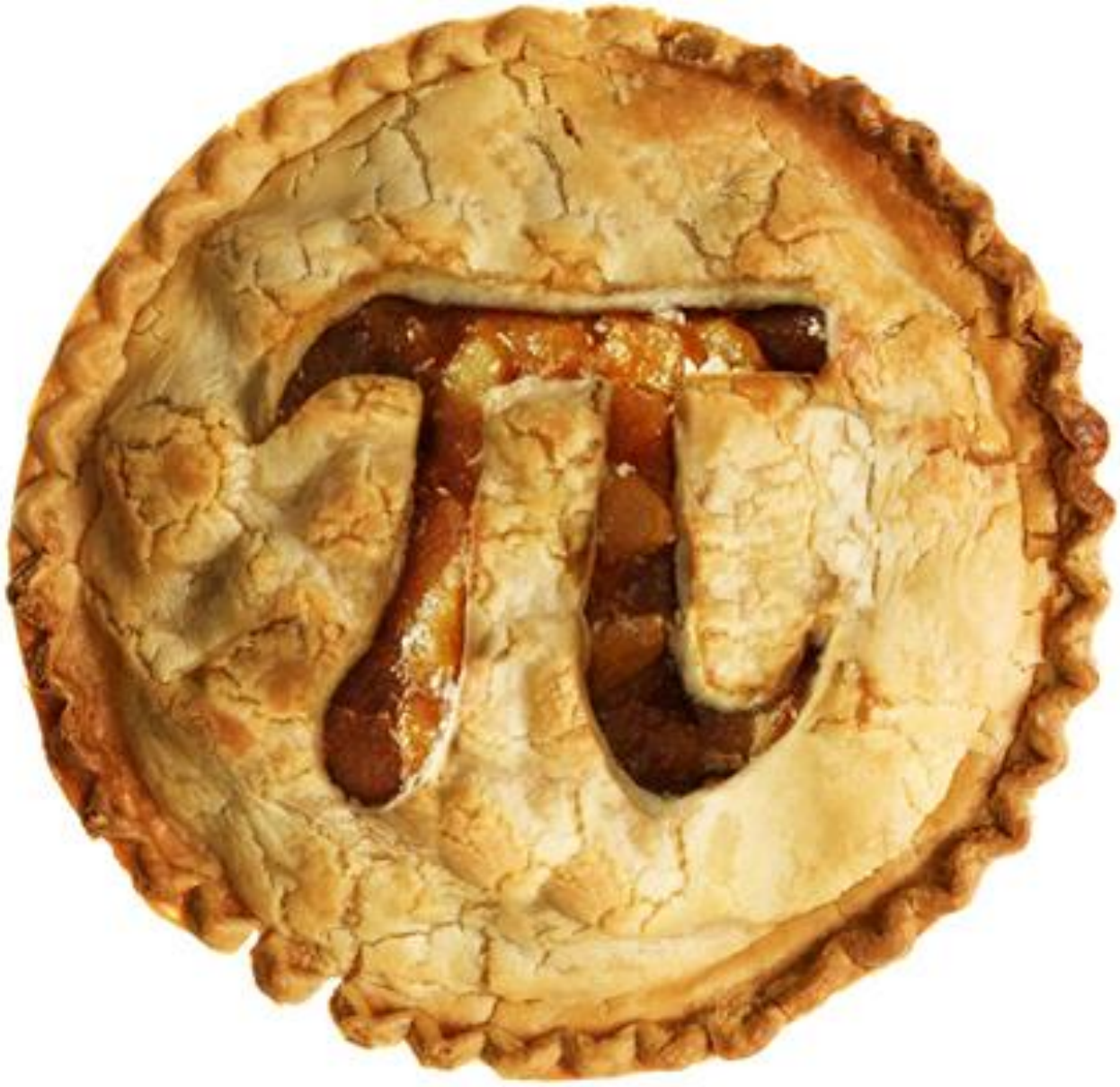

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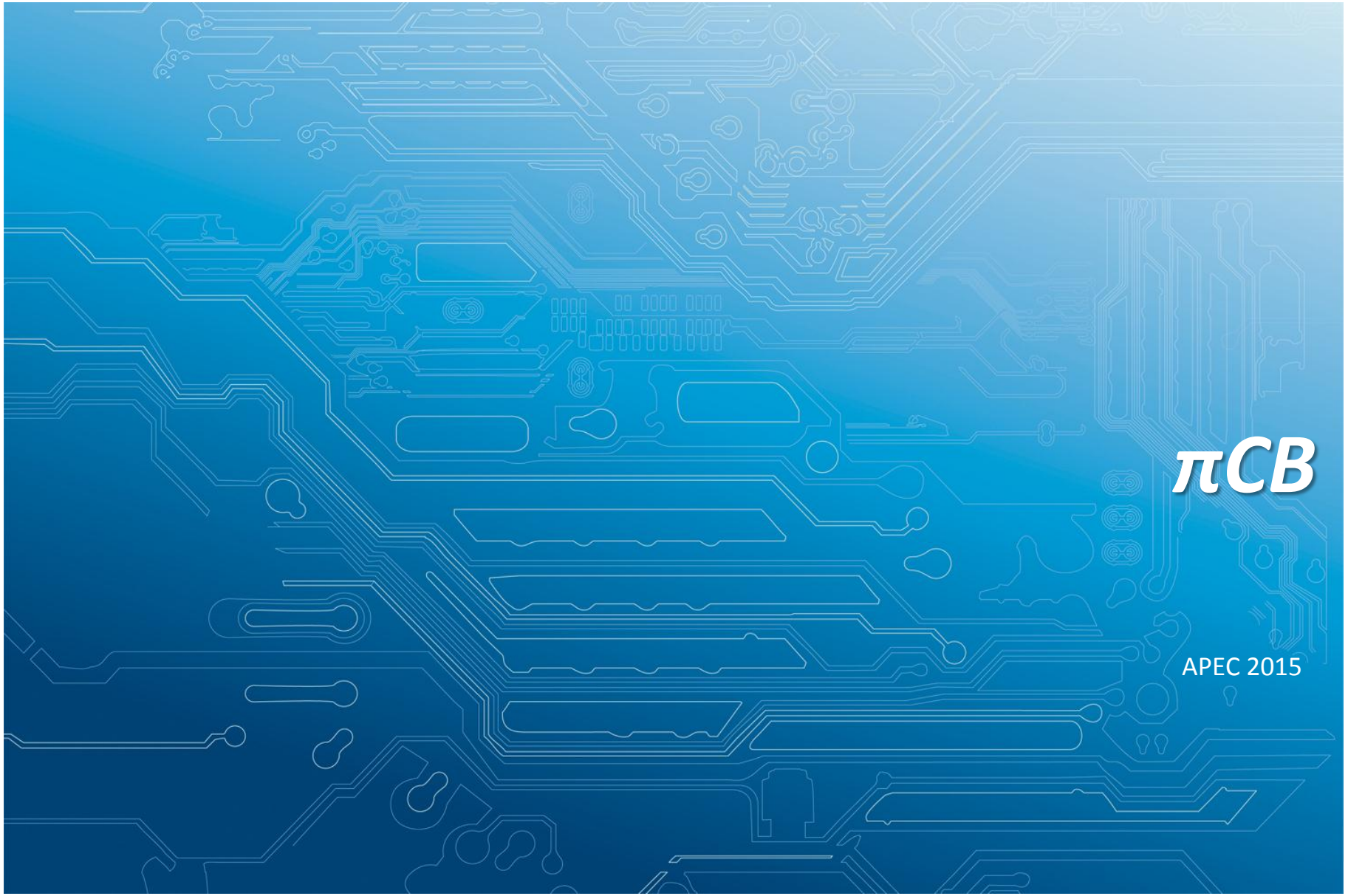

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Agenda

- Evolution of Embedding
- Die Connection
- Thermal Paths
- Comparison with QFN
- Conclusion

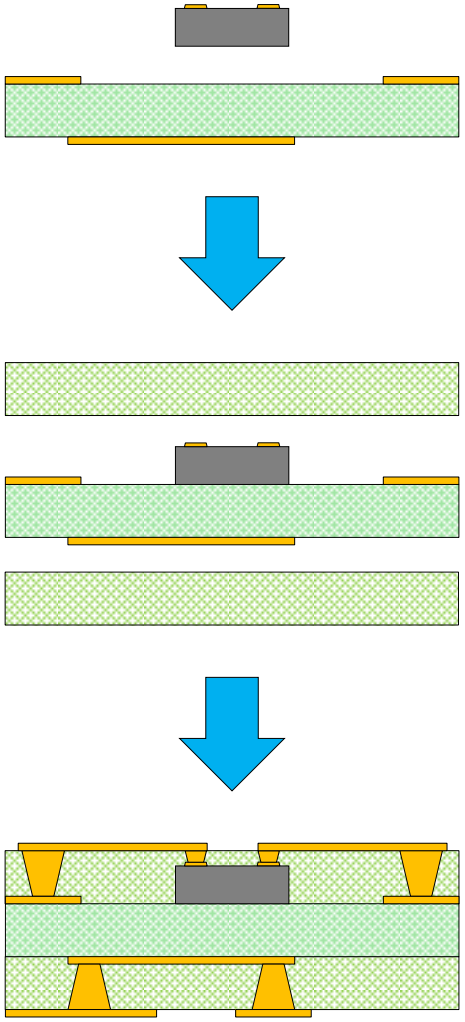
Evolution of Embedding

HIDING DIES (2005-2008)

- HIgh-Density INteGration of Dies Into Electronics Substrates

- Objective
  - Development of thin-die fine-pitch embedding

- Partners
  - AT&S
  - CWM
  - Datacon
  - IMEC
  - Nokia
  - Philips
  - TU Berlin



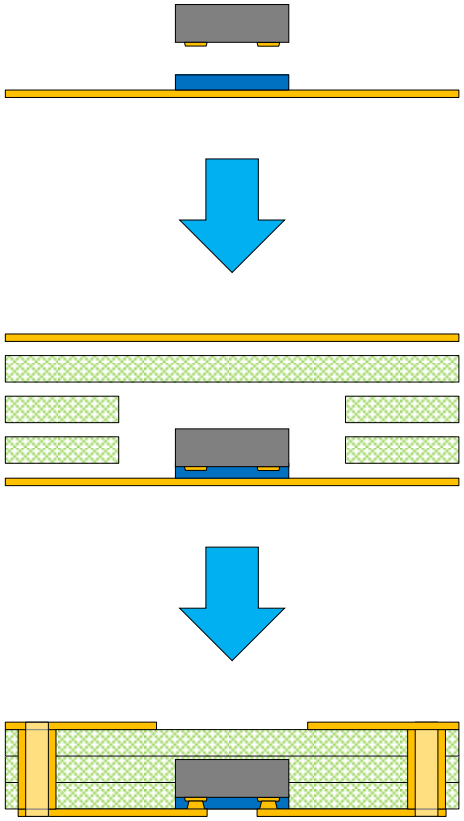
Evolution of Embedding

HERMES (2008-2011)

- High-Density Integration by Embedding Chips for Reduced Size Modules and Electronic Systems

- Objective
  - Industrialisation of embedding technology (ECP)

- Partners
  - Atotech
  - AT&S
  - Bosch
  - Circuit Foil
  - Fraunhofer IZM
  - IMEC
  - Infineon
  - Rood Technology
  - Siemens
  - Thales



Embedding by AT&S

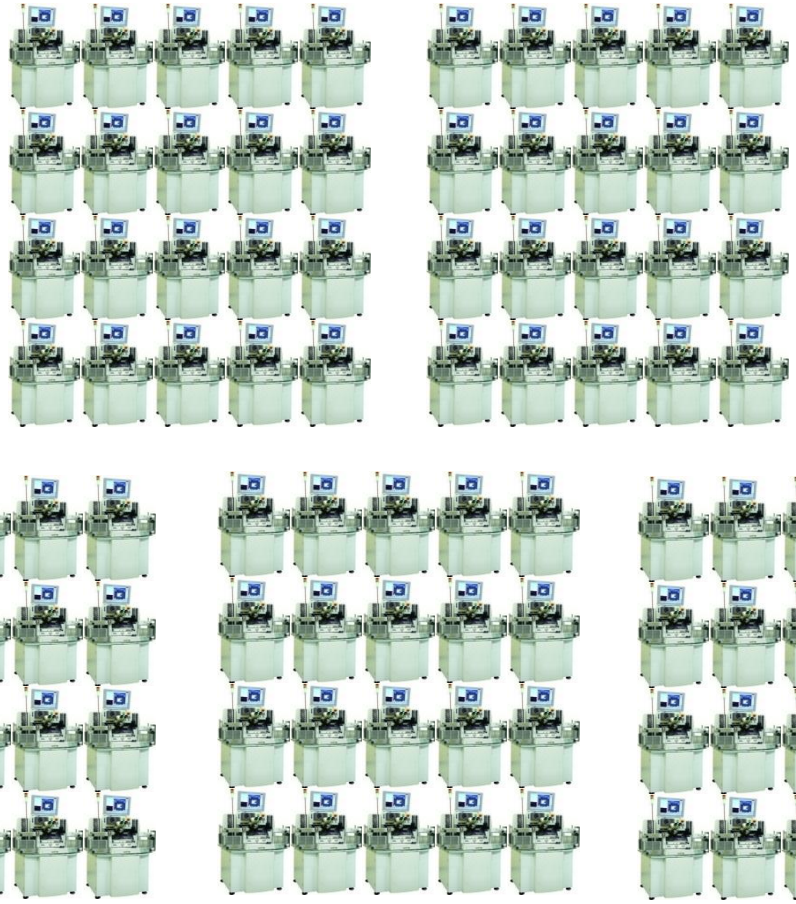
Component placement

- 1 ASM X4 equivalent to 80 die placers

Embedding by AT&S

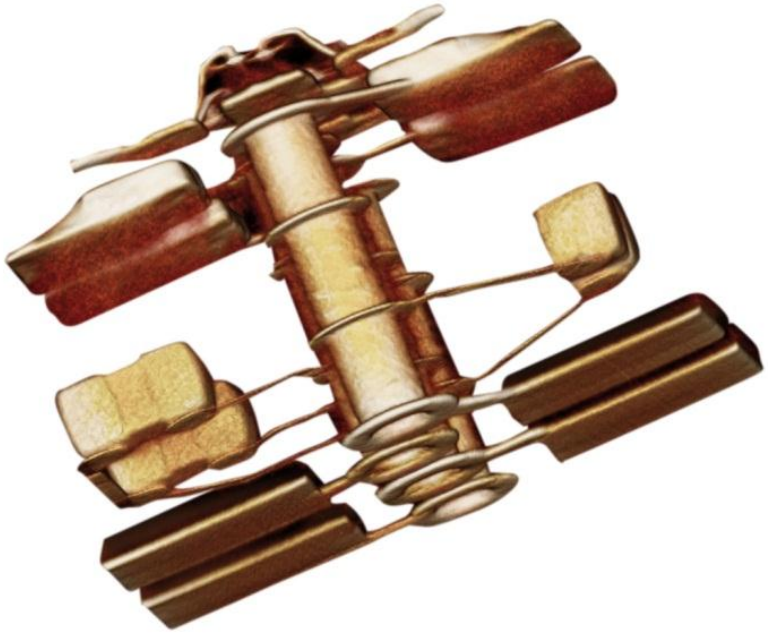
Interconnect formation

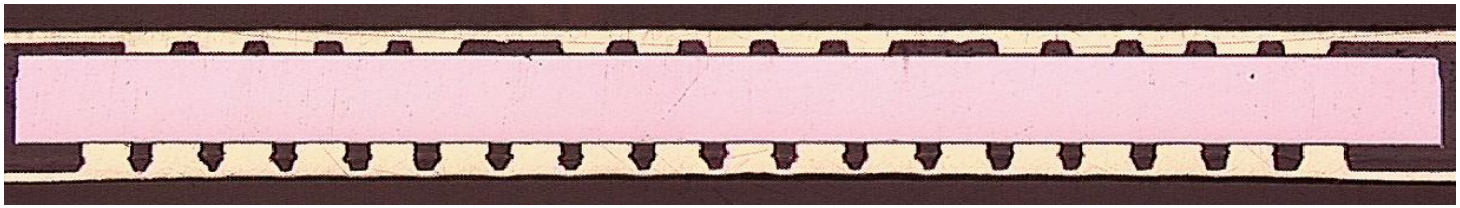
- 1 laser-drilling station equivalent to 100 wirebonders



Evolution of Embedding

HERMES (2008-2011)



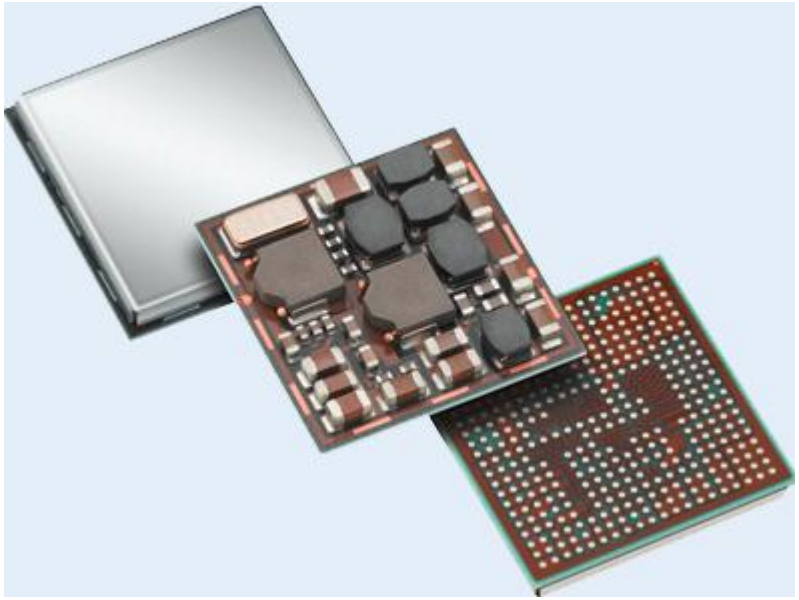


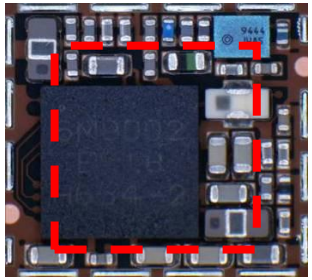
Other Embedding Technologies

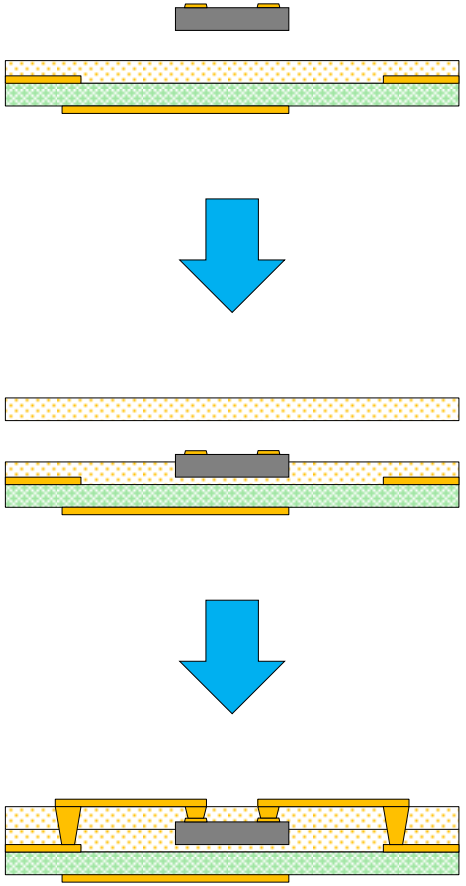
SESUB by TDK

- Semiconductor Embedded in SUBstrates

- Objective
  - Fine-pitch interconnection





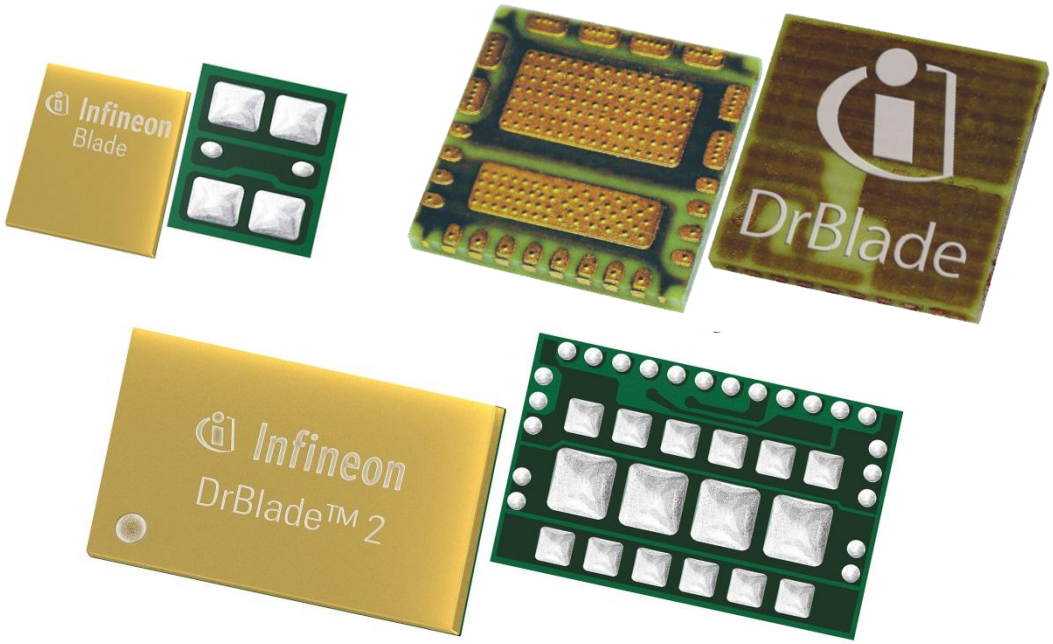


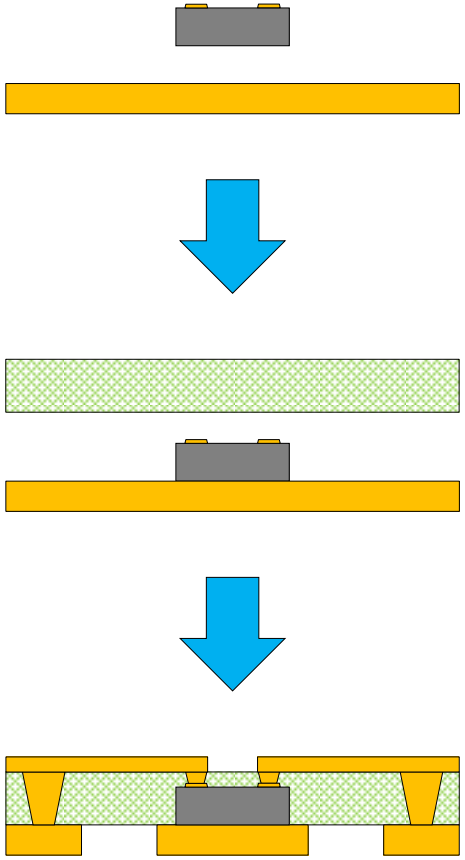
Other Embedding Technologies

BLADE by Infineon

- Evolution from HIDING DIES / HERMES

- Objective
  - Thermal management!!!





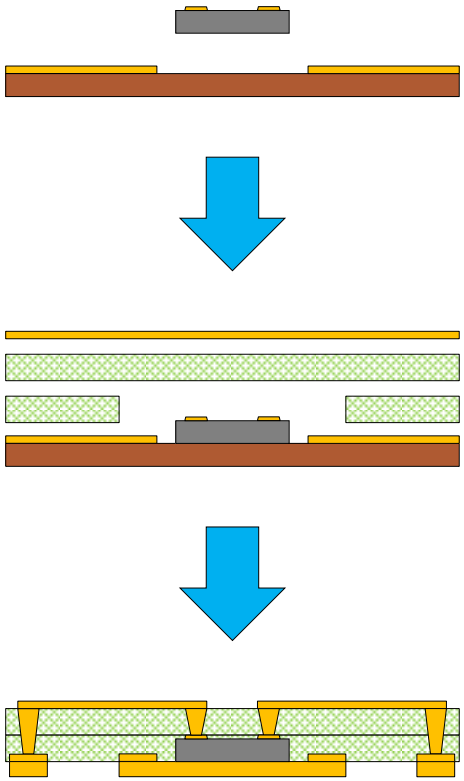
Evolution of Embedding

EmPower (2013-2016)

- Embedded Power components for electric vehicle applications

- Objective
  - Double-sided wafer plating
  - PARSEC embedding for high-power, high-reliability applications

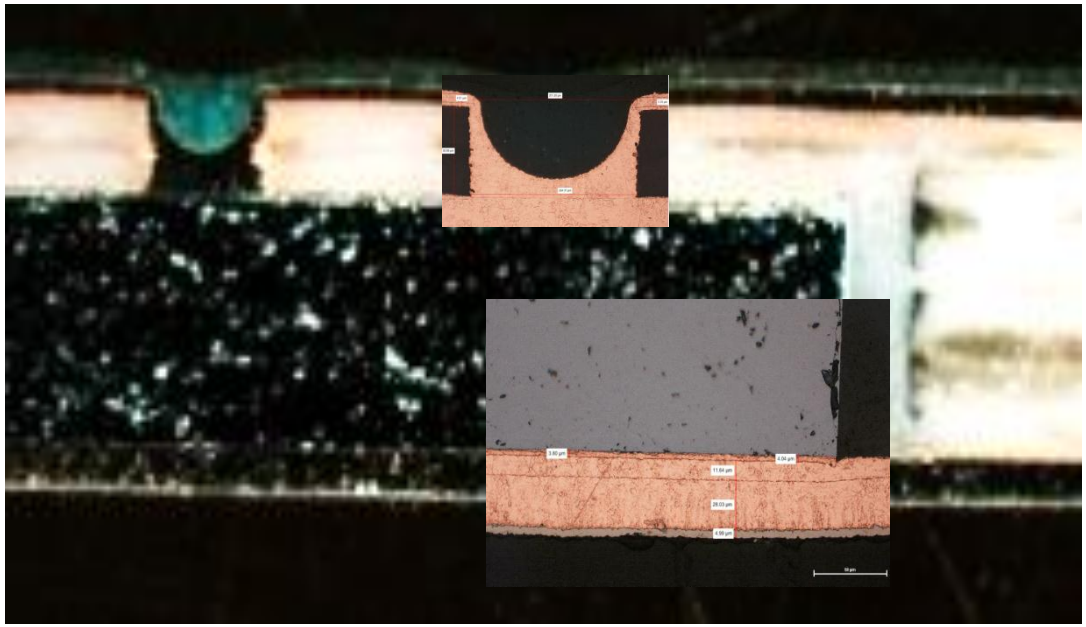
- Partners
  - Atotech
  - AT&S
  - Continental
  - ILFA
  - STMicroelectronics
  - TU Berlin
  - TU Wien

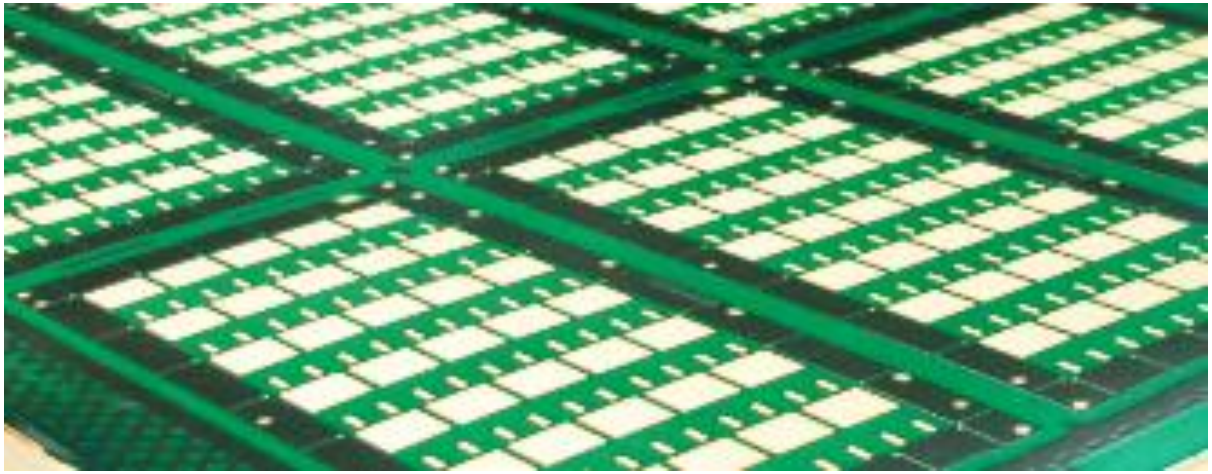


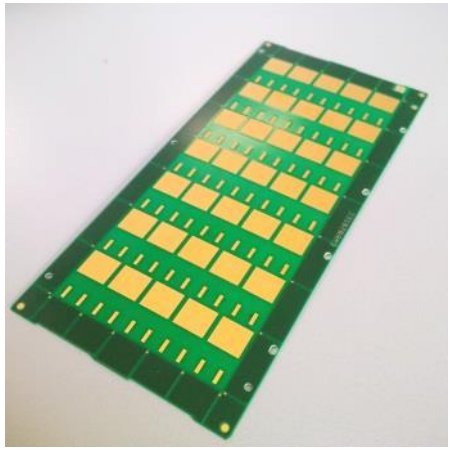
Evolution of Embedding

EmPower (2013-2016)

- First demonstrator
  - Power diode with DPAK footprint
- Reliability
  - Passed Reflow and MSL3 test
  - Other tests (incl. MSL1) ongoing

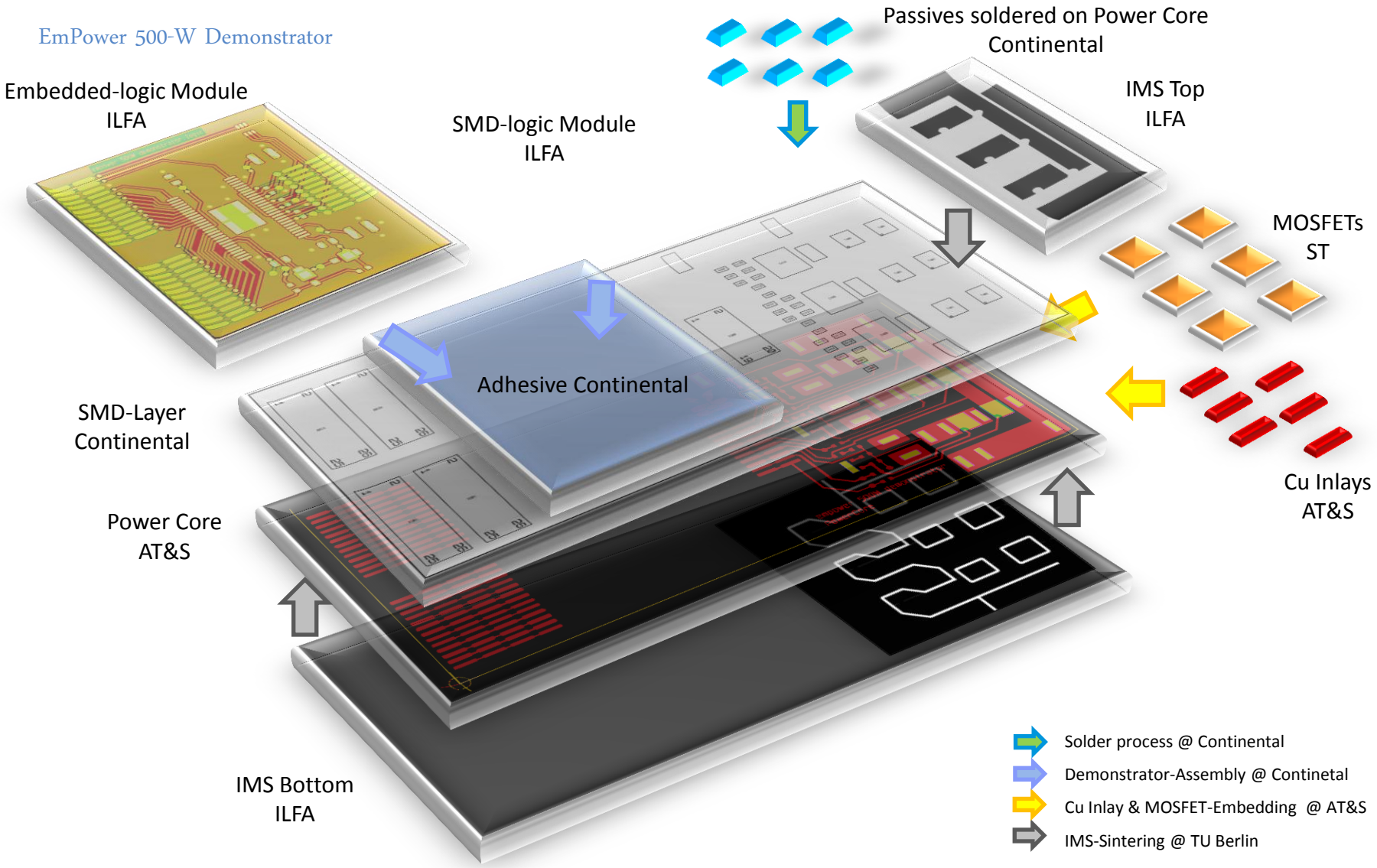






Evolution of Embedding

EmPower 500-W Demonstrator



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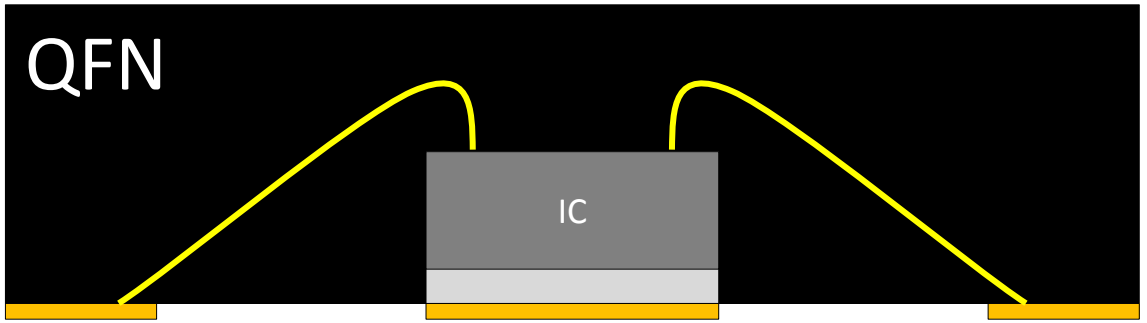
Die Connection

Thermal resistance

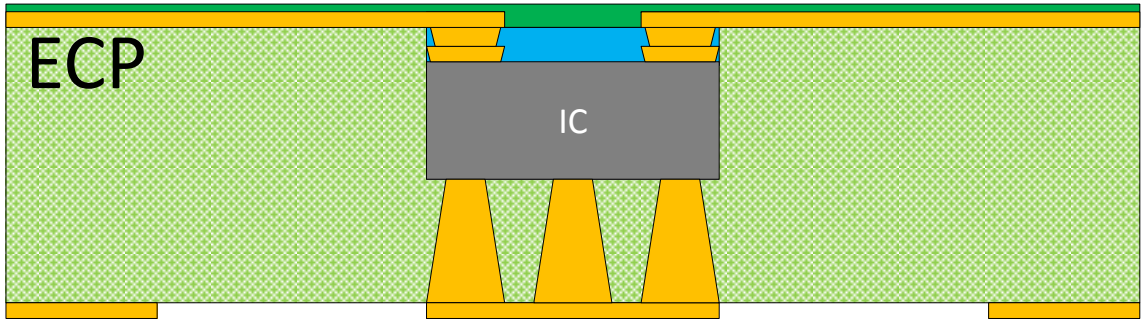


- Parameters
  - 4*4-mm die
  - 25-µm bondline
- DA material
  - Ag-loaded epoxy
    - Thermal conductivity @ 5 W/(m.K)
    - Thermal resistance @ 0.31 K/W
  - Solderpaste
    - Thermal conductivity @ 50 W/(m.K)
    - Thermal resistance @ 0.03 K/W
  - Sinter paste
    - Thermal conductivity @ 5 W/(m.K)
    - Thermal resistance @ 0.02 K/W

Die Connection

Thermal resistance

- Parameters
  - 4*4-mm die
  - 45-µm PP
  - Filled microvia diameter @ 130 µm
  - Microvia pitch @ 250 µm



- Materials
  - PP
    - Thermal conductivity @ 0.6 W/(m.K)
  - Cu
    - Thermal conductivity @ 400 W/(m.K)
  - Thermal resistance @ 0.03 K/W

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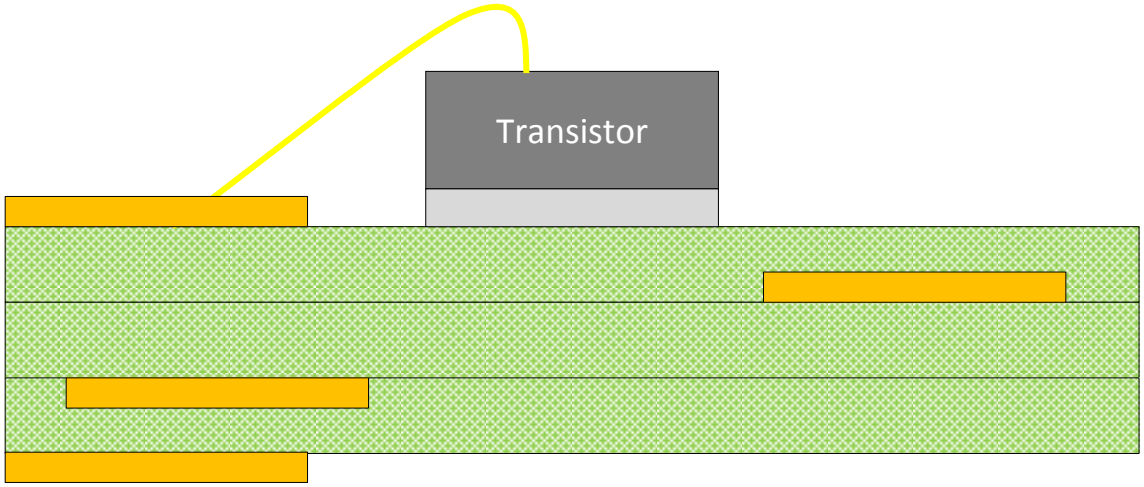
Thermal Path

Board-level integration

- Power transistor on FR4
  - 4*4-mm die
  - 4L
  - 500-µm PCB thickness

- Thermal resistance @ 403 K/W

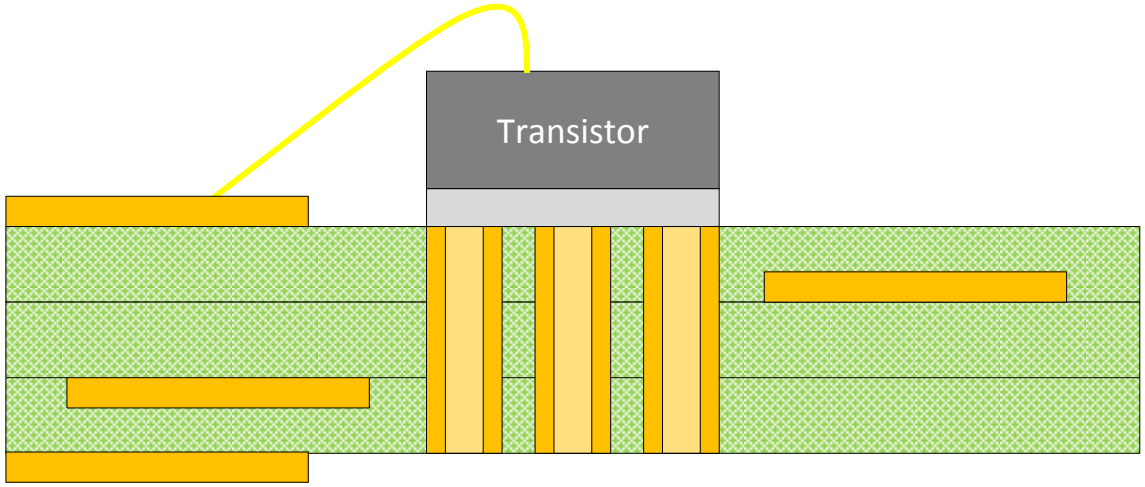


Thermal Path

Board-level integration

- Power transistor on FR4 with thermal vias
  - 4*4-mm die
  - 4L
  - 500-µm PCB thickness
  - 500-µm PTHs

- Thermal resistance @ 4 K/W

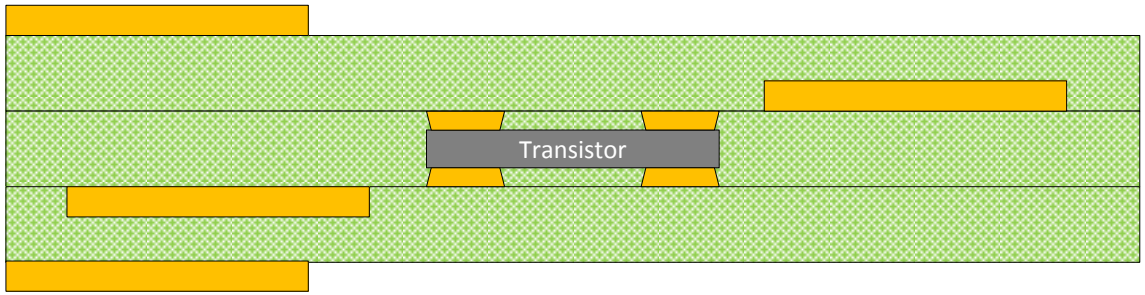


Thermal Path

Board-level integration

- Power transistor in FR4
  - 4*4-mm die
  - 4L
  - 500-µm PCB thickness

- Thermal resistance @ 19 K/W

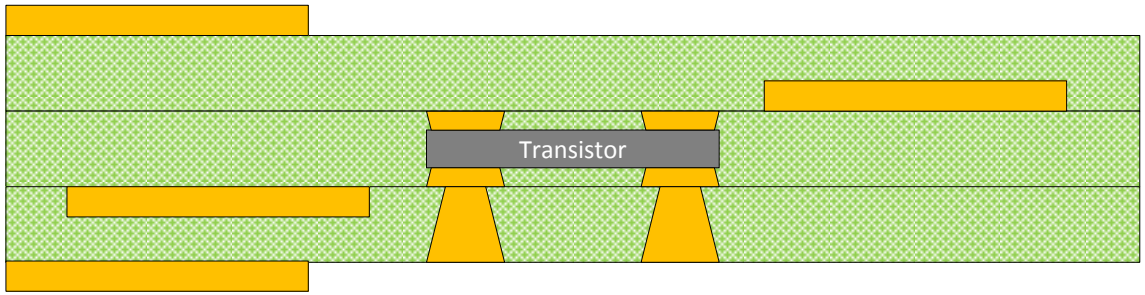


Thermal Path

Board-level integration

- Power transistor in FR4 with thermal vias
  - 4*4-mm die
  - 4L
  - 500-µm PCB thickness
  - 130-µm filled microvias

- Thermal resistance @ 0.03 K/W



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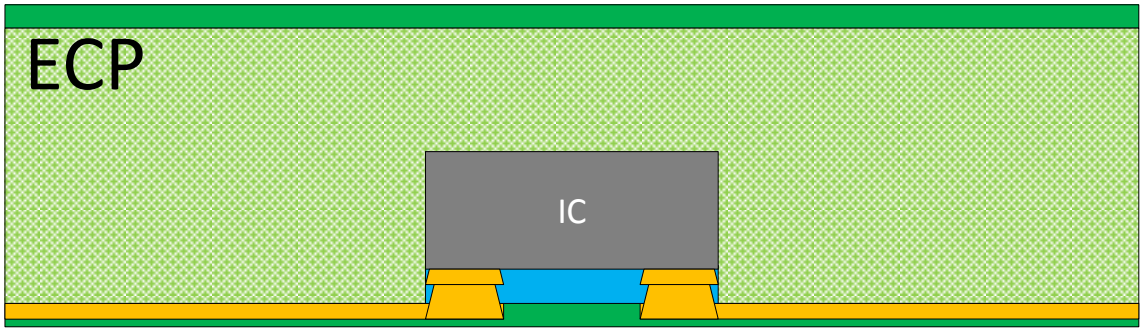
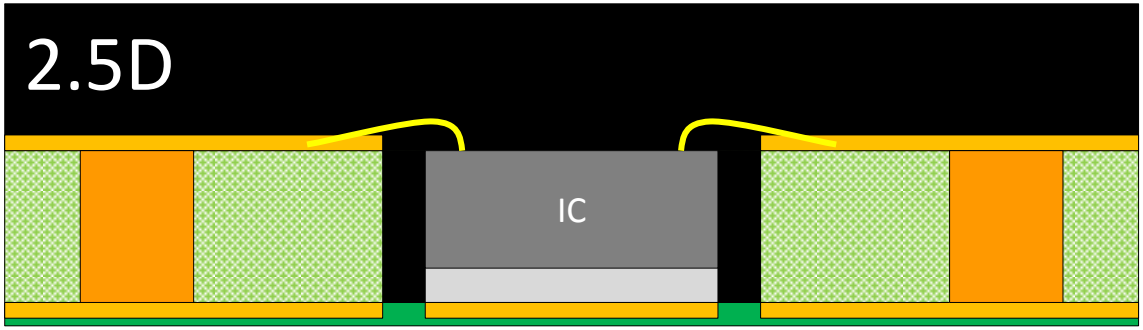
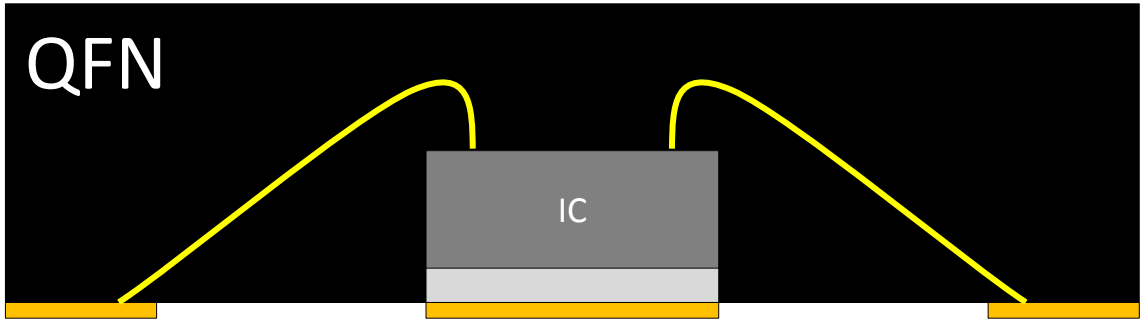
Comparison with QFN

Structure







Comparison with QFN

AT&S

Characteristics

		ECP	2.5D	QFN
Die size (mm)		2*2		
Package size (mm)		4*4		
Number of I/Os		12		
Die thickness (µm)		150	300	300
Package thickness		300	500	700
Interconnect		Via	WB	WB
Thermal resistance (K/W)	θ_{j-top}	30	94	120
	$\theta_{j-bottom}$	0.7	0.6	0.7
	$\theta_{j-ambient}$	0.7	0.6	0.7
Interconnect inductance (nH)		0.7	0.7	1.0
Cost		+	+	0
Testability		QFN footprint		

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Conclusion

Embedding

- Improved performance for limited to neutral cost increase
  - Size reduction
  - Improved thermal resistance
  - Improved electrical characteristics
- Maturing and reliable technology
- New variations under development for power applications

⇨ Will power make PCB exciting?

Thank you for your attention!

Questions?

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