Emerging high-performance and low-cost power packaging solutions with nanoscale capacitors and inductors

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& Heraeus Inc., Leverkusen, Germany.
GT-PRC is innovating power packaging technologies with advanced components and 3D integration,

and also creating an industry ecosystem of material suppliers, component manufacturers and end-users:

- **Capacitors in consumer power modules:**
  - Silicon-integrated nanoscale tantalum capacitors

- **High-temperature and high-voltage capacitors with:**
  - Porous copper electrodes
  - Nanoscale inorganic – organic hybrid dielectrics

- **Capacitors and inductors in integrated voltage regulators:**
  - Low-cost polymer nanomagnetic inductors
  - Panel-scale inductor and capacitor integration

- **Shielding:**
  - Nanolayered structures for performance beyond copper
Packaging R&D at GT-PRC

- RF (WLAN & LTE)
- Integrated Voltage Regulator
- 5G & mm-Wave
- 2.5D Glass Interposer
- Radar, Camera with GFO
- High-power & Reliability
- High-temp Material & Reliability
- Computing and Communications Electronic Products & Assembly
- Sensing Electronic Interconnections
- Design - Substrates - Passives - Interconnections - Electronic Properties & Assembly
Why Collaborate With Georgia Tech PRC

- No. 1 Academic Leader in IC & Systems Packaging
- Technical Vision Consistent with Market Needs
- Co-development of Panel-based Glass Packaging with 50 Global Researchers, Developers, Manufacturers and users
- Explore and Develop Advanced Systems Packaging Technologies Beyond Industry’s 3-year Horizon
- Seamless from R&D, Prototype, and Tech Transfer Enabling Commercialization
- Track Record of Technology Breakthroughs
- Only 300mm Cleanroom Panel Facility in the Academic World
- > 50 Person Co-development Team: Full-time Researchers, Manufacturing Industry Partners, Graduate Engineers, Faculty and On-campus Industry Engineers
- Leverage: $8M/100k
## Global Industry Partners in Co-development

### NORTH AMERICA
- Corning – Glass
- Dow Chemical – Polymers
- Advantech – Deposition
- Coherent – Laser
- ESI – Laser
- K&S – TCB Bonder
- MKS – Plasma Etching
- Rudolph – Lithography
- SavanSys – Cost Model
- Tango – PVD Tools
- Veeco – Cleaning
- QualiTau – Assembly
- AMD – 2.5D
- AVX – Passives
- GlobalFoundries
- Intel – Digital
- Johnson Battery – User
- Qualcomm – 5G, Fan-out, RF
- TE – Opto
- TI – Passives

### EUROPE
- HC Starck – Capacitors
- Schott – Glass
- Atotech – Plating
- Suss – LaserVia
- Xyztec – Assembly
- TDK-Epcos – RF
- Valeo – ADAS

### ASIA
- Orbotech – Metrology
- PacTech – Assembly
- JCET – Bumping
- Gigalane – RF
- Valeo – ADAS
- TSMC – User

### JAPAN
- Ajinomoto – Dry Film
- Asahi Glass – Glass
- JSR – Low-loss Polymer
- Nitto Denko – Magnetics
- Panasonic – Low-loss Polymer
- Taiyo Ink – Photopolymer
- TOK – Photopolymer
- Asahi Glass – TPV
- Disco – Dicing
- Hitachi Metals – 2.5D
- NGK/NTK – 2.5D
- Shinko – 2.5D
- Namics – Underfill
- WALTS – Substrate
- Murata – RF

### Materials
- Corning – Glass
- Dow Chemical – Polymers
- Advantech – Deposition
- Coherent – Laser
- ESI – Laser
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### Tools
- HC Starck – Capacitors
- Schott – Glass
- Atotech – Plating
- Suss – LaserVia
- Xyztec – Assembly
- TDK-Epcos – RF
- Valeo – ADAS

### Substrates
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- Shinko – 2.5D
- Namics – Underfill
- WALTS – Substrate
- Murata – RF

### Users
- TSMC – User
Technology Trends and Drivers

- Higher bus voltage to suppress losses
- Integrated power conversion with the load:
  - Suppress $I^2R$ losses
  - Minimize the need for decoupling capacitors
- Integration of storage elements – should not offset the benefits or interconnection losses
- Better Power distribution network designs

![Discrete Modules Diagram]

- Short PDN path
- Low impedance
- Less voltage drop
- Less voltage variation
- Less de-caps
- More efficiency

![Component Density Diagram]
Large-Area Capacitor and Inductor Integration

- Both capacitors and inductors are made as large-area free-standing films
  - Can be pre-tested for yield and performance
- Laminated onto substrate or wafer
- Or diced into IPDs and embedded or surface-assembled

Capacitor Layer at panel scale

Inductor layers at panel scale

Large panel LC integration process
Glass Panel Capacitor and Inductor Integration

- Glass to support high-density fine-line wiring on large 510 x 510 panel manufacturing

- Currently ongoing, in collaboration with component manufacturers and end-user companies
Capacitors in Consumer Power Modules

Silicon-integrated nanoscale tantalum capacitors
Capacitor Integration in Consumer Power Modules

Discrete power module

Integrated power module
Wafer Integration of Ta Film Capacitors

Component Manufacturer (Ex. AVX)

Ta foil

Anode

Cathode

Semiconductor Wafer

Integrated capacitor on a chip
Bulky Ta Vs Ta Film Capacitors

<table>
<thead>
<tr>
<th>Thickness: 500 microns</th>
<th>Thickness: 75 microns</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 200 micron conducting path</td>
<td>• 50 micron conducting path</td>
</tr>
<tr>
<td>• CP/Carbon/Silver paste</td>
<td>• Minimal interfaces;</td>
</tr>
<tr>
<td>• Molded in lead-frame</td>
<td>• Direct metallization of CP with Cu/Au</td>
</tr>
<tr>
<td>• (extra pkg volume)</td>
<td>• (Minimal packaging volume)</td>
</tr>
<tr>
<td>• 100 milliohms x microfarad</td>
<td>• 20-50 milliohms x microfarad</td>
</tr>
<tr>
<td>• 1-5 MHz</td>
<td>• &gt;10 MHz</td>
</tr>
</tbody>
</table>
## Competitiveness of GT capacitors

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Si deep trench</th>
<th>Discrete MLCC</th>
<th>Foil Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component thickness (µm)</td>
<td>~ 200-300</td>
<td>200</td>
<td>75</td>
</tr>
<tr>
<td>Capacitance (µF/mm²)</td>
<td>1</td>
<td>2-3</td>
<td>1</td>
</tr>
<tr>
<td>Frequency (MHz)</td>
<td>-</td>
<td>150</td>
<td>1 - 150</td>
</tr>
<tr>
<td>Leakage current (µA/µF)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

![Diagram of Si deep trench and discrete MLCC capacitors]
Capacitor Integration scheme

I. Passivation

II. Lamination onto substrate

III. Planarization

IV. Via drill

V. Metallization
   a. Desmearing
   b. Electroless Cu seed layer
   c. Photolithography
   d. Electroplating
Demo. of Capacitor Integration

Anode
- Printed tantalum with low-temperature sintering

Dielectric
- Anodization for conformal oxide growth with controlled thickness

Component Integration on silicon
- Thin-film design for high volumetric density and frequency stability
- Lamination onto silicon with short copper interconnections

Cathode
- Cathode dipping process for low ESR and high capacitance density
- Lift-off process for easy cathode patterning
Capacitor Reliability

65°C/95%RH for 500 hours

- Capacitance response to frequency similar before and after exposure to elevated temperatures and moisture
- Improved ESR after testing
- Near-hermetic seal that removes need for casing

65°C/95%RH for 1000 hours

- Capacitance response to frequency similar before and after exposure to elevated temperatures and moisture
- Improved ESR after testing
- Near-hermetic seal that removes need for casing

- 1.15 µF/mm² at 1 MHz
- 1.34 µF/mm² at 1 MHz

- 1.19 µF/mm² at 1 MHz
- 1.09 µF/mm² at 1 MHz

- 80 kA-8V
- 200 nm passivation

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Manufacturing Ecosystem for Silicon-Integrated Foil Capacitors

Component Manufacturer (Ex. AVX)
Ta foil

H.C. Starck

Heraeus

Power modules with passive-active integration

Texas Instruments

IC

CAPACITOR

INDUCTOR

Texas Instruments

AVX

Anode

Cathode

Cathode

Anode

Wafer or substrate
High-temperature and high-voltage capacitors with nanoscale hybrid dielectrics
## High-Temperature and High-Voltage Capacitors

**AMS’ metallized polymer film capacitors**

- 700 V; 625 A current;
- 68 mm x 34 mm x 30 mm

**Safron’s polymer film capacitors**

**Operative voltage | Capacitance | Case-size (in mm)**
--- | --- | ---
400 V | 120μF | Diameter: φ25 mm | Length: 30 mm
400 V | 68μF | Diameter: φ20 | Length: 30 mm

**Electrolytic caps Vishay**

- 400 V formed dielectric

**EPCOS: MLCCs with PLZT**

11 microfarad/cc; 350 V
Theoretical versus Achieved Volumetric Density for 450 V Applications

- Capacitance Density (nF/mm³ or microfarad/cm³)

Technology Gap (between current status and theoretically achievable)
Thin Planar HV and HT Capacitors

- Porous copper electrodes
- **Inorganic-organic hybrid dielectric**
  - Permittivity of 20
  - BDV of 300 V/micron
- Layering with high thermal conductivity adhesives
- High thermal-stability adhesives
- Vias and metallization
- Solder termination with through-vias
- 3D stacking for scaling up in capacitance

8-9 microfarad/cm³
450 V
85-115 C

40 microfarad/cm³
450 V
>175 C

Porous copper Electrode

Conformal counter electrode
Inorganic-Organic Hybrid Nanodielectrics
(Conformally coated on porous copper electrodes)

- Temperature stability of 300°C
- Permittivity ~ 20 and high breakdown strength
- Extractable energy density of 40 J/cm³ before packaging

Joe Perry, GT
Capacitors and Inductors in Integrated Voltage Regulators

Panel-scale integration
## Competitiveness of GT Embedded Inductors

<table>
<thead>
<tr>
<th></th>
<th>Air core</th>
<th>Sputtered Thinfilm</th>
<th>Magnetic Composites</th>
<th>Sputtered films as glass IPDs</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/R&lt;sub&gt;DC&lt;/sub&gt; (nH/mΩ)</td>
<td>0.20</td>
<td>0.20</td>
<td>~20</td>
<td>5-10</td>
</tr>
<tr>
<td>AC losses (% of total loss)</td>
<td>&lt;1%</td>
<td>&lt;1%</td>
<td>&lt;1%</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>Current handling (A/mm&lt;sup&gt;2&lt;/sup&gt;)</td>
<td>&gt;1</td>
<td>1-2</td>
<td>1-2</td>
<td>1-2</td>
</tr>
</tbody>
</table>
Advanced Magnetic Substrates

Nitto Denko Corporation

<table>
<thead>
<tr>
<th>Sample</th>
<th>Frequency[MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10</td>
</tr>
<tr>
<td>Sheet A</td>
<td>182</td>
</tr>
<tr>
<td>Sheet B</td>
<td>141</td>
</tr>
<tr>
<td>Sheet C</td>
<td>92</td>
</tr>
<tr>
<td>Sheet D</td>
<td>9</td>
</tr>
</tbody>
</table>

Polymer insulation
Magnetic sheets

Substrate
Copper winding
Nanomagnetic High-Sat, Soft Magnetic Core Material

- Material sample thickness = >40um
- High deposition rate – high throughput and low cost
- IC or glass substrate- compatible
- Deposition thickness capability up to 50um demonstrated
- $\mu_r= 200$, $B_{sat} = 1.3$ T, $Q @ 5$ MHz$>90$, $Q@ 20$ MHz$=30$
- 0.5 microhenries; Isat of 2 Amp demonstrated on 6 inch;
- Toroid and solenoid inductors demonstrated
Inductors IPDs with Nanomagnetic Films on 50 microns glass

Solenoid inductors

Potcor or racetrack inductors

Magnetic inductors

~10X enhancement in inductance
LC-Embedded Power Substrate

- Pre-manufactured capacitors fan-out embedded in organic laminate panels
- Magnetic components as large-area substrates
- Vertical through-via interconnections
- Ability to support redistribution layers on the top for routing
- Fine-pitch processor or other logic ICs on the topic
## Component- and Package-Level Shielding

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Objectives</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shielding</td>
<td>60 - 120 dB</td>
</tr>
<tr>
<td>Frequency</td>
<td>1 MHz – 40 GHz</td>
</tr>
<tr>
<td>Distance of separation</td>
<td>0.1 – 10 mm</td>
</tr>
<tr>
<td>Shield metal thickness</td>
<td>~5-50 µm</td>
</tr>
</tbody>
</table>

Component-level shielding:
- Plated copper
- Multilayered metallic structures

External shielding:
- Spray-coated, plated, sputtered

Illustration borrowed from Murata

Materials beyond copper are needed to shield magnetic fields
Better EMI isolation Over Cu with Cu-Magnetic structures

(a)

(b)

Port 1

Port 2

(b)

Port 1

Port 2

NiFe+Ti

NiFe

Cu

No shield

Cu(7)NiFe(3)

Cu(3)NiFe(7)Ti

Isolation (dB)

Separation Distance (mm)

-80

-70

-60

-50

-40

-30

-20

NiFe

Cu

NiFe+Ti

No shield

Cu(7)NiFe(3)

Cu(3)NiFe(7)Ti
Summary

GT-PRC is innovating power packaging technologies and also creating an industry ecosystem of material suppliers, component manufacturers and end-users:

• Capacitors in consumer power modules:
  • Silicon-integrated nanoscale tantalum capacitors

• High-temperature and high-voltage capacitors with:
  • Porous copper electrodes
  • Nanoscale inorganic – organic hybrid dielectrics

• Inductors and capacitors in integrated voltage regulators:
  • Low-cost polymer nanocomposite inductors
  • Panel-scale inductor and capacitor integration

• Integrated shielding at component and package-level
  • Materials beyond copper