Interconnect Reliability

Considerations in Dense Power Packages

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Agenda

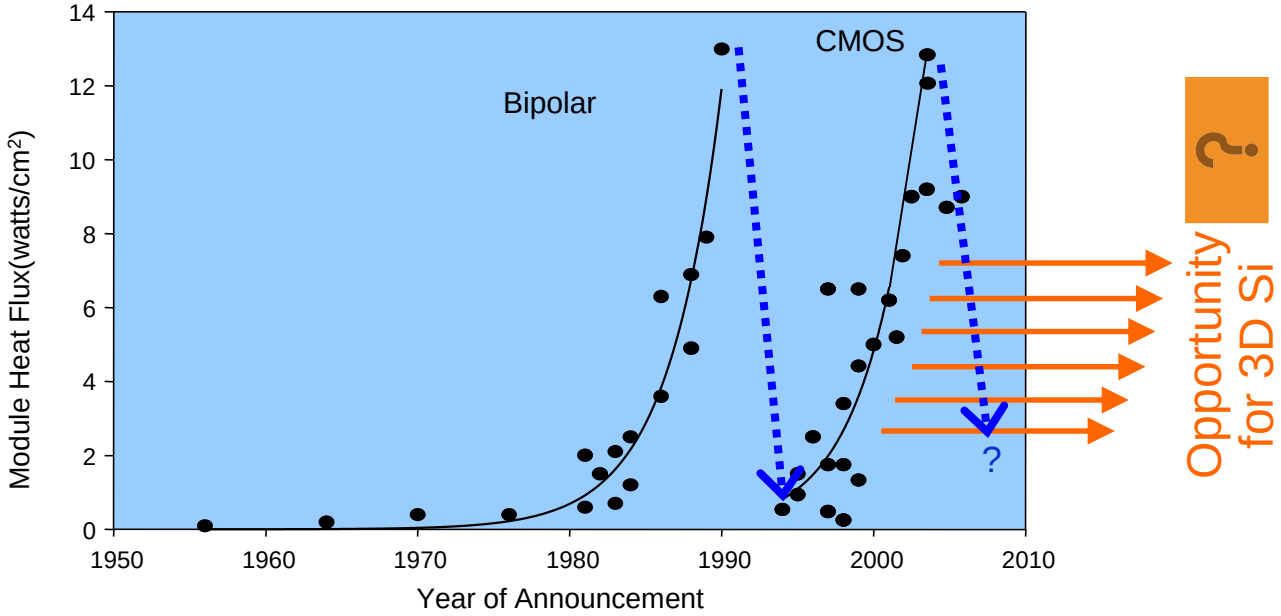
Introduction	**Stress the Importance of Interconnect within electronics as they scale**
Areas of Concern	**Discuss the various areas of concerns with interconnect due to scaling and other system packaging considerations in a 3D structure**
Electromigration	**Review of electromigration and establishing a design of experiments to verify the robustness of interconnect**
Continuing Research	**Introduce the concept of all copper interconnects and continuing research**

The Miniaturization Challenge

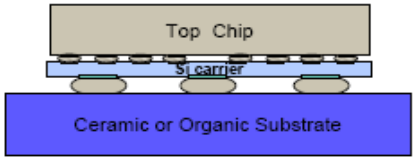
- Today, more than one billion transistors are crammed onto a single microprocessor die thanks to 50 years of miniaturization of integrated circuits
- Further scaling becomes problematic as transistors of only a few atoms are approached
- An alternative concept is **3D integration** – the stacking of integrated circuits on top of each other – improving wiring of electronic circuits similar to the neural network inside the brain

- But challenges arise as you stack chips….
  - For example, the **increased current densities** and the communication bandwidth to a chip stack
- Microprocessors connect to printed circuit boards (PCB) by several 10,000s of solder balls
  - Up to 80% of the interconnects are used for provisioning up to 300 Amps of current
    - Solder ball technology was invented by IBM engineers in the 1960s resulting in the still widely used flip chip technology (commonly called C4 which stands for controlled collapse chip connection)

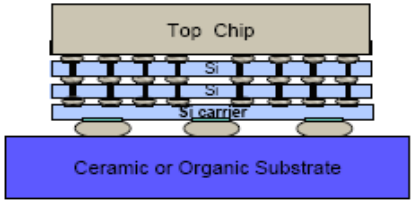
Transition to 3D



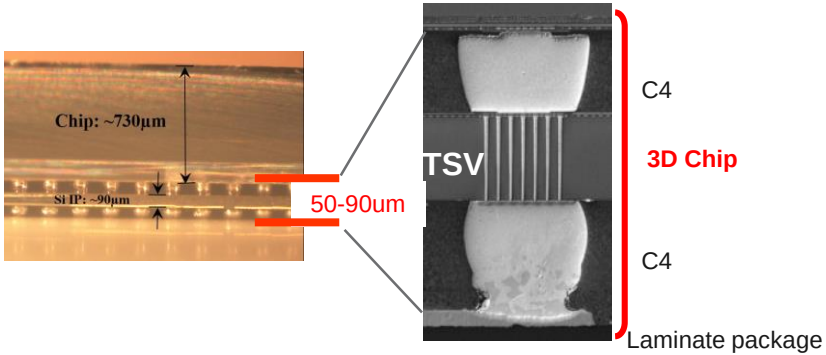
Importance of Interconnect



2-layer stack



4-layer stack



Current through base interconnect increases as number of stacked chips increase

Scaling goes against wiring performance (resistivity) and reliability (electromigration).

It is critical to understand the amplitude of the current flow through each ball within the stackup to determine the worst case current density

Interconnect Concern Areas

1. Effect of multiple solder reflows on metal interfaces
2. Effects of the time above liquidous (TAL) which increases with card size
3. Affects of attach process heat ramp and cool down ramp on interconnect
4. Vulnerability to physical damage due to strain or warping effects of the substrate or PCB material
5. Impact of compression loading forces
6. Verification of acceptable interconnects throughout package
7. Rework of the power package
8. Long term electromigration concerns due to current density

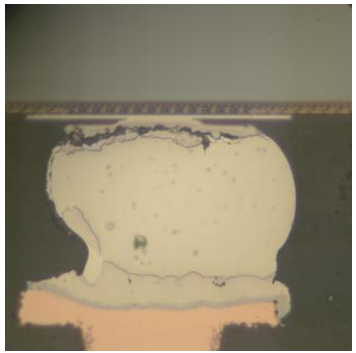
Interconnect Application Trends

- Changes in Application Conditions, Typically:
  - Increasing Operating Temperatures
  - Increasing Interconnect Currents
- Shrinking Interconnect Sizes
  - Increases Current Density Values
- Die Size Changes
  - Larger Die: Increases Total Power / Ground C4 Counts
  - Smaller Die: Can Drive Reduction in Number of Connections
- RoHS Compliance: Pb – Free Interconnects
  - Pb / Sn Bumps Replaced with Sn / Ag Bumps

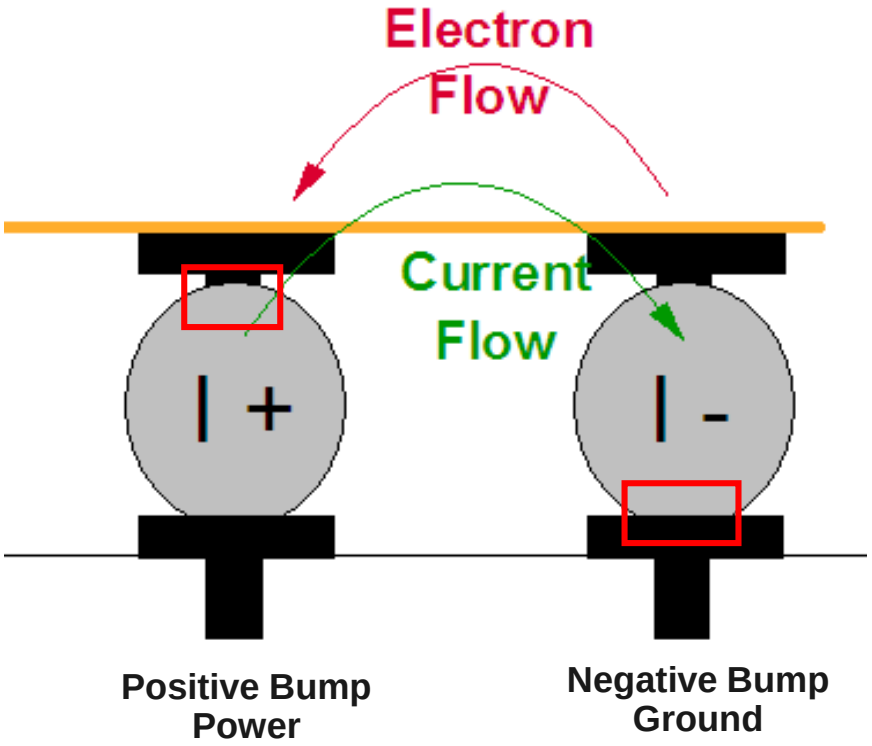
Can Electromigration be an Issue?

Electromigration

- Electromigration (EM) is the transport of material caused by the gradual movement of the atoms in a conductor due to momentum transfer driven by conducting electrons.
  - It causes a net atom transport along the direction of electron flow.
  - The atoms pile up at the anode, voids are generated at the cathode
  - The typical failure of a solder joint due to electromigration will occur at the cathode side.
  - Current crowding accelerates the creation of voids within a solder joint.
  - As the voids extend, electrical failures can result.
  - Electromigration also influences the formation of intermetallic compounds.



Electromigration Schematic



Chip / BLM Side

- BEOL Design
- BLM Thickness / Type
- C4 Solder Composition

Substrate Side

- Pad Metallurgy
- C4 Solder Composition
- Presolder Composition
- Substrate Design

Fails occur at transition point to solder!

Black's Law for Electromigration

$$t_{50} = \frac{A}{j^{n}} e^{\frac{\Delta h}{kT}}$$

Δh = Activation Energy
0.7 – 1 eV Typical

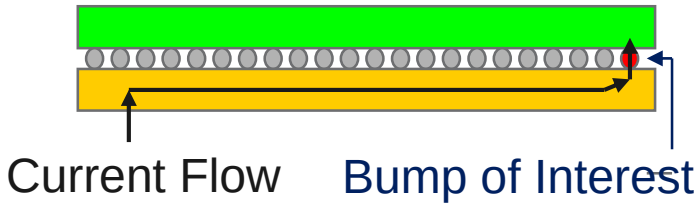
n = Current Density Exponent
1.5 – 2 Typical

Performance Governed By:

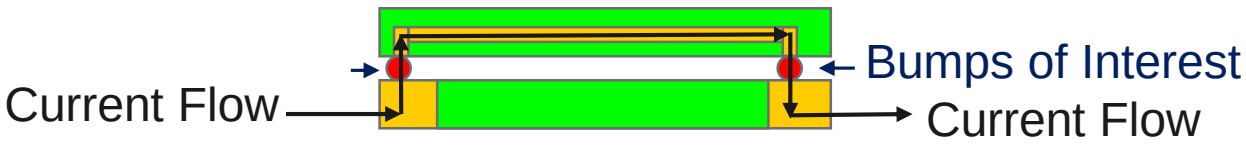
- Application Temperature
- Current Density (Local & Global)
- Materials System

Electromigration Test Vehicle Current Flow

Side View

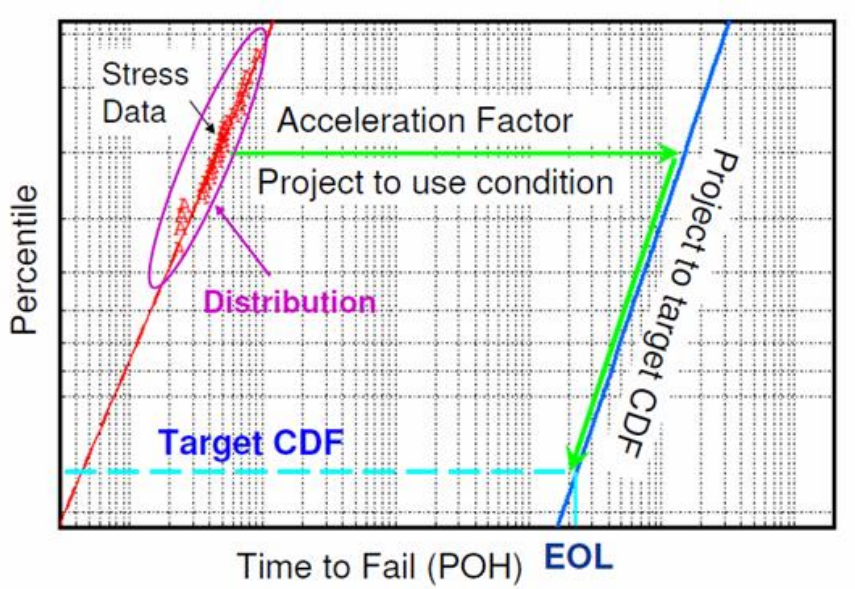


Edge View



The Purpose of the Test Vehicle is to isolate the current path to single ball of interest
Measure: Bump Resistance (4 wire Kelvin measurement)
Bump Temperature

General Reliability Testing Strategy



Terminology:
Acceleration Factor – fail time ratio @ use vs @stress
CDF → Cumulative Failure (for this talk)
EOL → End of Life; POH → Power On Hours

Projection Methodology Maintains Sigma from Accelerated Testing

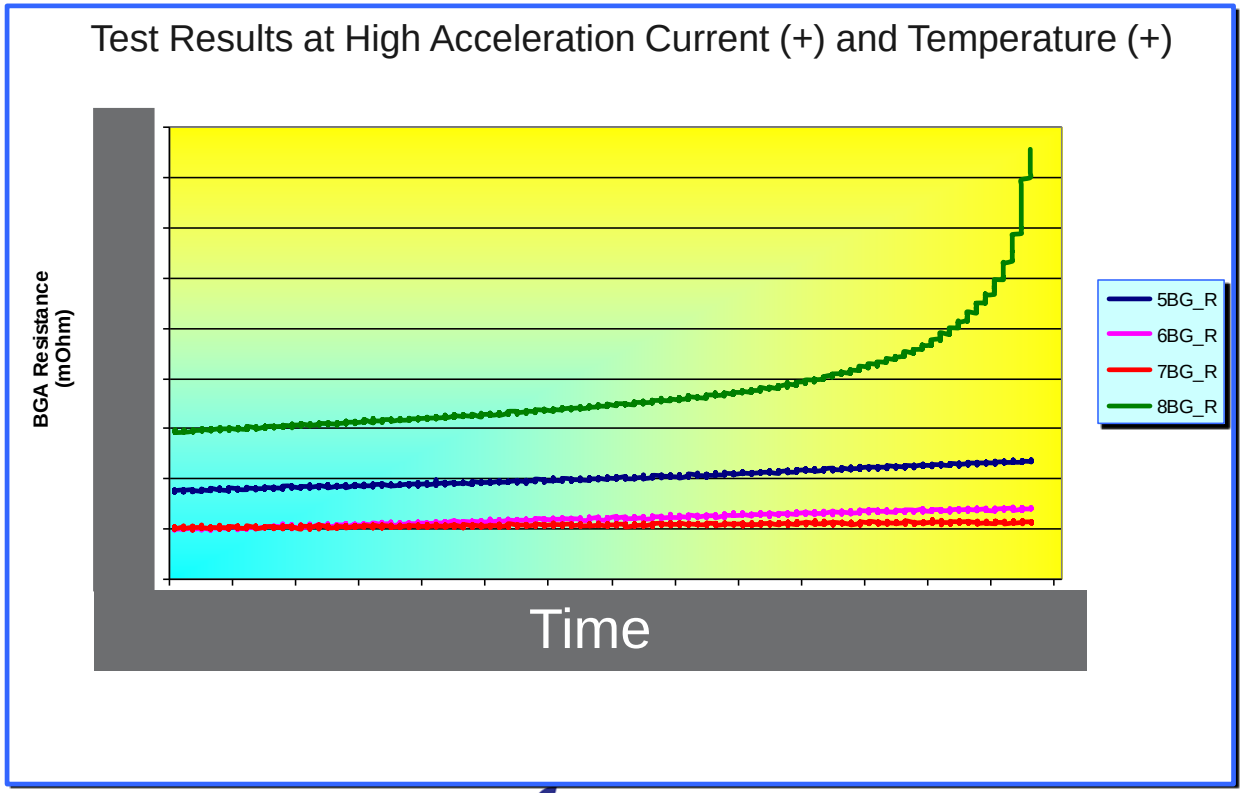
Design of Experiment

Experiment control parameters

Test #	Ambient Temperature (° C)	Joule Heating (~ ° C)	BGA Temperature (~ ° C)	Current (A)	Current Density (A/cm^2)
1	−	−	−	−	−
2	−	+	+	+	+
3	+	−	−	−	−
4	+	+	+	+	+

Monitor delta-R of interconnect joint

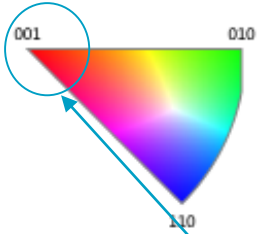
BGA Interconnect Resistance Change

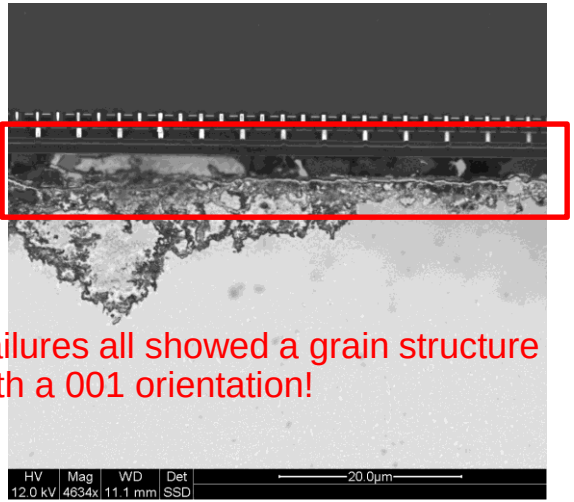


Electromigration Studies – Grain Orientation

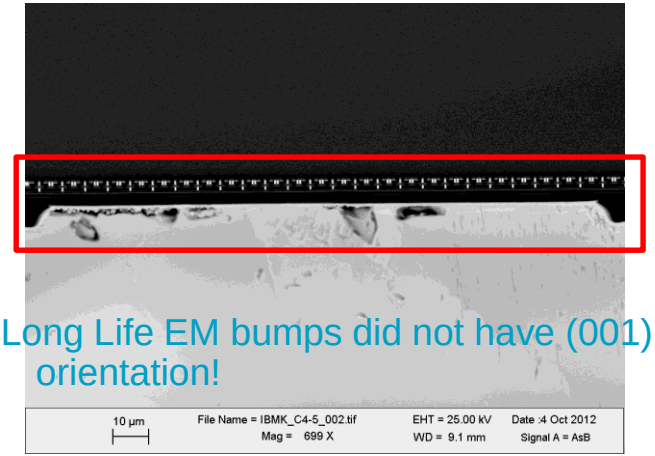
- **Early Failure Samples Analyzed**

Non Failed Samples Analyzed



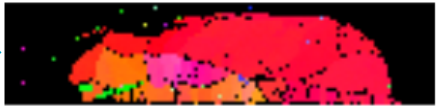


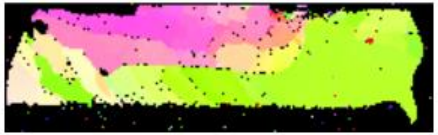
Failures all showed a grain structure with a 001 orientation!



Long Life EM bumps did not have (001) orientation!

Electron Backscatter Diffraction (EBDS) Analysis

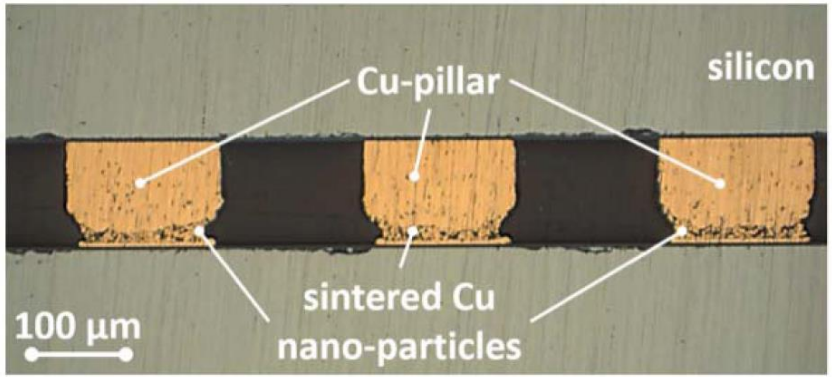


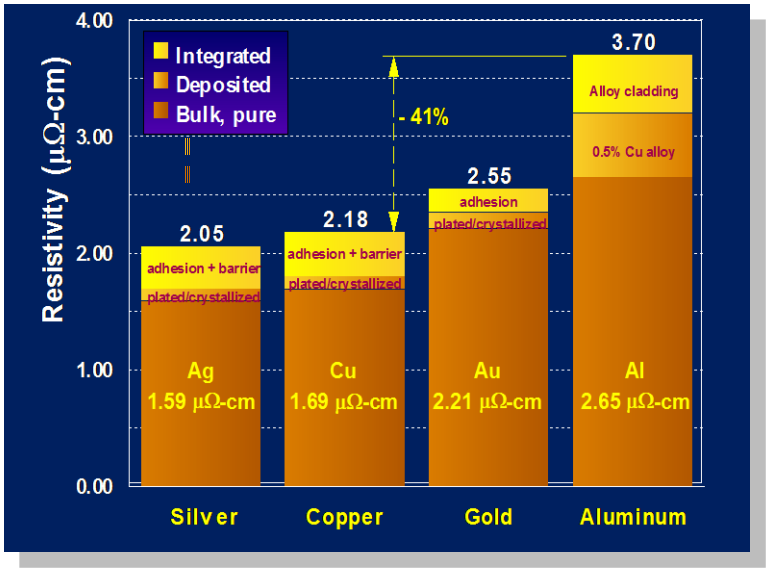


EBSD / SEM Analysis by J. Advocate, Y. Guo, B. Backes

IBM Research – All Copper Interconnects

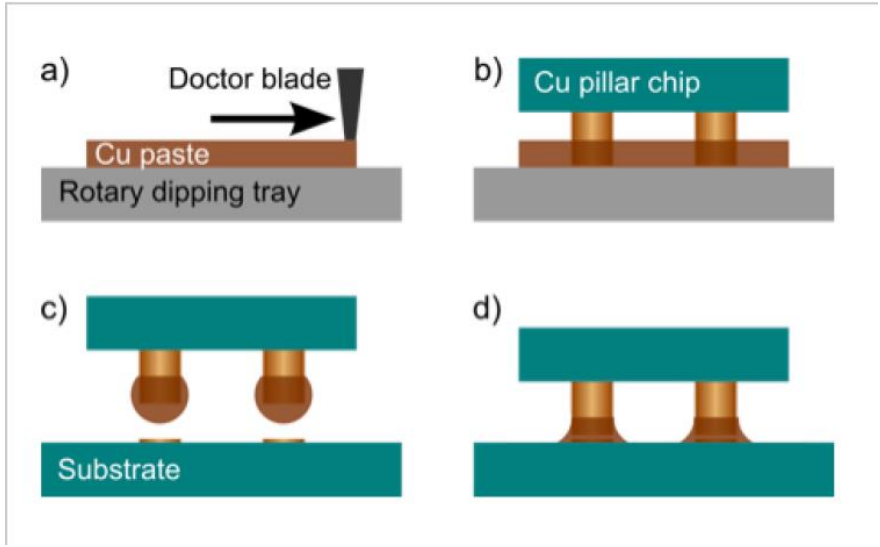
- Copper interconnect is about ten-fold more resistant to electromigration than solder
- The high melting temperature of copper (1085°C) needed to be overcome
  - IBM researchers invented a process to replace solder with copper together with colleagues from Intrinsiq Materials, SINTEF, and the Technical University of Chemnitz
  - Interconnects formed by using a copper nanoparticle paste between a copper pillar and a pad followed by an annealing step at temperatures as low as 150°C





All Copper Interconnect

- All Copper Interconnects have the potential to overcome current density and pitch limitations of current solder joint technology
- Research to improve the all copper interconnect is continuing
  - Final Electromigration robustness of the interconnect must be evaluated
  - Investigate smaller pillar heights and pitches may be supported
  - For more information, refer to “Nanoparticle Assembly and Sintering Towards All-Copper Flip Chip Interconnects“ published at the IEEE 2015 Electronic Components & Technology Conference



Conclusions

- To Verify Interconnect Reliability:
  - Many factors must be modelled and verified including:
    - Verify Robustness to Electromigration
    - Effects of thermal cycles due to attach processes
    - Analyze impact of thermal ramp rates during attach and rework
    - Impact of warpage and strain on stack interconnect during assembly
    - Review compression loading forces on package
    - How to ensure interconnect robustness in large 3D stacks
- In addition to traditional life tests such as accelerated thermal cycling, bias temperature & humidity, etc., an Electromigration (EM) analysis shall be done to verify whether EM concerns exist
  - Be aware of the impact that grain orientation may have on the expected life. Guard against (001) grain orientation.
  - Insure high power interconnects are redundant / fault tolerant
- Packaging & 3D integration are critical to systems scaling

Acknowledgments

- I would like to acknowledge and thank the following IBM colleagues for their technical contributions and input to this work.
  - Jerry Bartley – IBM Distinguished Engineer
  - Thomas Wassick – Microelectronics Package Reliability
  - Thomas Brunschwiler, et. all - IBM Research

- Excerpts From "The Charge of the Light Brigade"
By Lord Alfred Tennyson, Crimean War 1854

'Forward, the Light Brigade!'
Was there a man dismay'd?
Not tho' the soldiers knew
Some one had blunder'd:
Theirs not to make reply,
Theirs not to reason why,
Theirs but to do and die:
Into the valley of Death
Rode the six hundred.

Cannon to right of them,
Cannon to left of them,
Cannon behind them
Volley'd and thunder'd;
Storm'd at with shot and shell,
While horse and hero fell,
They that had fought so well
Came thro' the jaws of Death,
Back from the mouth of Hell,
All that was left of them,
Left of six hundred.