3D SiP with Embedded Chip Supply Chain Integration

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Agenda

• Introduction of UTAC and AT&S
• Trends, Applications & Trade offs for 3D SiP w/ Embedded Chip
• AT&S ECP® Technology and Performance Summary
• Examples of Embedded Chip Product Solutions
• 3D SiP with Embedded Chip UTAC / AT&S Collaboration
• Summary
UTAC at a Glance

- Outsourced Semiconductor Assembly and Test services (OSAT) provider in support of Analog, Mixed-Signal, Logic, Power and Memory products
- UTAC 2015 Revenue $878M; Ranked 6th in the Top Ten OSATs; 12k employees strong; Sales offices located worldwide
- Focus – Assy, Test and Full Turnkey; Test comprises 35% of sales in 2015
- Est. 1997 Singapore; ten factories w/ 260K M²; operations in six countries Singapore, Taiwan, Malaysia, Indonesia, Thailand, China
- 3 Factories with SiP capability
- Markets: Mobile, Automotive, Security, Wearable’s, Industrial & Medical
AT&S at a Glance

High-end interconnection solutions for Mobile Devices, Automotive, Industrial, Medical Applications and Semiconductor Industry

9,452 employees

Continuously outperforming market growth

# 3 in high-end technology worldwide

€ 762.9m revenue in FY 2015/16; 5.2% organic growth

One of the most profitable players in the industry*  

Cost-competitive production footprint with 6 plants in Europe and Asia

# 1 manufacturer in Europe

* In terms of EBITDA margin
AT&S ECP® Platform Technology

ECP® (Embedded Component Packaging) uses the space in an organic laminate substrate (PCB) for active and passive components integration.

01 Component assembly
02 Lamination
03 Structuring

Components embedding into the PCB core with copper plated microvia connections.

Embedded passives
SMT WLCSP
PCB with embedded IC
Trend to 3D SiP

3D integration
Chip Embedding

3D Interconnect
2 side cooling
Shielding

SiP Performance (size, electrical & thermal)

Co-Design
Optimization

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AT&S
## Applications for 3D SiP with Embedded Chip

### Embedded Die Potential Applications Matrix

<table>
<thead>
<tr>
<th>Stand-Alone active die packages</th>
<th>Embedded SiP Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell phones</strong></td>
<td>Cellular Radio: IPD-RF, Transceiver, PA</td>
</tr>
<tr>
<td>IPD - ESD protection</td>
<td>WLAN Module: IPD-RF, DC/DC converter</td>
</tr>
<tr>
<td>IPD – RF</td>
<td>Bluetooth/GPS/FM: DC/DC converter, processor</td>
</tr>
<tr>
<td>DC/DC converters</td>
<td>CPU/GPU: Embedding of stacked ICs in PoP</td>
</tr>
<tr>
<td>IC Drivers: Audio codec, battery charger, display interface, LED driver)</td>
<td>Memories: Embedding of stacked ICs in PoP</td>
</tr>
<tr>
<td>Power Management Unit</td>
<td>Baseband: Embedding of stacked ICs in PoP</td>
</tr>
<tr>
<td>Transceivers</td>
<td>Audio Module: IPD-ESD, IPD-Capa, Audio codec/driver</td>
</tr>
<tr>
<td>Bluetooth/GPS/FM: Processor</td>
<td>Digital TV Module: IPD-Capa, Video decoder, DC/DC converter</td>
</tr>
<tr>
<td><strong>Portable media players</strong></td>
<td>Camera Modules: Sensor, DC/DC ISP, AF driver</td>
</tr>
<tr>
<td><strong>Notebooks</strong></td>
<td>MEMS/Sensor Modules: Sensor(s), ASIC</td>
</tr>
<tr>
<td><strong>Digital cameras</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Medical &amp; industrial</strong></td>
<td>LED Modules: LED driver, MOSFET</td>
</tr>
<tr>
<td>IPM “Intelligent Power Modules”</td>
<td>Engine Control Module: MCU, memory, IPD</td>
</tr>
<tr>
<td>MOSFET, IC drivers, Thin-film batteries</td>
<td>Hearing Aids: IPD-ESD, IPD-Digital, processor, memory</td>
</tr>
<tr>
<td><strong>Automotive</strong></td>
<td>Pacemakers: PD-ESD, IPD-RF, IPD-Digital, processor, memory</td>
</tr>
<tr>
<td>IPM “Intelligent Power Modules”</td>
<td>Wireless Sensor Node applications: RFID, thin-film battery, magnetic hall sensor</td>
</tr>
<tr>
<td>MOSFET, IGBT, IC driver, Sensor</td>
<td>Telematics/Car information units: GPS, NFC</td>
</tr>
<tr>
<td><strong>Co-Marketing Materials</strong></td>
<td>MEMS/Sensor Modules: Sensor(s), ASIC</td>
</tr>
<tr>
<td>AT&amp;S</td>
<td>Camera Modules: Hall Sensors, TMPs, IMU modules, RFID</td>
</tr>
</tbody>
</table>


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Embedding Technology Milestones

Concepts ➔ Research ➔ Development Projects ➔ Industrialization ➔ Serial Production

- Embedded silicon
- Printed capacitor
- Discrete capacitor
- Printed resistor
- Discrete resistor
- Embedded Chip

- 1970
- 2000
- 2002
- 2004
- 2006
- 2008
- 2010
- 2012
- 2014
- 2016

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Co-Marketing Materials
# Why Chip Embedding?

## Unique Selling Propositions

<table>
<thead>
<tr>
<th>Proposition</th>
<th>Detail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Miniaturization</td>
<td>• Footprint reduction</td>
</tr>
<tr>
<td></td>
<td>• Higher component integration (additional assembly layer)</td>
</tr>
<tr>
<td>Electrical performance</td>
<td>• Improved signal performance (higher data rates)</td>
</tr>
<tr>
<td></td>
<td>• Reduction of parasitic effects</td>
</tr>
<tr>
<td>Mechanical performance</td>
<td>• Higher durability and reliability through copper-to-copper connections (copper filled microvias)</td>
</tr>
<tr>
<td></td>
<td>• Package enables protective enclosure</td>
</tr>
<tr>
<td></td>
<td>• High drop, shock and vibration tolerance</td>
</tr>
<tr>
<td>Thermal management</td>
<td>• Improved heat dissipation through direct copper connection</td>
</tr>
<tr>
<td></td>
<td>• Improved heat dissipation FR4 versus air (compared to SMD)</td>
</tr>
<tr>
<td>Additional functions</td>
<td>• EMV shielding (partial or full shielding of a package)</td>
</tr>
<tr>
<td></td>
<td>• Package is the housing → no additional molding required</td>
</tr>
<tr>
<td>ECP is supporting the trend towards modularization</td>
<td>• Lower set-up costs compared to other packaging technologies (packaging versus PCB processes)</td>
</tr>
<tr>
<td></td>
<td>• Customization of footprint and module versions can be done due to digital imaging - no separate tooling necessary (e.g. QFN)</td>
</tr>
<tr>
<td>Anti-Tamper and Security</td>
<td>• Hidden electronics preventing reverse engineering and counterfeiting</td>
</tr>
</tbody>
</table>
Comparison of Package Area vs. Thermal Resistance

Source: GaN Systems, AT&S IMAPS 2014

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Co-Marketing Materials
Package Inductance Ranking

Source: GaN Systems / AT&S IMAPS 2014

GaN PX
100V package
6.9 x 3.1 mm
0.45 mm thick
TI MicroSiP™
(Introduced 2011  > 20 products)

Thermal Evaluation

Thermal Image of MicroSiP™ when IC is dissipating 0.45W. Ambient temperature is 22°C, max junction temperature is 72°C. For thermal modeling, a value of $\Theta_{JA}=125^\circ C/W$ provides an excellent initial estimate of thermal performance.

Board-Level Reliability Data

<table>
<thead>
<tr>
<th>8-pin MicroSiP™</th>
<th>Test Parameters</th>
<th>Results ($t_{\text{first fail}}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Drop</td>
<td>1500G/1.0ms pulse, &gt; 100 drops</td>
</tr>
<tr>
<td></td>
<td>Temp Cycle</td>
<td>-40/125°C, 2 cycles/hr, &gt; 1000 cycles</td>
</tr>
</tbody>
</table>
TDK’s SESUB Technology shrinks power mgmt section 60% in Blackberry™ Z10 Phone (2013)
Embedded Chip Technology – adoption accelerating in Power Applications

Cross section (X-ray)

Control pin (BOOT)

Cross section (SEM)

Buck converter with driver and high-side and low-side switches

Embedded Chip Power Solutions also from:

General Electric
Schweizer
TDK

Infineon’s embedded chip DrBlade™

Infineon’s embedded chip DrBlade™
UTAC & AT&S Collaboration

- System in a package (SiP) is a strategic focus area for UTAC and AT&S
- 3D SiP with Embedded Chip provides integration, size and performance benefits over 2D planar SiP solutions
- 3D Embedded Chip technology adoption is accelerating in Power and High Density Interconnect Applications
- Supply chain collaboration for emerging 3D SiP solutions with embedded chip technology will advanced the technology and provide full turnkey (FTK) supply solutions for customers.
- Flexible business models available to fit to customer requirements
3D SiP Supply Chain UTAC / AT&S Collaboration

Alignment on Design Rules & Roadmaps
- Substrate design
- Assembly design
- Design integration

KGD test
RDL
Thin / Dice
Inspect / TnR

Substrate manufacturing
Embedded chip
Strip Test

SMT
Top FC / under fill
Cap or Mold
Solder Ball Attach
Package saw

Package level test
Reliability test

Co-Design
Customer Specs

Wafer to Die
Customer Consigned Option

AT&S

AT&S

AT&S

AT&S

AT&S

AT&S over 5 years production embedding experience.

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Co-Marketing Materials
Die require 5-10um thick Cu pads for embedding

- > 200um pad pitch for yield / cost optimization
3D SiP w/ Embedded Collaboration Example

Package Type: 4.5 x 7.2mm LGA-SIP
Highlights: 2 embedded die + 24 passive components on substrate top side

<table>
<thead>
<tr>
<th>Package size / Type</th>
<th>4.5 x 7.2 mm LGA-SIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Thickness</td>
<td>560 um ± 10% 320um core</td>
</tr>
<tr>
<td>Die thickness</td>
<td>200 um Max.</td>
</tr>
<tr>
<td>Surface finish (Die DAP)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td>Surface finish (Land Pad)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td># of Passive Component</td>
<td>24 Passives</td>
</tr>
<tr>
<td>(Top of substrate surface)</td>
<td></td>
</tr>
<tr>
<td>Component Sizes</td>
<td>10ea 01005 10ea 0402 4ea 0201</td>
</tr>
<tr>
<td># of embedded chip</td>
<td>2</td>
</tr>
<tr>
<td>Strip Size</td>
<td>188x64mm</td>
</tr>
<tr>
<td>Substrate Metal layers</td>
<td>4 Layer</td>
</tr>
</tbody>
</table>

Assembly Layout

Top-side components (Capacitors, Resistors, Diodes)

CMOS Driver Die  GaAs FET Die

Courtesy of Sarda Technologies, Inc.
3D SiP w/Embedded Chip Business Models

1. UTAC provides full turnkey with AT&S as strategic supplier for embedded chip in substrate. Customers place 1 PO to UTAC -full responsibility for quality. Since embedding is a chips 1st process KGD supply is critical to yield. Customers consign wafers. Substrate design complexity has yield complexity so Yield ranges need to be agreed based on KGD quality level and embedded substrate density / yield.

2. AT&S provides FTK with UTAC as strategic supplier for wafer to die processing, assy / test. This applies where customer is better fit for AT&S due to level of current biz relations. AT&S and UTAC have guides in place and discuss in good faith who best positioned to serve a customer requiring FTK. Above items still apply.

3. Split business with customer providing a PO to AT&S for embedding and UTAC for assy / test. This model often applies in development phase, but in some cases may apply for production.

In some cases a 3 way NDA may be executed to enable AT&S, UTAC and customer to exchange confidential information to enable Co-design to optimize a design for: Performance, Cost, Reliability, Test and Mfg yield
Summary

- System in a package (SiP) is a strategic focus area for UTAC and AT&S

- 3D SiP with Embedded Chip provides integration, size and performance benefits over 2D planar SiP solutions

- 3D Embedded Chip technology adoption is accelerating in Power and High Density Interconnect Applications

- Supply chain collaboration with AT&S for emerging 3D SiP solutions with embedded chip technology will advance the technology and provide full turnkey (FTK) supply solutions for customers.
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Mr. Rainer Frauwallner - R.Frauwallner@ats.net