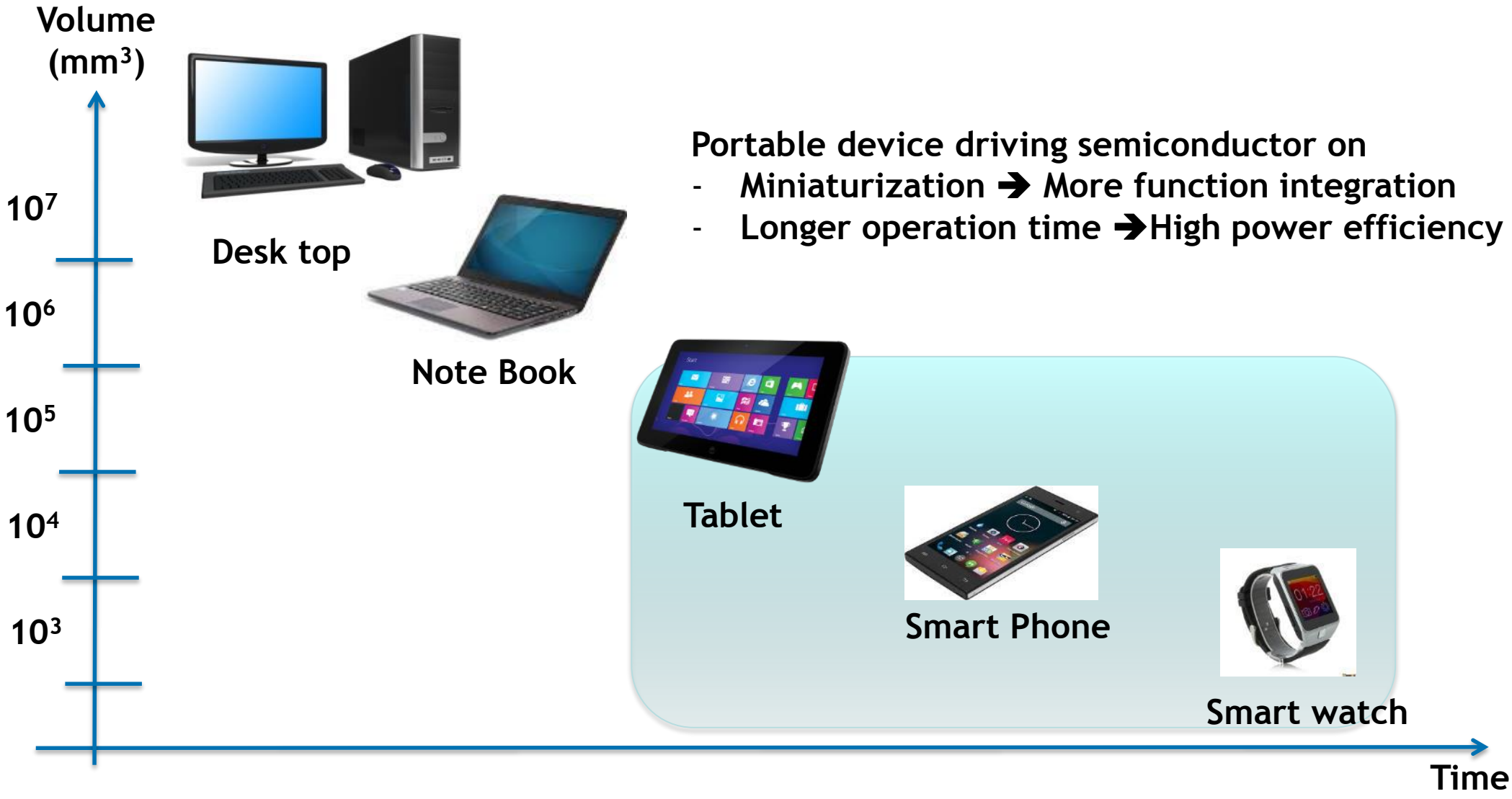
ASE GROUP

Innovations in Chip Embedding for Power Packaging

ASE
Nov, 2016

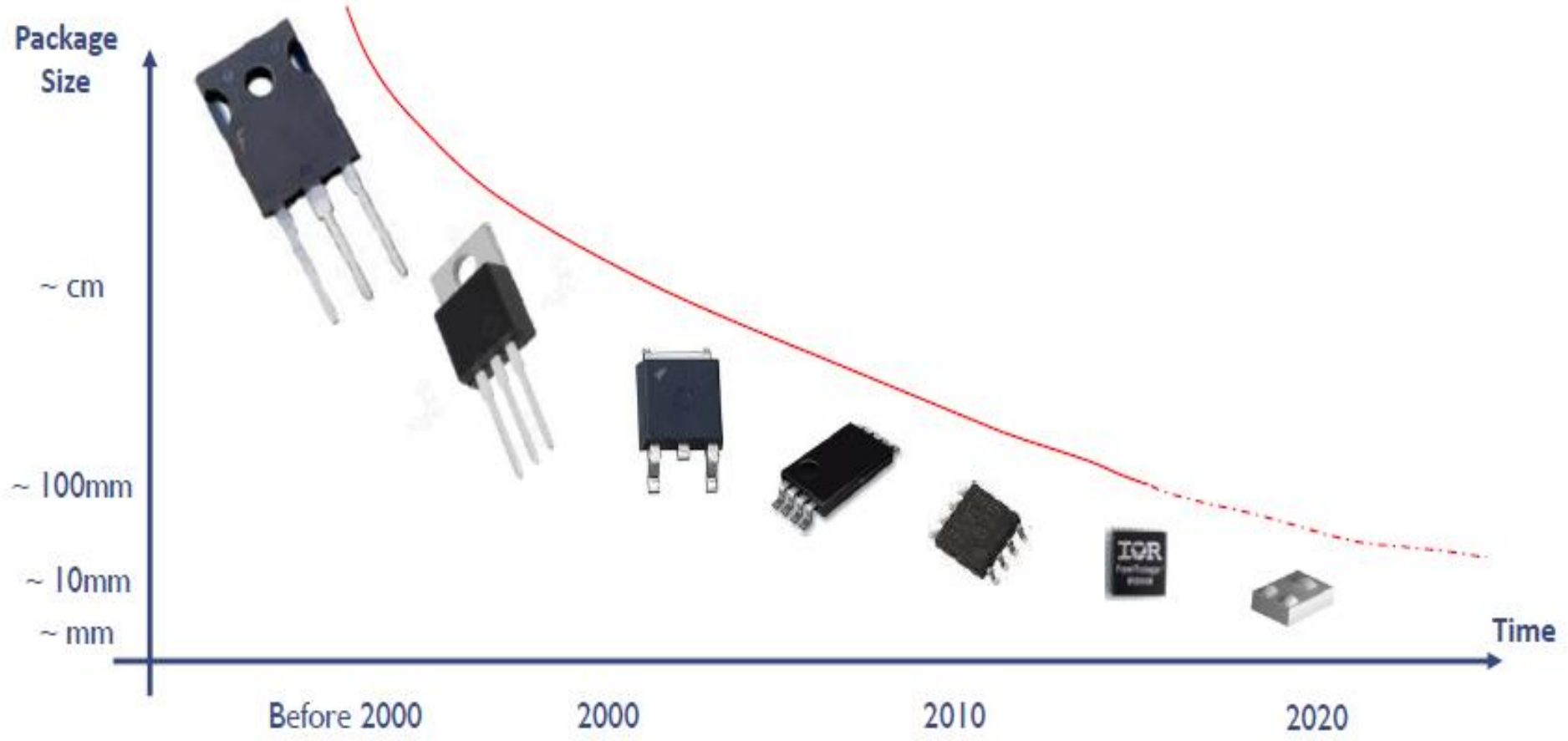
Device continue the way to Miniaturization



Portable device driving semiconductor on

- Miniaturization ➔ More function integration
- Longer operation time ➔High power efficiency

Package Solution to Support Miniaturization - Power Device Packaging



Source: Yole

The Evolution Cycle & Challenge

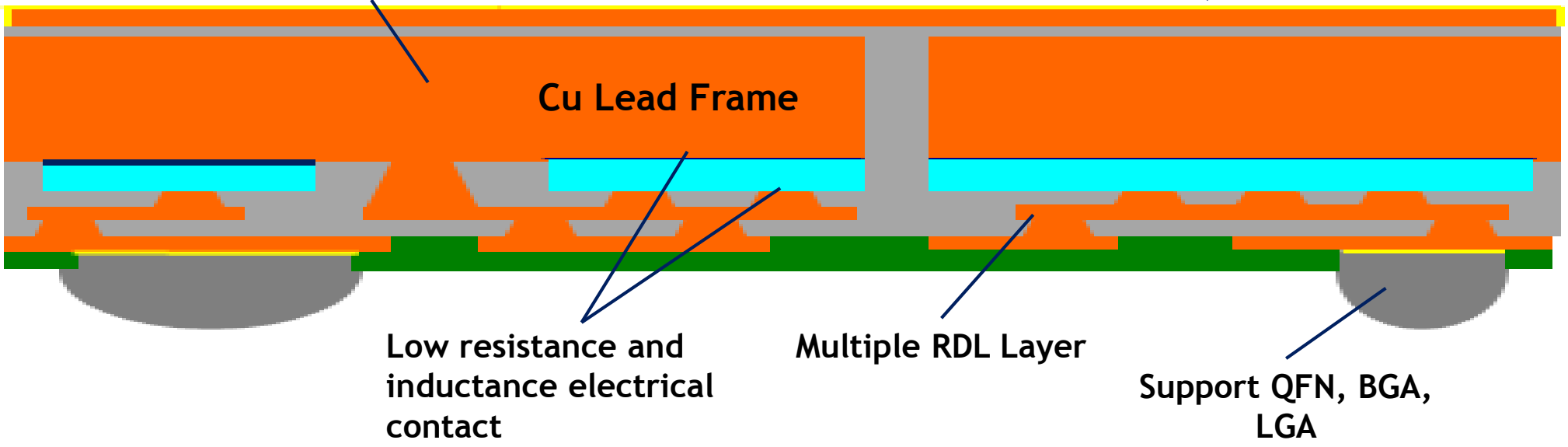
- Higher switching frequency (IC/Wafer design Evolution)

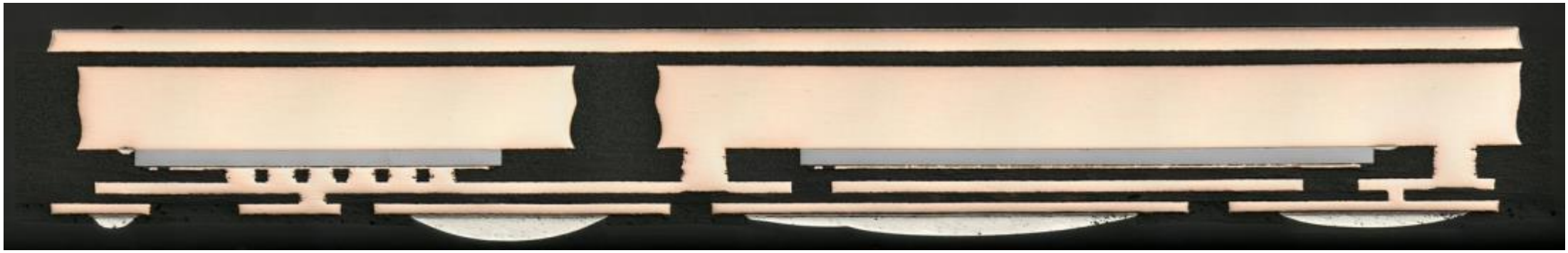
- Smaller Capacitor/inductor
- Light weight
- Small form factor in module/package

Challenge to Package and system

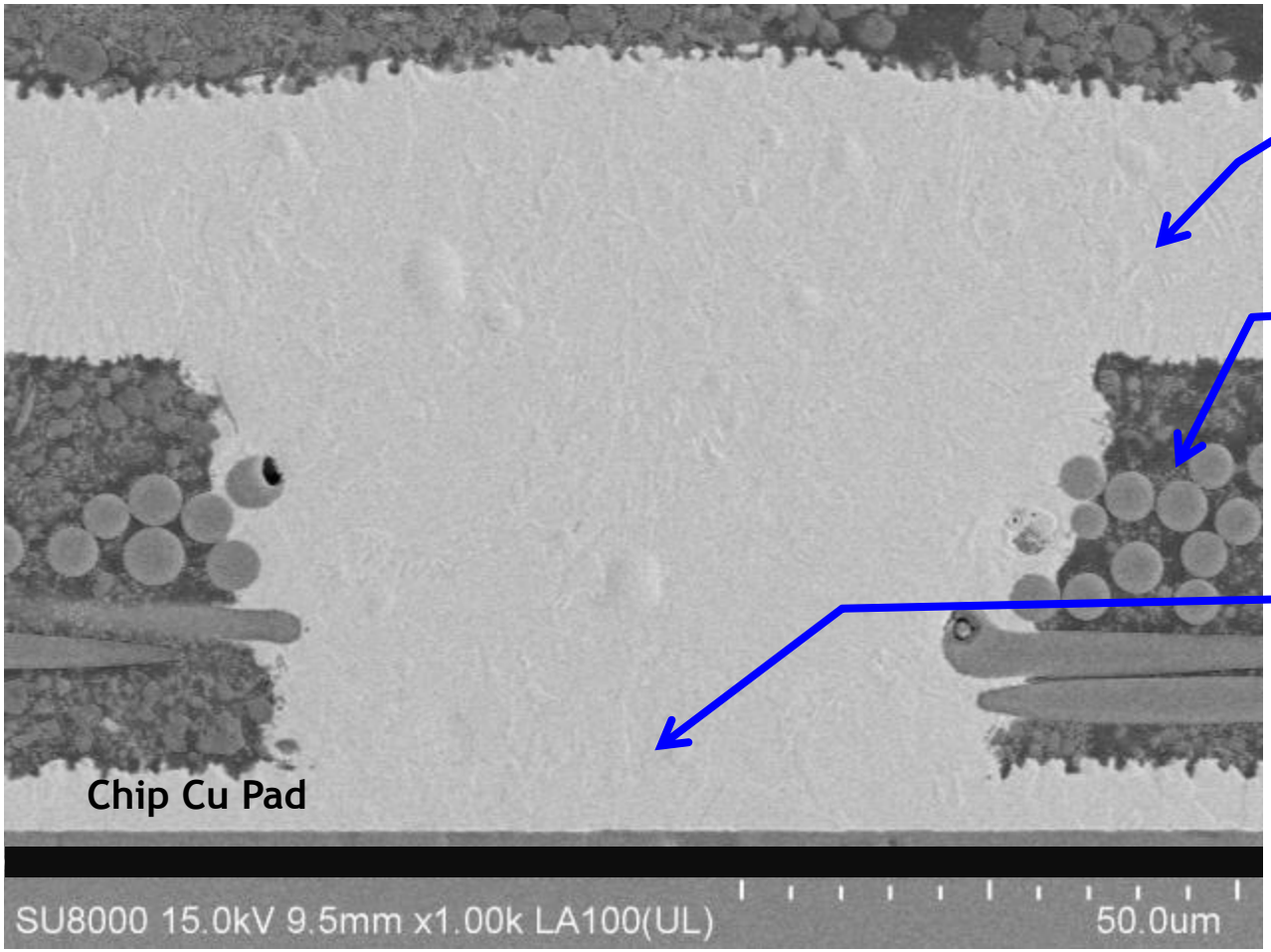
- Higher current density
- High thermal requirement
- Low package parasitic
- High reliable material
- EMI interference
- Passives integration

Package innovation for Power SiP
- Chip Embedded Technology, aEASI



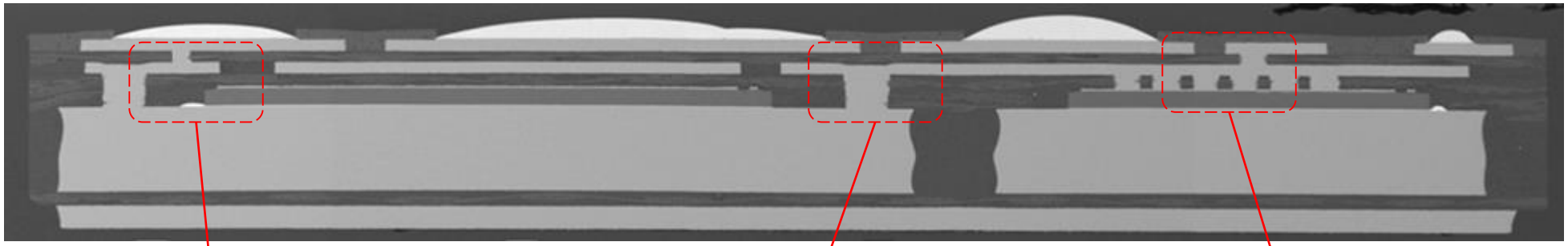


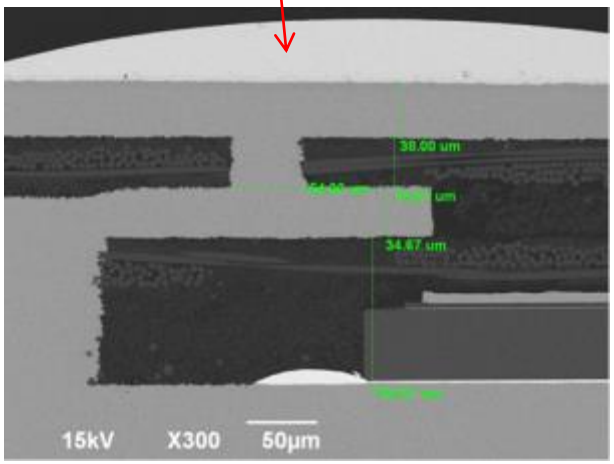
Die-to-Package Interconnection



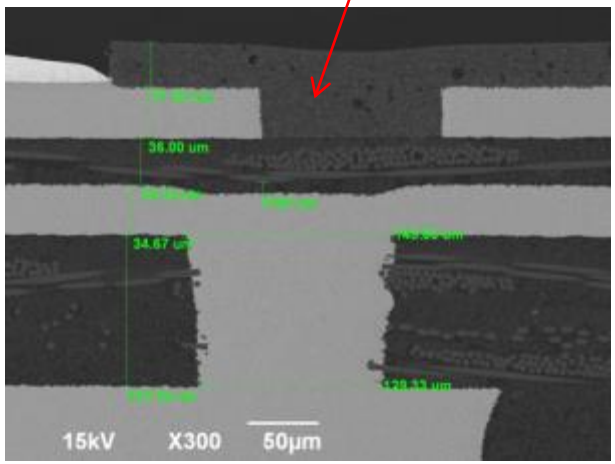
- Thick Cu RDL (32 um). Minimize turn on resistance.
- Prepreg material provide >2.5KV breakdown voltage >230°C (Tg)
- 50um via diameter (Equal to Four 1 mil wire bond in conductor area)
- Cu to Cu interface. Minimize reliability risk in high current density condition

aEASI P1

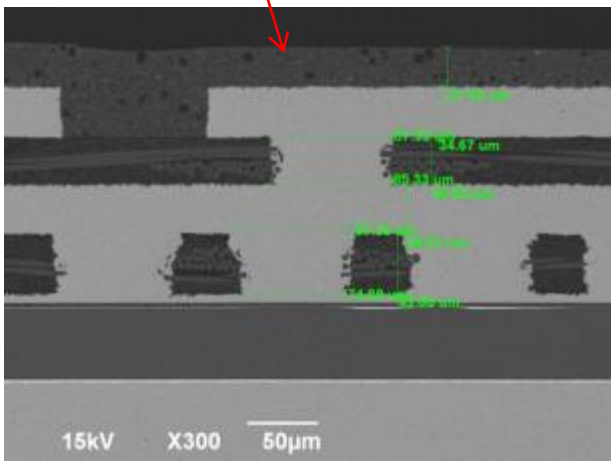




Thick Cu RDL (32um)

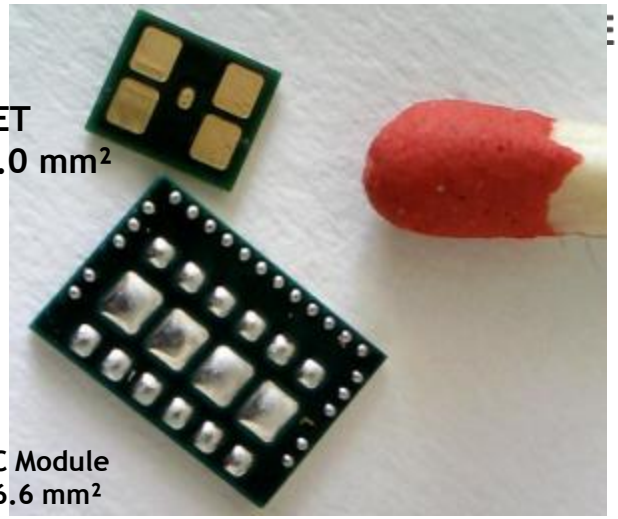


Deep Via (Diameter = 120um)



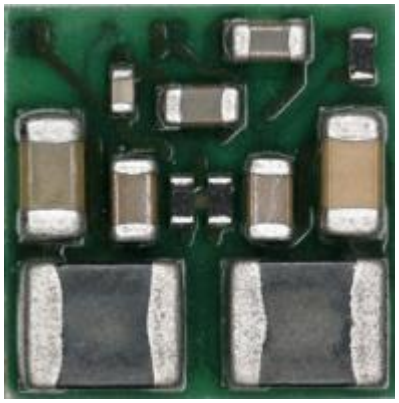
Small via (Diameter = 70um)
Thin Die (60um)

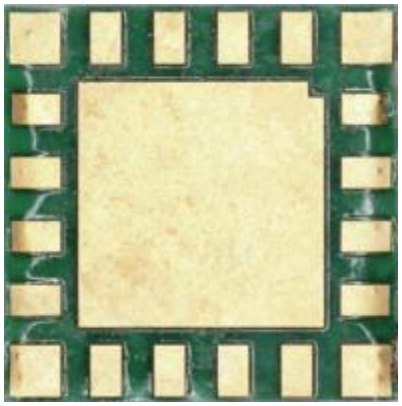
Power SiP Device - realized by aEASI



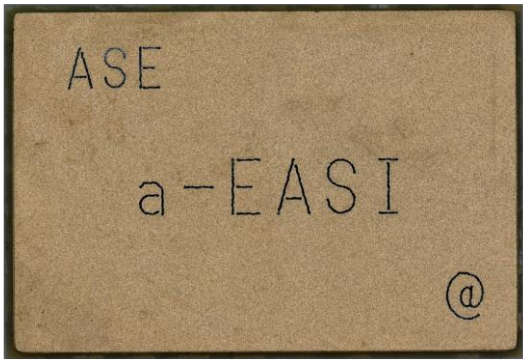
MOSFET
3.4x3.0 mm²

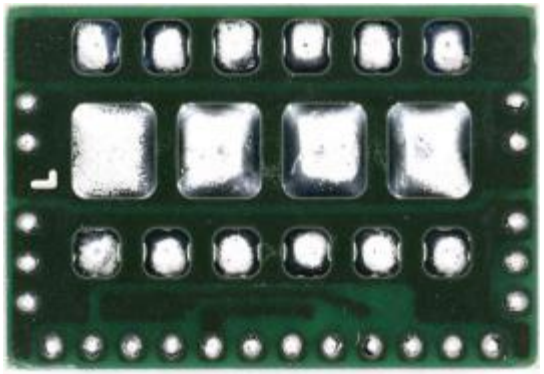
DC/DC Module
4.5x6.6 mm²





Package Size: 5 x 5 x 0.57 mm (exclude passives height)
1 Micro Power Management Chip
Passives: 12pc
0806 x 2, 0603 x 2, 0402 x 4, 0201 x 4
RDL: 2+1 Layer





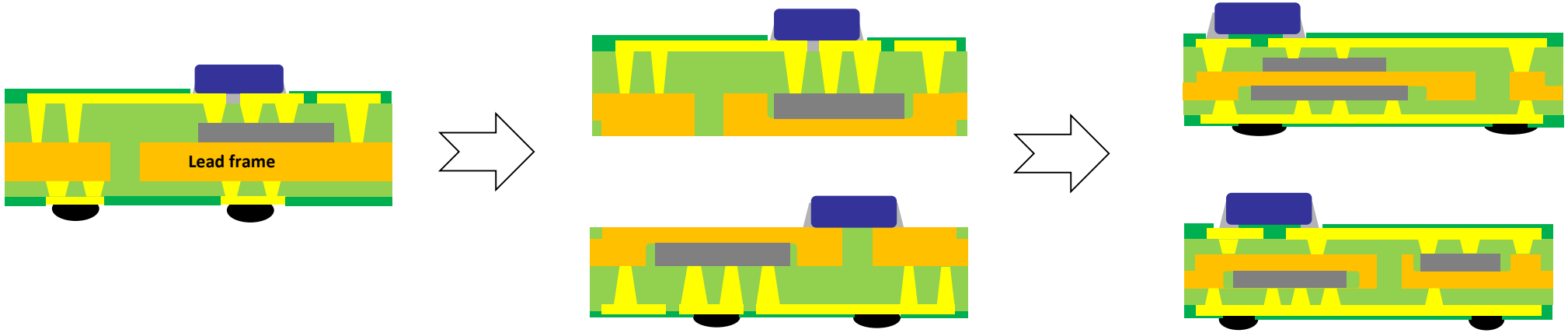
Package Size: 6.65 x 4.55 x 0.8 mm
2 power MOSFET + 1 Driver
RDL: 2+1 Layer

Continuous Innovation

- Excellent Electrical & Thermal performance
- HVM Production proven

- Thermal Enhance (Exposed pad)
- Thinner Package
- Support various footprint (BGA, LGA, QFN_

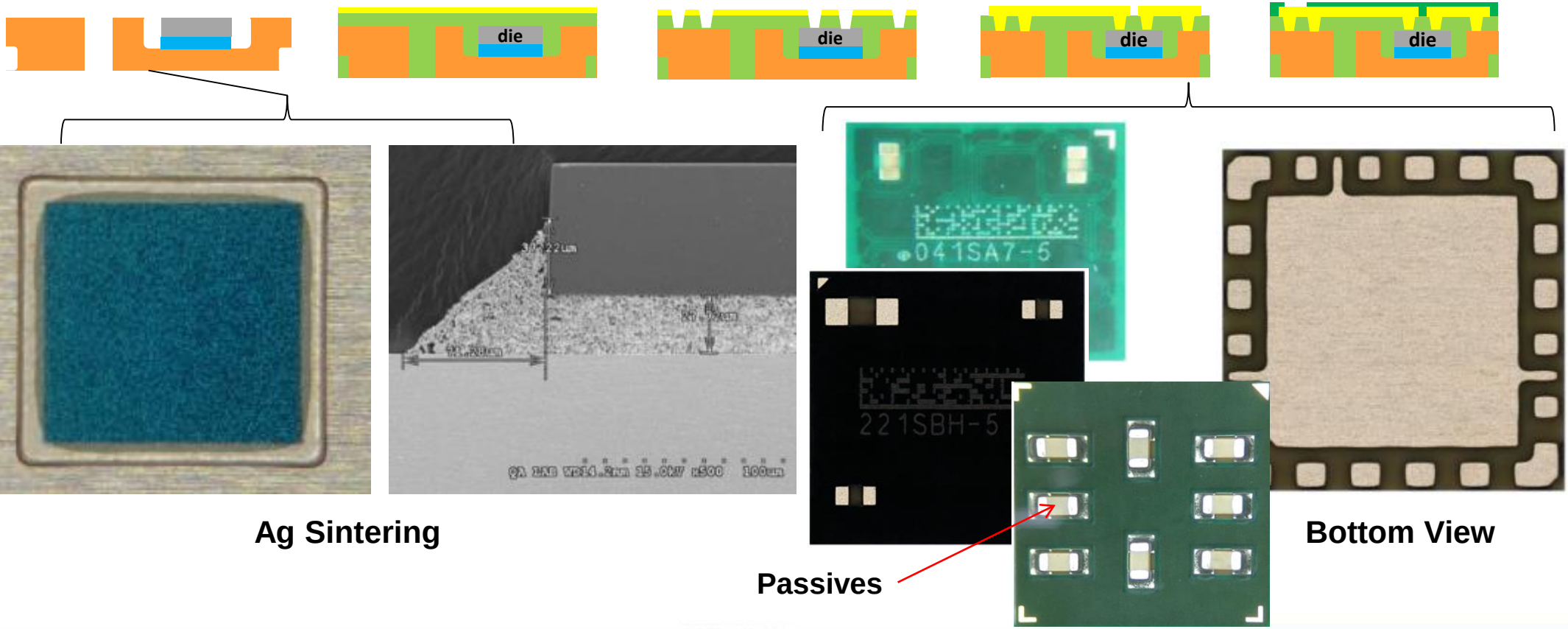
- Improve design flexibility for vertical current device.
- Highly Integration – Smaller form factor



P1 P2 P3

aEASI P2

Die attach | Lamination | Laser drill | Plating & Patterning | S/M, Marking, Singulation

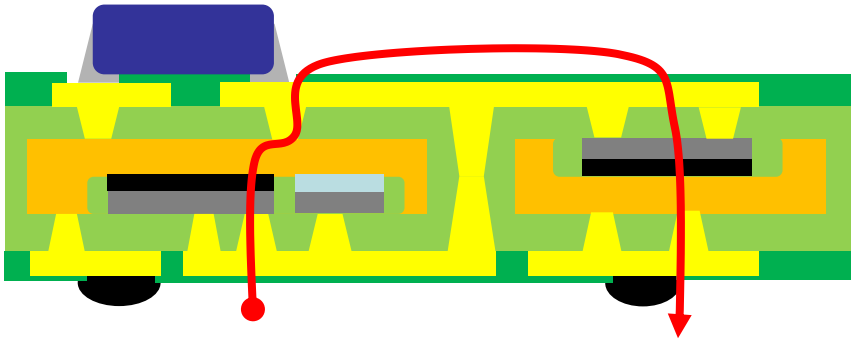


Ag Sintering

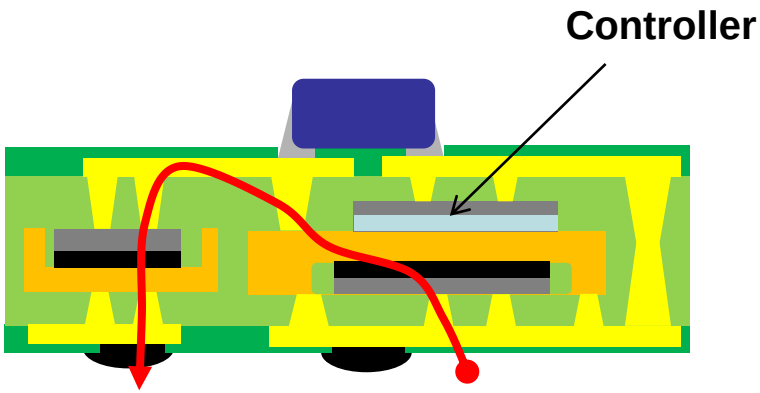
Passives

Bottom View

aEASI P3

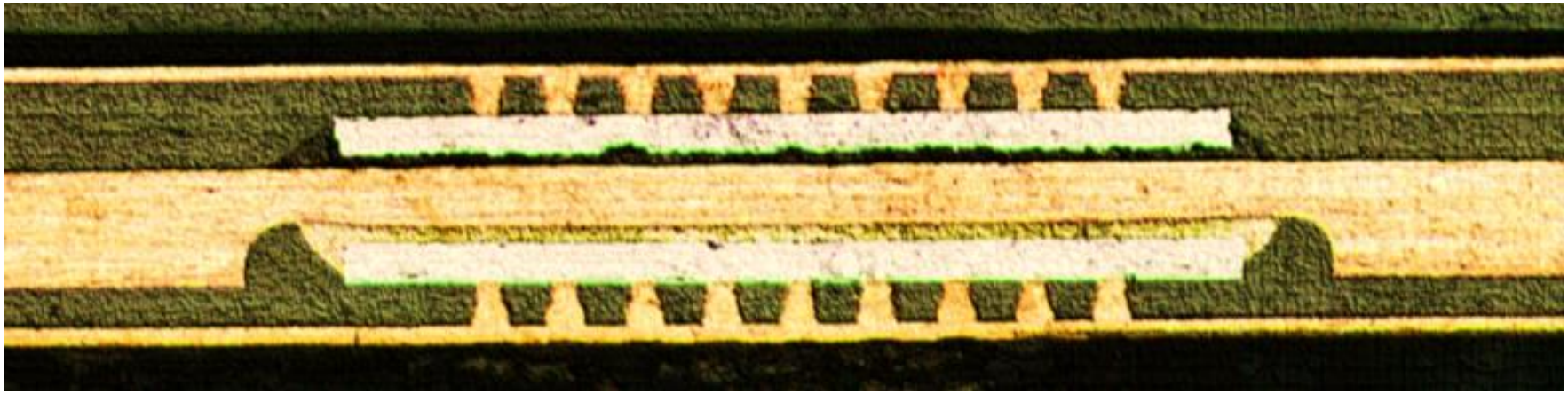


P3

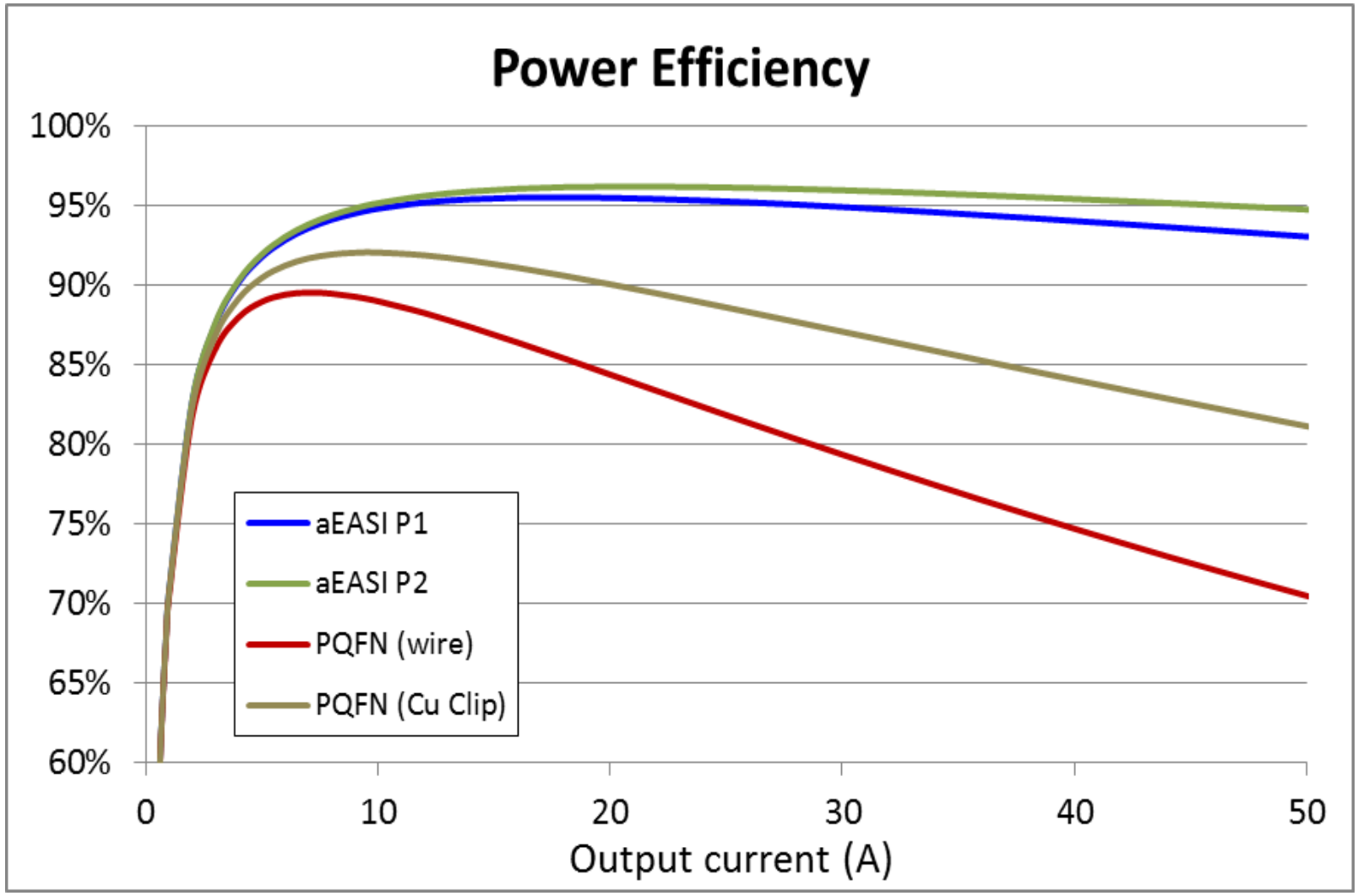


P3 – Stack

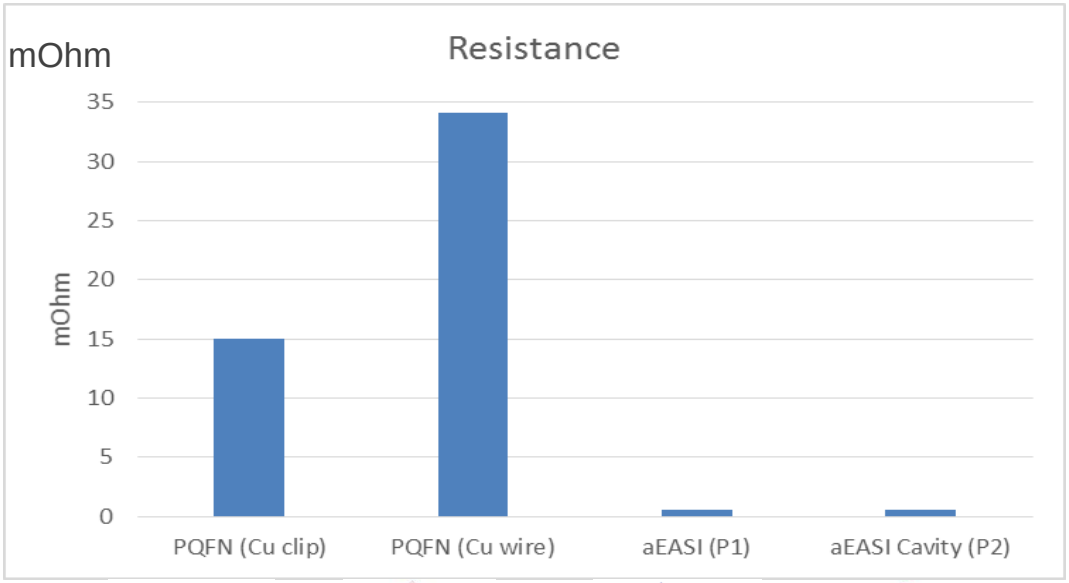
(3D stacking in Chip Embedded Structure)

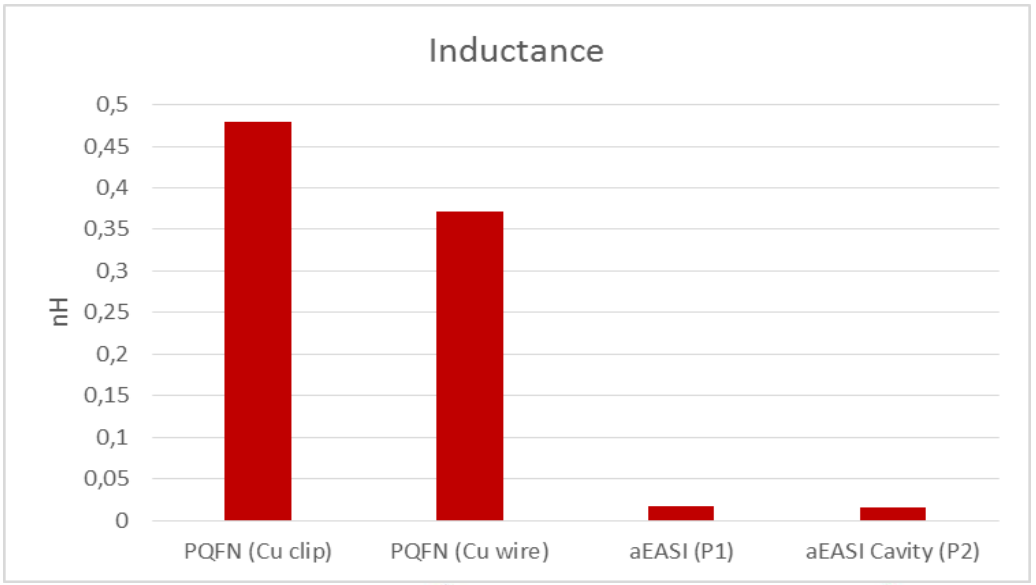


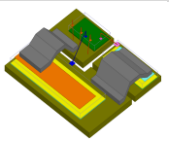
Power Conversion Efficiency

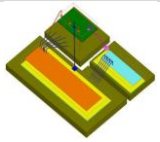


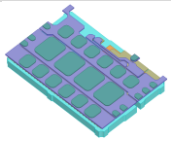
Packaging Parasitic Resistance & Inductance

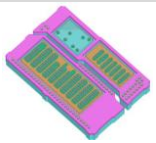


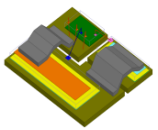


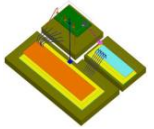


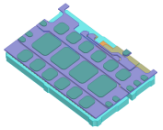


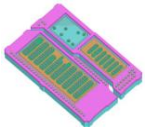


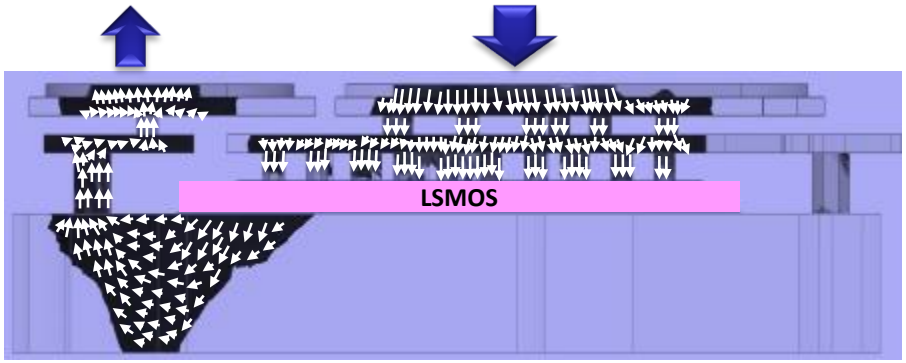


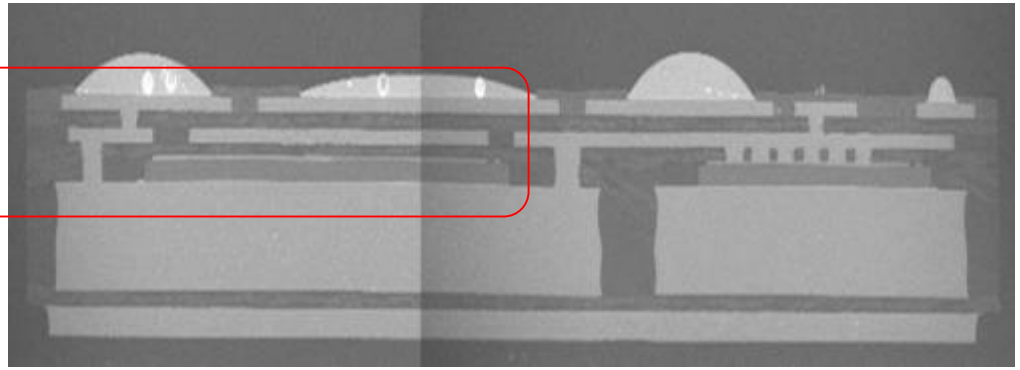




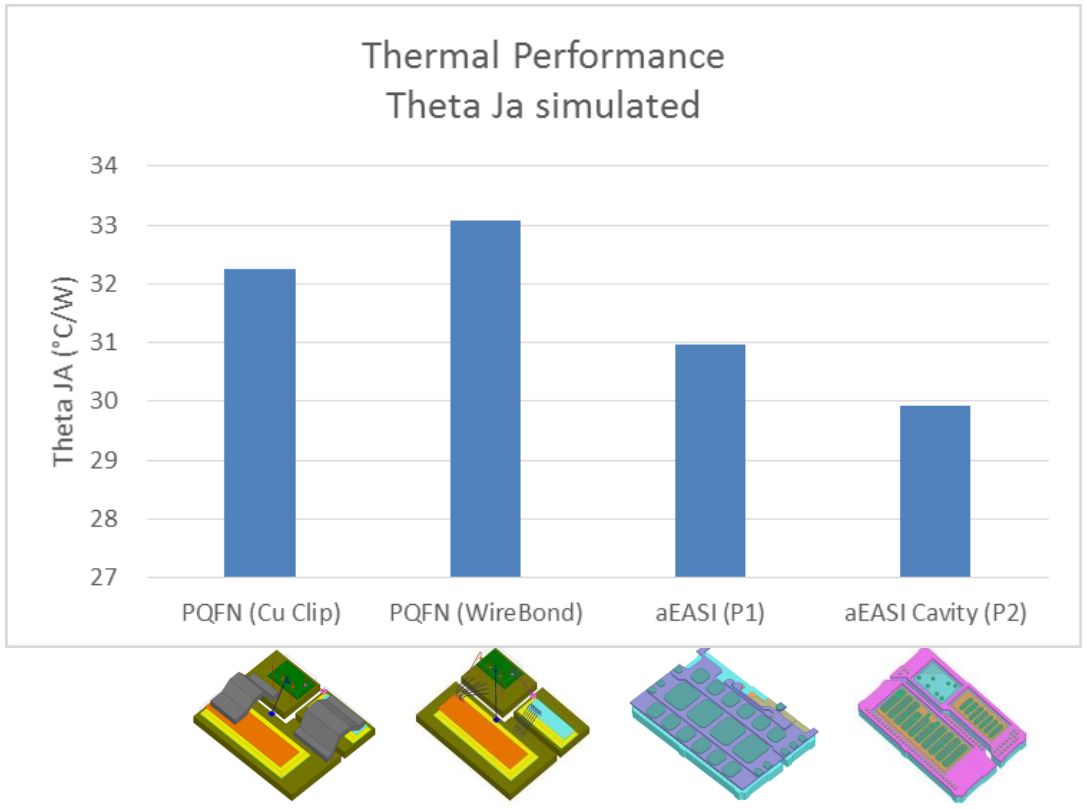


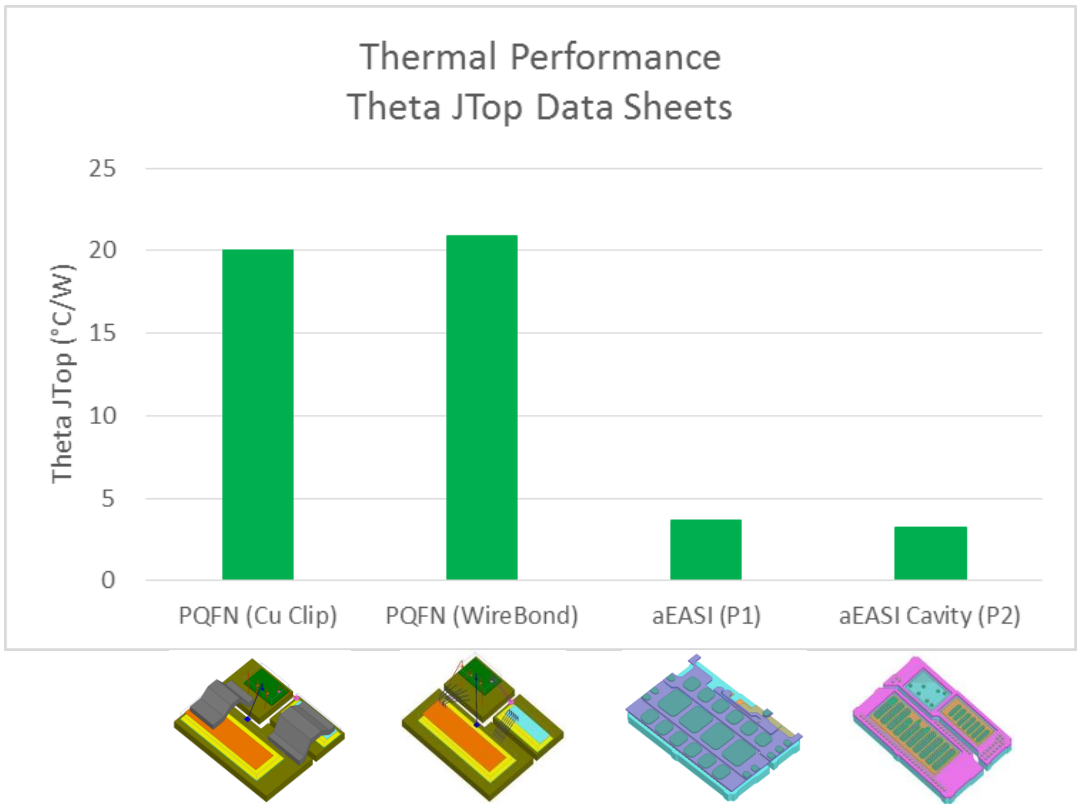






Thermal Resistance





Summary

- **Advance power device are highly demanding on high switching frequency, higher power efficiency, highly integration and smaller form factor**

- **Chip embedded technology now full fill the requirement with proven high volume production record.**
  - Smaller form factor
  - Passives integration
  - Excellent Electrical & Thermal performance
  - EMI shielding
  - Good Reliability performance

Thank you