Innovations in Chip Embedding for Power Packaging
Device continue the way to Miniaturization

Portable device driving semiconductor on
- Miniaturization ➔ More function integration
- Longer operation time ➔ High power efficiency

**Volume (mm³)**

- **Desk top**
- **Note Book**
- **Tablet**
- **Smart Phone**
- **Smart watch**

Time
Package Solution to Support Miniaturization - Power Device Packaging

Source: Yole
The Evolution Cycle & Challenge

- Higher switching frequency (IC/Wafer design Evolution)
- Smaller Capacitor/inductor
- Light weight
- Small form factor in module/package

Challenge to Package and system

- Higher current density
- High thermal requirement
- Low package parasitic
- High reliable material
- EMI interference
- Passives integration

As courtesy of Cree
Package innovation for Power SiP - Chip Embedded Technology, aEASI

- Good Thermal Dissipation
- EMI Shielding
- SMD on Top of package
- Low resistance and inductance electrical contact
- Multiple RDL Layer
- Support QFN, BGA, LGA
Die-to-Package Interconnection

- Thick Cu RDL (32 um). Minimize turn on resistance.
- Prepreg material provide >2.5KV breakdown voltage >230°C (Tg)
- 50um via diameter (Equal to Four 1 mil wire bond in conductor area)
- Cu to Cu interface. Minimize reliability risk in high current density condition
aEASI P1

- Thick Cu RDL (32um)
- Deep Via (Diameter = 120um)
- Small via (Diameter = 70um)
- Thin Die (60um)
Power SiP Device - realized by aEASI

Package Size: 5 x 5 x 0.57 mm (exclude passives height)
1 Micro Power Management Chip
Passives: 12pc
0806 x 2, 0603 x 2, 0402 x 4, 0201 x 4
RDL: 2+1 Layer

Package Size: 6.65 x 4.55 x 0.8 mm
2 power MOSFET + 1 Driver
RDL: 2+1 Layer
Continuous Innovation

- Excellent Electrical & Thermal performance
- HVM Production proven

- Thermal Enhance (Exposed pad)
- Thinner Package
- Support various footprint (BGA, LGA, QFN)

- Improve design flexibility for vertical current device.
- Highly Integration – Smaller form factor

P1 → P2 → P3 - Stack
aEASI P2

Die attach
Lamination
Laser drill
Plating & Patterning
S/M, Marking, Singulation

Ag Sintering
Passives
Bottom View
aEASI P3

P3

P3 – Stack
(3D stacking in Chip Embedded Structure)

Controller
Power Conversion Efficiency

![Graph showing power efficiency vs. output current for different components: aEASl P1, aEASl P2, PQFN (wire), PQFN (Cu Clip).]
Packaging Parasitic Resistance & Inductance

<table>
<thead>
<tr>
<th></th>
<th>Resistance (mOhm)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PQFN (Cu clip)</td>
<td>15</td>
<td>0.1</td>
</tr>
<tr>
<td>PQFN (Cu wire)</td>
<td>35</td>
<td>0.5</td>
</tr>
<tr>
<td>aEASI (P1)</td>
<td>20</td>
<td>0.2</td>
</tr>
<tr>
<td>aEASI Cavity (P2)</td>
<td>10</td>
<td>0.15</td>
</tr>
</tbody>
</table>

LSMOS
Thermal Resistance

Thermal Performance
Theta Ja simulated

![Thermal Performance Bar Chart](chart1.jpg)

- PQFN (Cu Clip)
- PQFN (WireBond)
- aEASI (P1)
- aEASI Cavity (P2)

Thermal Performance
Theta JTop Data Sheets

![Thermal Performance Bar Chart](chart2.jpg)

- PQFN (Cu Clip)
- PQFN (WireBond)
- aEASI (P1)
- aEASI Cavity (P2)
Summary

- Advance power device are highly demanding on high switching frequency, higher power efficiency, highly integration and smaller form factor

- Chip embedded technology now full fill the requirement with proven high volume production record.
  - Smaller form factor
  - Passives integration
  - Excellent Electrical & Thermal performance
  - EMI shielding
  - Good Reliability performance
Thank you