APEC Presentation

Reliability of 3D Integrated Power Packaging

F. Patrick McCluskey CALCE/Dept. of Mechanical Engineering University of Maryland, College Park, MD 20742 <u>mcclupa@umd.edu</u> (301) 405-0279





Trends in Power Electronic Packaging

- Increasingly the key product differentiator is size, weight, power efficiency and cooling (SWaP-C)
- Power Electronics are being used at
 - Increased load levels
 - In harsher environments
 - With denser packaging schemes
- Drive towards a fully integrated power electronics module.
 - Vital subsystems are placed in closer proximity to the power module.
- Physics-of-failure concepts enable reliable designs for future systems.







Physics of failure

- The basic premise of PoF is that all failures can be traced to a fundamental degradation mechanism that is operative for the design used and the environment in which it is expected to operate.
- PoF tools model the stress-failure relationship for the dominant environmentally-induced failure mechanisms. These relationships are used to compute expected life and compare it to requirements.
- PoF provides a systematic approach to plan, conduct, implement and evaluate accelerated life tests, especially under multiple load conditions.



Implementing Physics of Failure

- Define realistic product requirements.
- Define the design usage profile.
- Characterize the design.
- Conduct a virtual qualification
- Identify potential failure sites and mechanisms.
- Determine overstress and destruct limits
- Develop an accelerated test plan
- Characterize individual failure mechanisms
- Conduct an accelerated life test and update failure models
- Conduct a reliability assessment







Probabilistic PoF Reliability Assessment

A PPoF approach can be used to determine reliability. This includes the following:

- Estimating MTTF and FFOP for each element failing by each failure mechanism
- Using a fault tree analysis to see which components are in series
- Using probabilistic mathematical approaches to combine the independent distributions for identical or non-identical parts failing due to identical or non-identical failure mechanisms



Center for Advanced Life Cycle Engineering

FA

www.calce.umd.edu





3D Integrated Packaging

- Moving from 2D packaging of discrete components on a PWB to 2.5D – 3D stacked modules
- Examples are:
 - Power Supply on Chip (PSOC)
 - Power Supply in Package (PSIP)
- These packages contain embedded actives, embedded passives, embedded thermal management, and attachments.
- Additive manufacturing may be used for true 3D structures









Increasing Power Density \rightarrow Integrated Cooling

- Increasing power densities in electronics require more effective cooling solutions, particularly for power electronics modules.
 - Dissipation levels on the order of several hundred watts/cm² are not unusual.
- Controlling temperature is critical to device performance and reliability.
 - Performance
 - Slower switching, Higher leakage current, Higher forward voltage
 - More Losses (Thermal run-away)
 - Reliability
 - Many failure mechanisms occur more quickly at higher temperatures.
 - Others occur more quickly with wide temperature swings.







From Wirebond → Sintered Interconnect

"Traditional" Wirebond



- Chips interconnected with 125-375 mm diameter wire.
- Dice soldered to a thick metalized ceramic substrate (e.g. DBA, DBC) which is soldered to a heat spreader.
- Most heat (>85%) dissipated from the back of the die through the substrate to the heat spreader.

Sintered Interconnect



- Chip bonded top and bottom with a permanent attach.
- Eliminates wirebond failures
- Supports double sided cooling
- Need high temperature attach robust against delamination and cracking

Z. Liang, "WBG Inverter Packaging," 2013 U.S. DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review





Permanent Attach Materials



Adhesives



TLPS

- The traditional die attach for power modules was a high lead solder. (e.g. PbSn5 or Pb2Sn2.5Ag)
- RoHS has required the removal of lead from most solder since 2006, but has permitted the use of lead in high temperature melting solders until mid 2016 with review in 2014.
- This exemption (7a) is now valid, but a replacement is needed that:
 - Has T_m > 250°C
 - Has excellent wettability
 - Is reliable due to ductility
 - Is commercially competitive
- Exemption may be cancelled if an alternative is available and proven.
- Four types of materials are being considered as substitutes.



Solders









Sintered Interconnect

Reflow Attachments

Solder	T _m	Issues
Sn37Pb	183°C	 Low T_m, Regulatory Restrictions
SAC305	217°C	 Low T_m, Short Fatigue Life
Pb5.0Sn2.5Ag /other high Pb	296°C	High process tempRegulatory restrictions
Bi-Ag Alloys	262°C	 Small elongation, brittle Limited wetting Low thermal conductivity
Au20Sn	280°C	High process tempHigh cost
Au12Ge	361°C	
Au3.2Si	363°C	
Zn6Al	381°C	- Complicated processing
Zn5.8Ge	390°C	 Limited wetting High process temp

Sintered Silver

Combine moderate range processing temperatures (225°C - 275°C) with 30-40 MPa pressure to convert a silver powder paste into a porous solid joint. Order of magnitude better power cycling reliability than soldering [1].







calce

TLPS Attach Technology

- TLPS (Transient Liquid Phase Sintering) is a liquid-assisted sintering process during which a low melting temperature constituent, A, melts, surrounds, and diffuses in a high melting temperature constituent B.
- Intermetallics with high melting temperatures are formed by liquid-solid diffusion
- TLPS systems can be processed at low temperatures but are capable of operating at the high melting temperatures of the intermetallic compounds.



TLPS joints with flux can be formed from low cost material systems (Cu-Sn, Ni-Sn) without pressure or vacuum. Common metallizations can be joined.



Initial Arrangement Heating to T_p

Isothermal Hold

Final Alloying

University of Maryland

Copyright © 2016 CALCE

A. James Clark School of Engineering



Center for Advanced Life Cycle Engineering www.calce.umd.edu

TLPS Attach Technology

- Increasing Cu-content in Cu-Sn joints produces joints that retain their shear strength to $T > 400^{\circ}C$, but reduces strength at room temperature.
- Cu-Sn joints can be made in less than 10 minutes at P < 1 MPa, and T < 300°C.
- Ni-Sn joints made in less than 30 minutes at P < 1 MPa, and $T < 300^{\circ}C$ retain shear strength to $T > 600^{\circ}C$.





Ni-**Sn Joint** (T_m :< 30min, P < 1MPa)





A. James Clark School of Engineering University of Maryland Copyright © 2016 CALCE

Center for Advanced Life Cycle Engineering www.calce.umd.edu

AgIn TLPS: Reliability Testing

- Reliability assessment was conducted by passive thermal cycling.
- Thermo-mechanical strains were induced by the combination of thermal profiles and die sizes (3X3 mm², 5X5 mm², and 7.5x7.5 mm²).
- Specimens were inspected for damage every 50 cycles using X-ray.



Quintero, P., McCluskey, F.P., "Silver-Indium Transient Liquid Phase Sintering for High Temperature Die Attachment," *J. Microelectronics and Electronic Packaging*, 6 (2009). pp. 66-74.





Ceramic Substrate Failure Mechanisms

- Direct Bond Copper on Al₂O₃, AlN
 - Failure mode: Debonding of metallization followed by cracking in the ceramic
 - Cause: Local CTE mismatch between metallization and ceramic in temp cycling
 - DBC cracking can be mitigated by:
 - Dimpling or Copper Metallization Thinning
 - Increased Fracture Tougheness (Additions)
 - Bonding of Substrate to Copper Heat Sink
- Direct Bond Aluminum
 - − Cu: σ_y ≈ 70 MPa → High stresses in ceramic and Cu-ceramic interface → short time-to-failure under system temperature excursions
 - Al: σ_y ≈ 20 MPa → Reduced susceptibility for ceramic fracture, but: extensive deformation of metallization → Hillock formation











Polymer Substrate Failure Mechanisms

- Conductive Filament Formation
 - Creation of thin metal conducting filaments between traces and vias on the board at high voltage when subjected to thermal cycling and humidity
- Solder Fatigue
 - PTH and SMT components
- PTH/Via Fatigue
 - Fatigue cracking of the walls of a plated through hole or via as a result of thermal cycling. Crack can propagate around the circumference of the plated through hole (PTH) or Via when cyclic stresses exceed the fatigue strength of the copper wall
- Corrosion
- Creep Corrosion/Dendrite Growth
 - Electrochemical metal degradation









Reliability of Embedded Capacitors

- Methods for integrating capacitors into 3D structures
 - Embedded capacitor films
 - Pin holes/partial discharge
 - Metal migration
 - Dielectric breakdown
 - Embedded capacitor devices
 - Cracking and delamination thermomechanical stress
 - Swelling and delamination hygrothermal stress







Embedded Inductors

- Planar Magnetics
 - Via fatigue
 - Delamination
 - Core adhesion
- Deposited Inductors
 - Grain structure and flux domains



Planar inductor (cut view)









Center for Advanced Life Cycle Engineering www.calce.umd.edu



Embedded Manifold-Microchannel Coolers for High Heat Flux Power Electronics

- Manifold-Microchannel coolers can be embedded directly into the substrate or chip to provide localized heat removal at high volumetric rates from the backside of active ICs and power electronic devices.
- These coolers take many forms. For example single vs. two-phase, silicon vs. ceramic substrates and different alloys, filter size, working fluid, fluid velocity, and temperature.
- They are used to overcome thermal limits that can cause power electronic devices to operate at voltages and currents below their inherent electrical limits.
- No "one-size-fits-all" reliability solution.



3D rendering of Si microchannel cooler









Force Fed Two Phase Manifolded Cooler

- Force Fed Microchannel Heat Exchanger (FFMHX) design. Series of parallel microchannels with perpendicularly oriented manifold to distribute flow.
- Micro-grooved surface is manufactured in single-crystal Silicon Carbide (SiC).







Reliability Aspects of MCCs

<u>Erosion</u>: Entrained particles impinge on the walls altering channel geometry and generating particulates.

<u>Corrosion</u>: Relatively uniform dissolution of material into solution, and formation of brittle oxide layers.

<u>Clogging/fouling</u>: Entrained particles become attracted to channel surfaces. Layers of particles form eventually leading to full blockage.



Erosion-corrosion phenomena ⁵





Clogging of microchannels

Previous studies have shown that particulate build-up and clogging <u>within</u> the microchannels are not likely to occur.



Particulate formations on the fin surfaces connect to block the channel entrance¹⁸



Fouling occurs in the manifold while clogging occurs at the channel entrances $\frac{19}{19}$

- Major location of fouling is within <u>header/manifold</u> region due to the lower shear stress and abrupt changes in flow direction as fluid enters channels.
- One of the best ways to control particle agglomeration and build-up is by adjusting pH and very stringent particle filtering controls (e.g. less than 0.5µm).





Thermal Isolation







Reliability of Additive Manufacturing

- High level of porosity
 - Increased compliance
 - Lower strength
 - Fracture initiation sites
 - Potential fracture arresting
- Horizontal artificial grain boundaries





gure 1 – Evolution of a 3D magnetic flux sensor illustrating increased levels of 3D component placement and conductor routing, leading to improved integration and packaging.

- Knit strength of materials across the layers
- Materials compatibility and interactions







CALCE Prognostics and Health Management

CALCE's Approach to PHM

Remaining Useful Life (RUL) Assessment

Value







Electrothermal Mechanical Modeling

- Electrothermal Model Created
 - Power Loss \rightarrow Temperature Increase
- Degradation Model Added
 - Temperature Increase \rightarrow Attach Fatigue
 - Fatigue \rightarrow Increased Thermal Resistance
 - Increased Resistance \rightarrow Temp. Increase
- Precursor Parameter Identified
 - Temp. Increase \rightarrow Voltage Increase
- Damage Correlated with C-SAM
- Monitor Voltage Increase
- Estimate Remaining Life





Conclusions

- 3D integrated power electronics will use new packaging technologies the reliability of which will need to be understood and modeled.
 - Sintered Interconnects
 - Embedded Actives and Passives
 - 3D Integrated Thermal Management
 - Additive Manufacturing
- Power electronics will become ever more important as it is the critical enabling technology sitting at the intersection of renewable power generation, reliable power distribution and transmission, and efficient power utilization and storage.
- Addressing the reliability issues inherent in compact and high power density packaging which includes integrated thermal management will be the most important research area for realizing the full potential of power electronics.



