ASE GROUP

New Wave SiP solution for Power

Vincent Lin

Corporate R&D

ASE Group

APEC March 7th, 2018 in San Antonio, Texas.

Outline

- **Challenges Facing Human Society**
  - Energy , Environment and "Traffic"
- **Autonomous Driving and Technologies Needed**
  - A approach to reduce energy and resource
  - Sensors, GPU-Based AI, 5G and Cloud
  - The bottleneck : Wireless /PMIC and Inter Data Center
- **SiP Solutions for Power**
  - Tool Box of Passive integration for RF and PMIC
  - Tool Box of Si-Photonic Packaging
- **Concluding Remarks**

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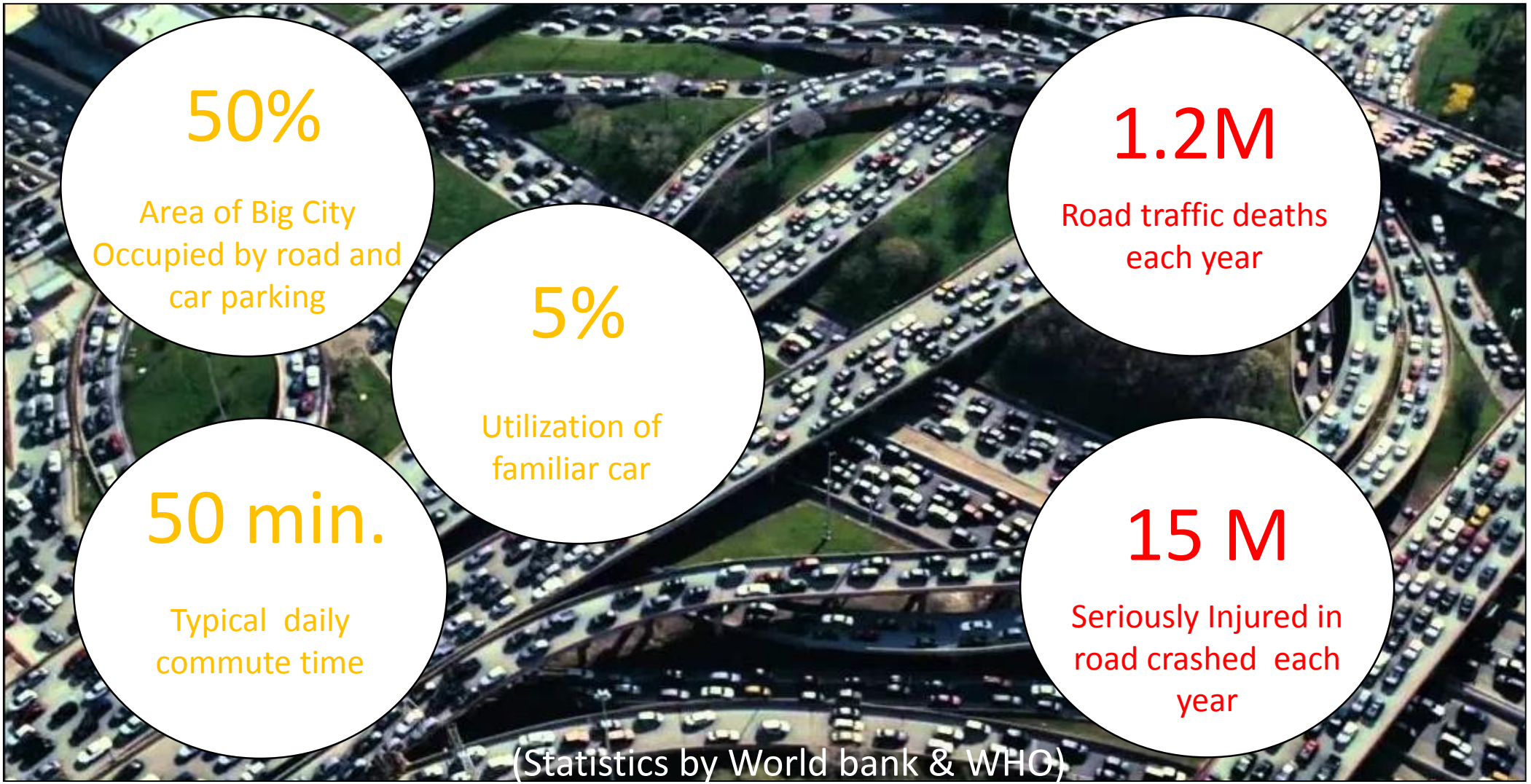
Traffic

Resource Wasted : Land, time and Power

Life-and-Death Matter, Must to take actions



Autonomous Driving: Technologies needed

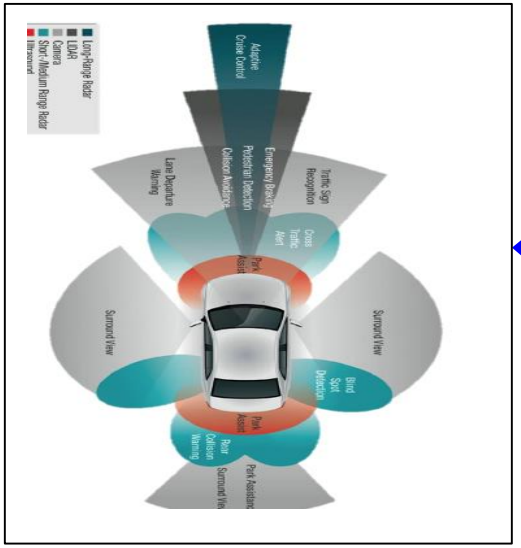
AI-GPU based

Sensor

5G Platform

Optical interconnection

CAR



CONNECTIVITY

Training

Inference

DATA CENTER

100Mps to 1Gps

100Gps to 1Tps

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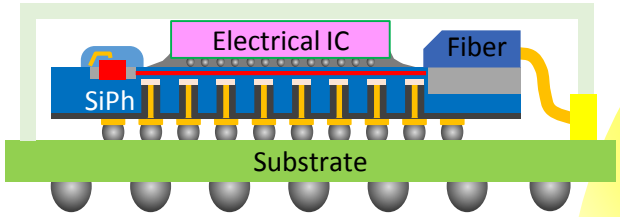
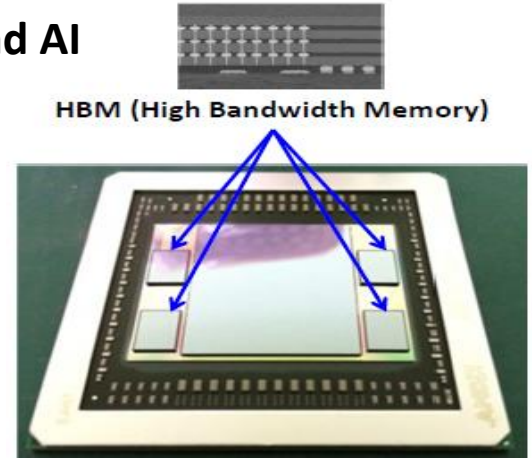
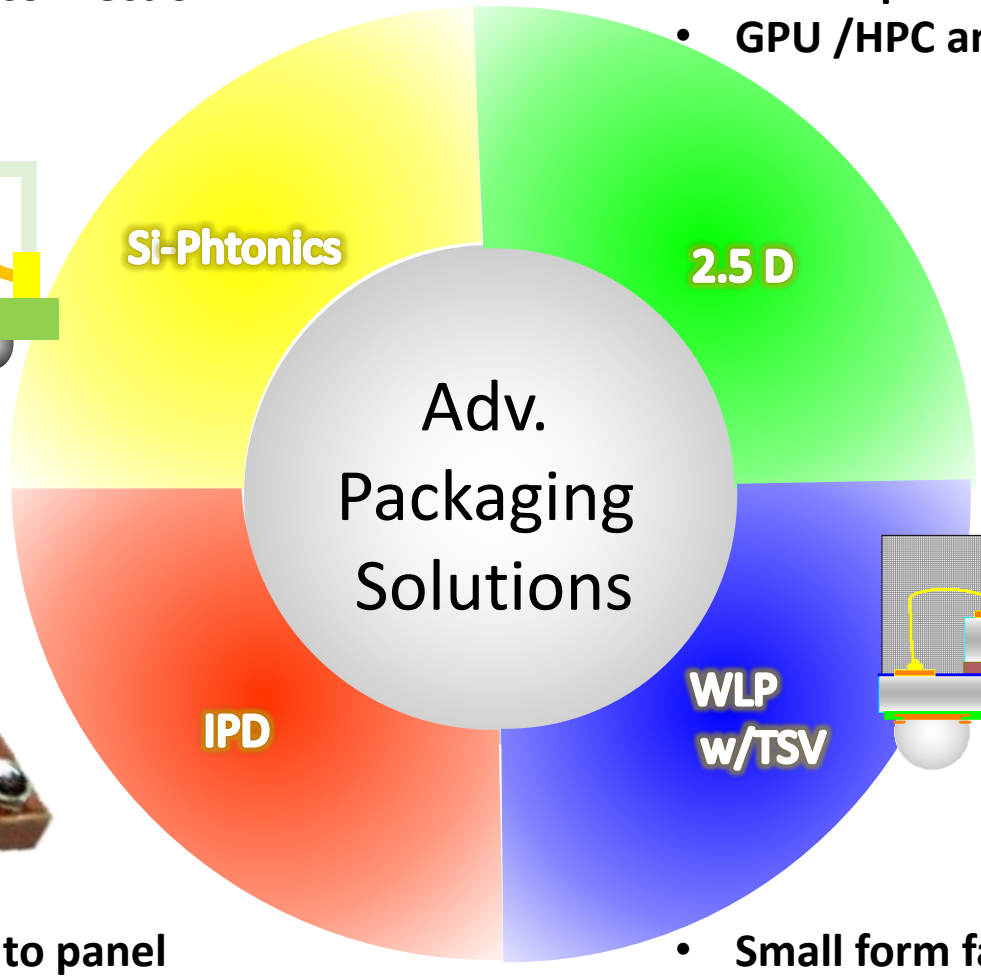
Heterogeneous Integration Solutions

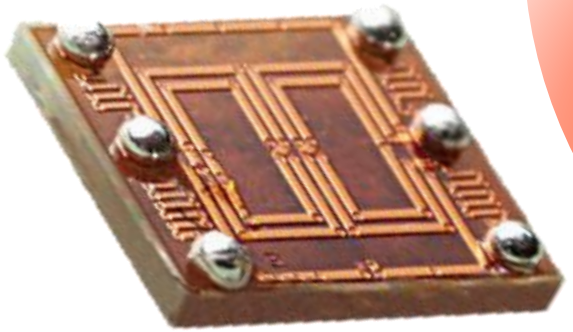
- Ultra-high speed (>100Gps)
- E-O modulation/interconnection
- Data center

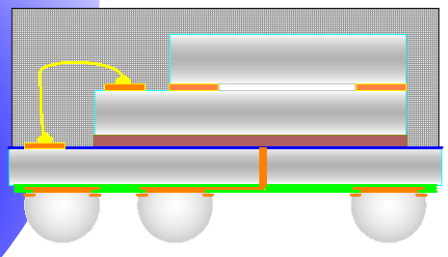


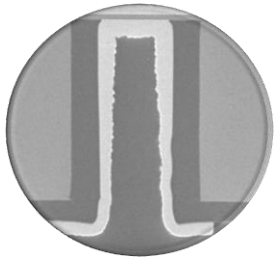
- Ultra-high density I/O (>200K/PKG)
- Si-Interposer
- GPU /HPC and AI





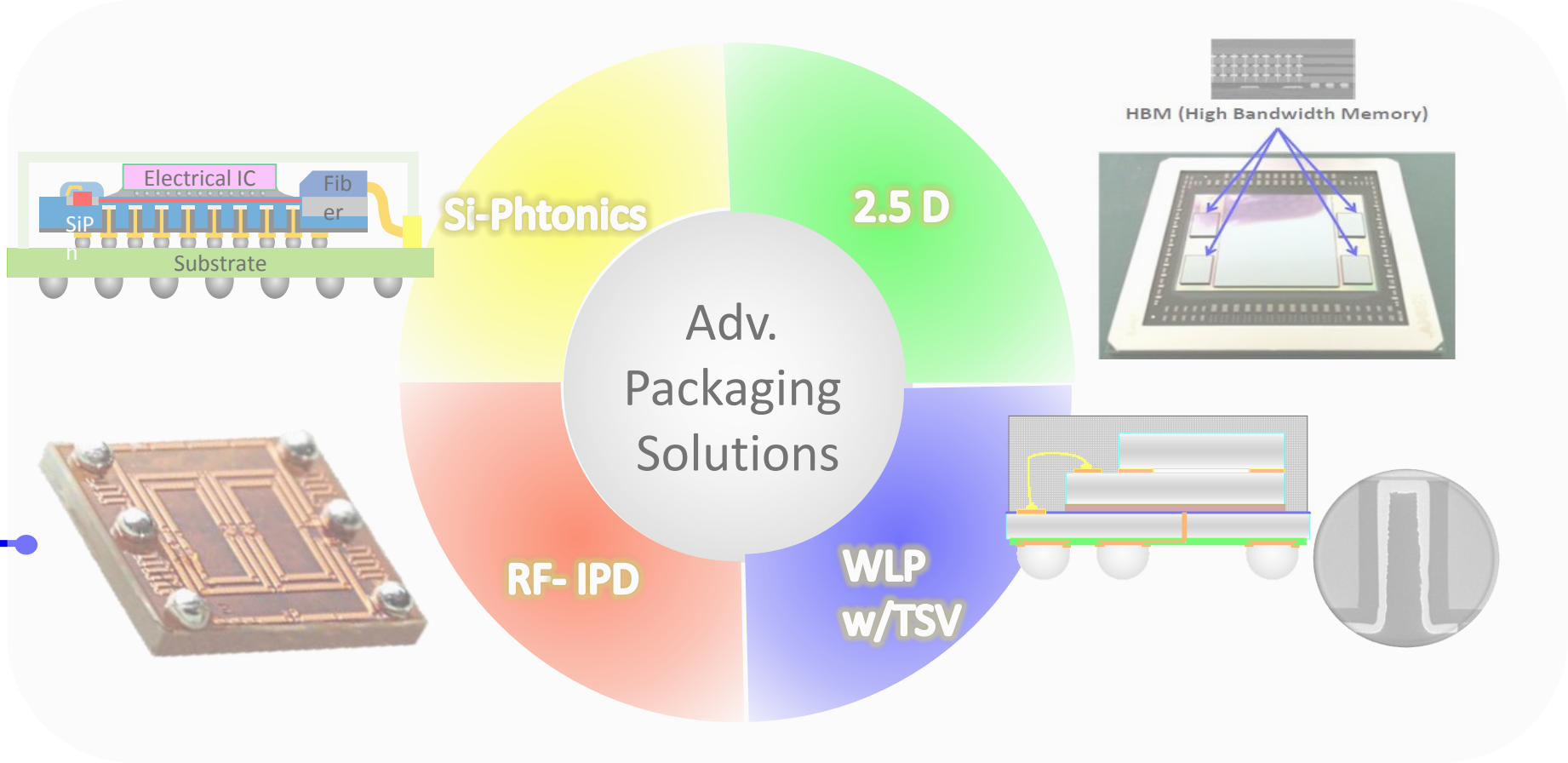






- Glass platform : wafer to panel
- Passives (L/C) & PKG integration
- RF & PMIC

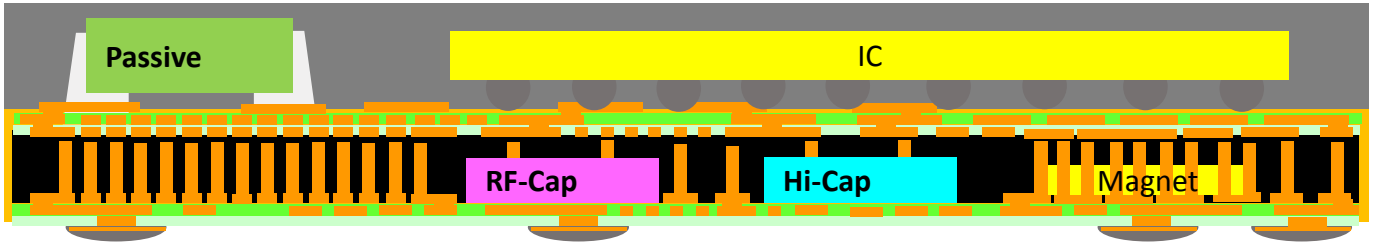
- Small form factor WLP (<1mm^2)
- TSV-Last for 8" wafer
- Sensors



- **Passive integration :**
  - Mission Statement of **HyPas Platform**
  - Evolution of RF-Passives integration : 2D/ 3D TGV/ 3D Cu-P
  - **Inductor : RF to PMIC , Integrated with Magnet**

Mission Statement of HyPas Platform

- ✓ **IPD vs HyPas:**
  - IPD : Integrated Passives (L/C) Device
  - HyPas : Hybrid/ High Performance Passives/ Packaging integration solution
- ✓ **HyPas Key Features:**
  - High AR Cu-P 3D Structure
  - Embedded with Special Material : Ferrite Hi-Ind, and Hi-Cap
  - Capex/Tool compatible with ASE Panel level FO Plan



RF-Ind
- 1~20nH
- 140umt

RF-Cap
- Cap. Density: 0.58nF/mm^2
- BD Voltage > 70V
- < 100umt

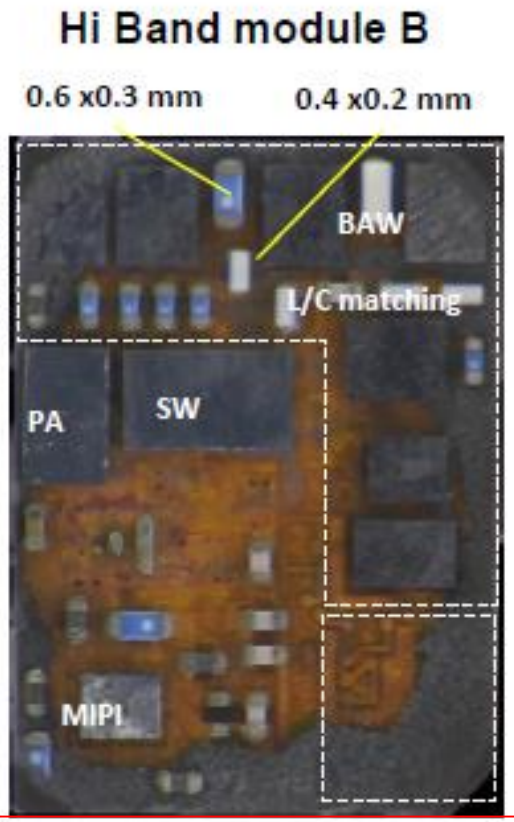
Hi-Cap
- Cap. Density: 200nF/mm^2
- BD Voltage > 5V
- < 100umt

Hi-Ind
- 0.1~1uH
- 140umt
- Embedded Magnet

Joint development w/ Tier-1 Passives Company

Typical RF FEM (PAMiD) Scenario

- 7 x 5 mm, 6-7 layers coreless substrate → Module size reduction trend : 20% per year
- 7-10 Acoustic Filters (BAW/SAW)
- > 30 passives (most of 0402 Inductor) → IPD solution to reduce the discrete passives
- PA and Switch

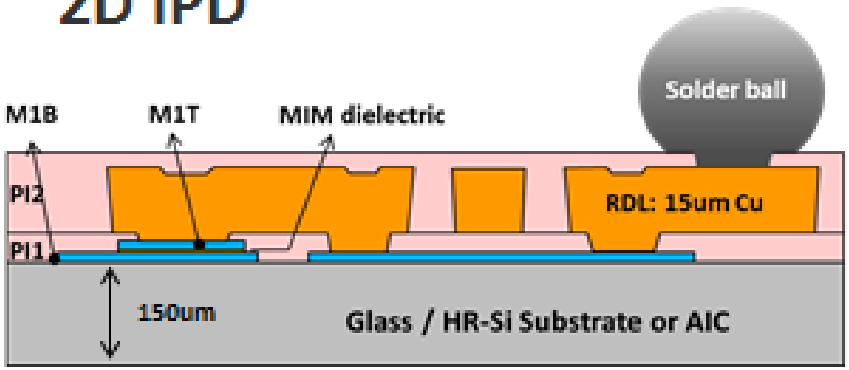


(Source: Yole)

Need have solution of Acoustic Filter size reduction and Passives (L/C) integration

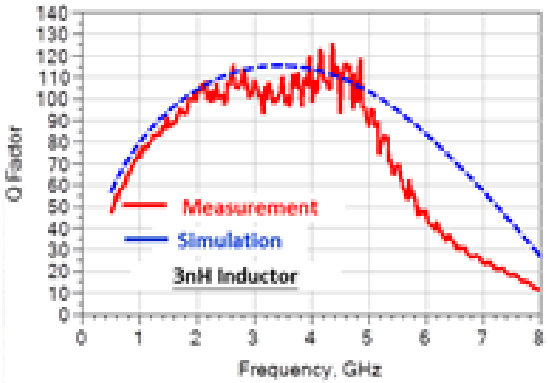
2D vs 3D IPD

2D IPD



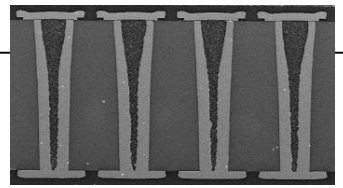
2D inductor :

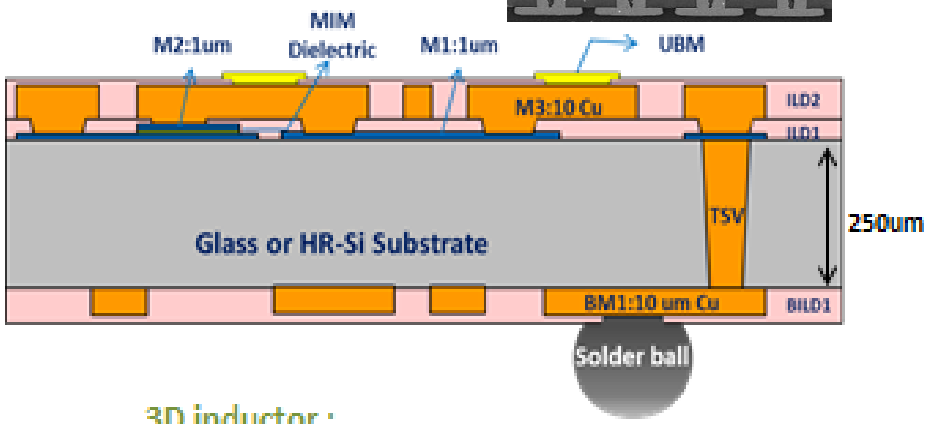
3xRDL
(15/15/10 um)



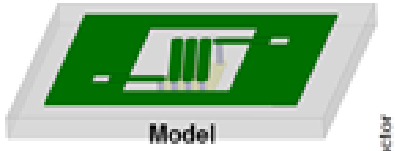
Q >60@1GHz, Peak Q ~100

3D TGV IPD

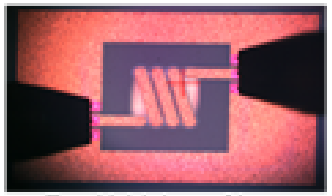




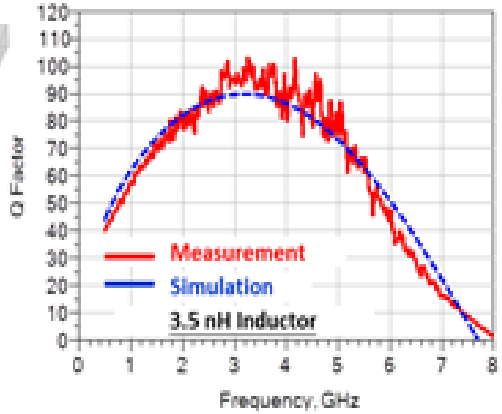
3D inductor :



Model



Test Vehicle on Glass

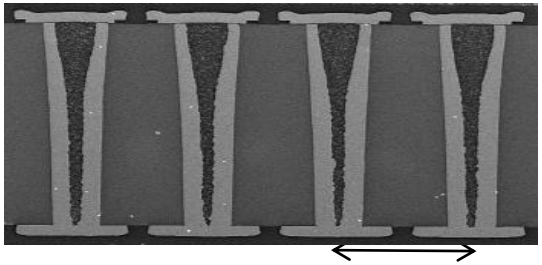


Q >60@1GHz, Peak Q ~100

50% size reduction

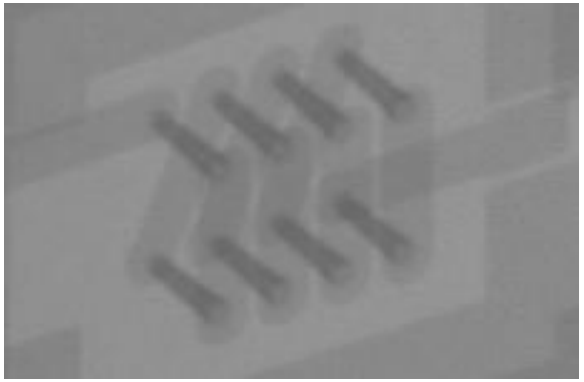
3D Solution: TGV vs Tall Cu-P

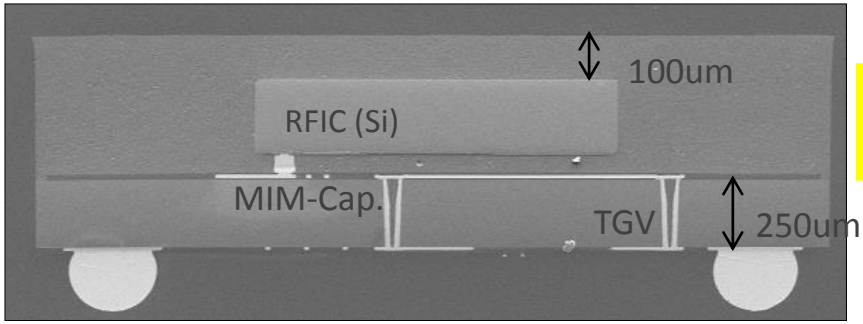
TGV



250um

130um

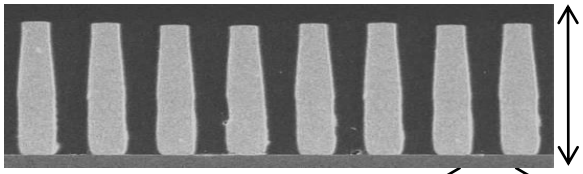




2.4x2.4x 0.8 mm

Tall Cu-P

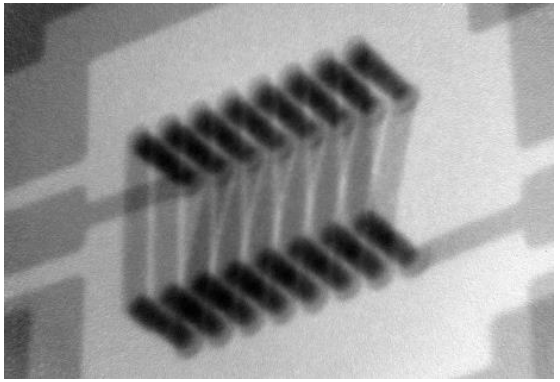
1/2
Via Pitch



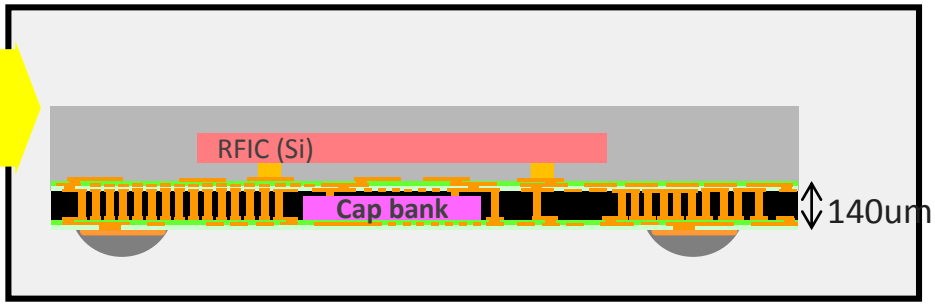
140um

70um

2X
Inductor Density

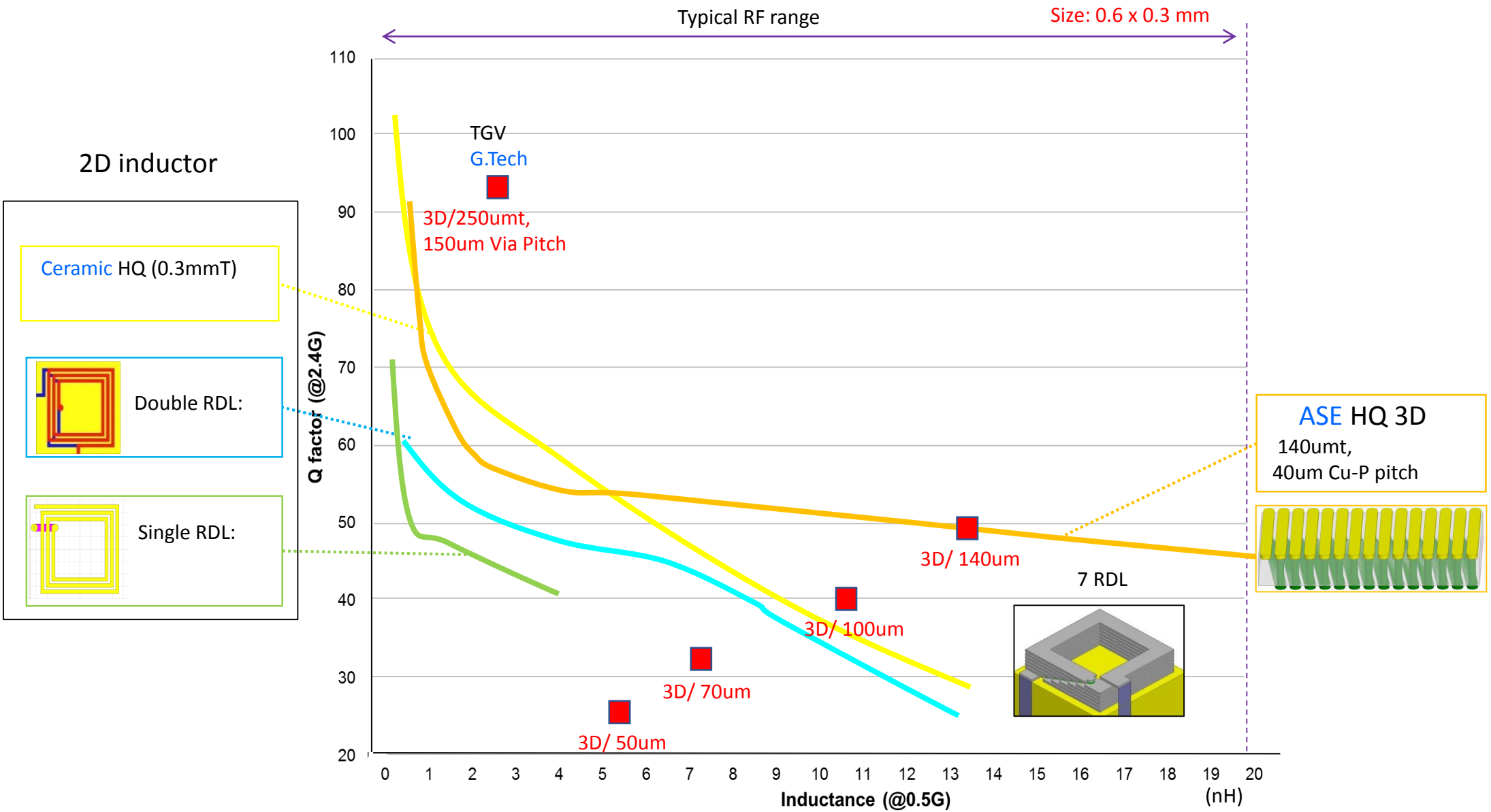


Much Smaller
Module

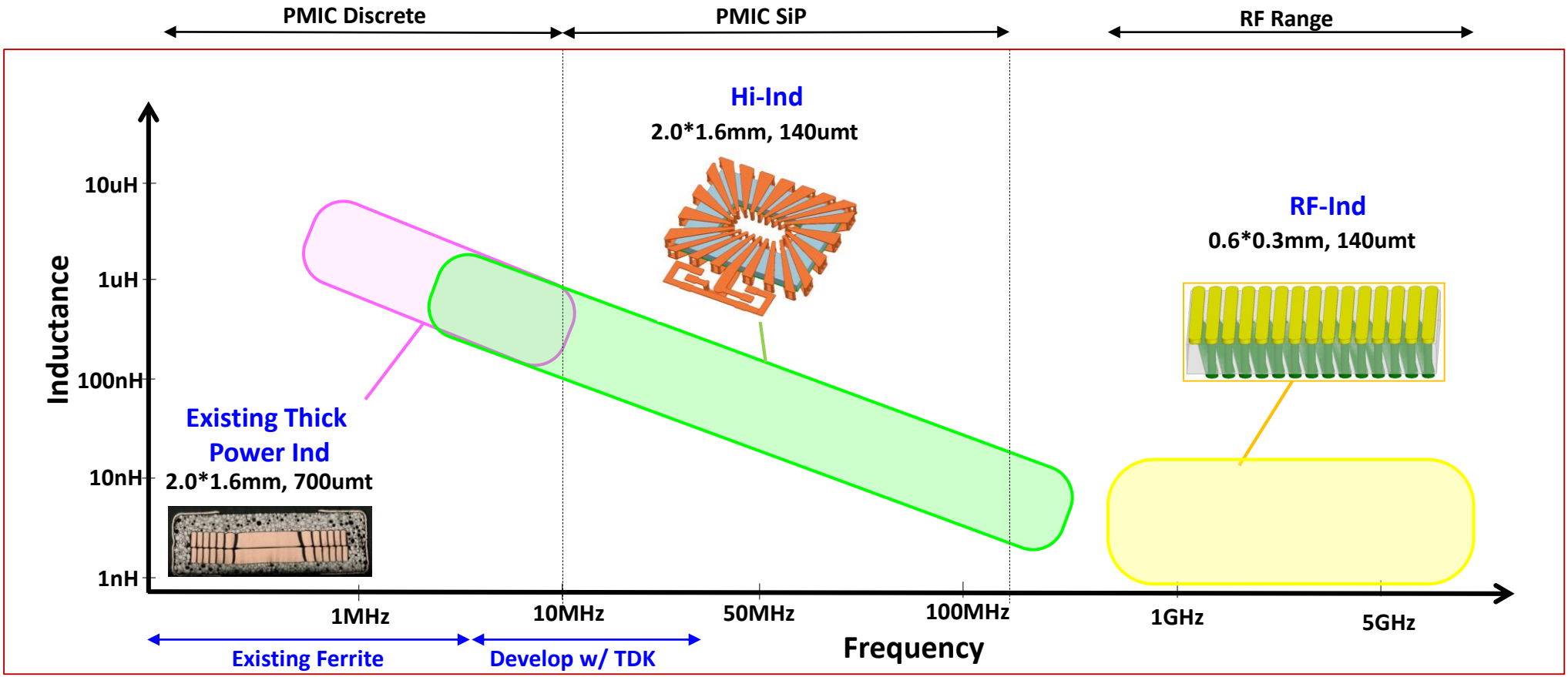


< 2x2 x0.5mm

Benchmark Discrete Inductor & ASE win Design Rule/Strategy



Inductor : RF to PMIC , Integrated with Magnet



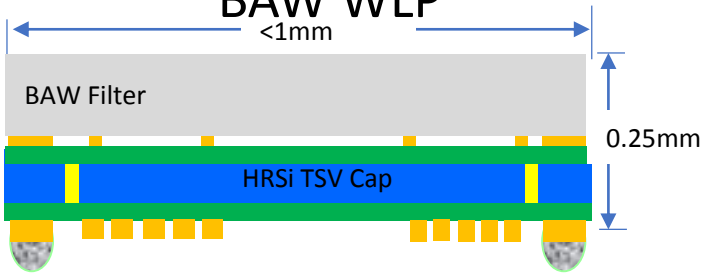
Special Magnet material :

1. Bulk magnet thin down to 100um.
2. Material can support to 30MHz.
3. Ring pattern machining.

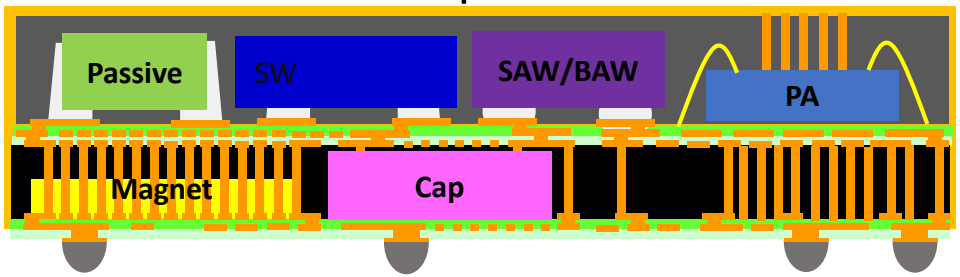
Tool Box of RF Packaging

RF Key Devices	Active	PA, Switch
	Filter	BAW, SAW, Passives
ASE Corp. Technology	Passive Integrated Substrate	2D IPD, Cap +TSV, 3D IPD
	Wafer Level Technology	W2W Bonding, C2W Bonding, Bump/ Cu Pillar, RDL/AIC, WL Molding

BAW WLP



Compact FEM



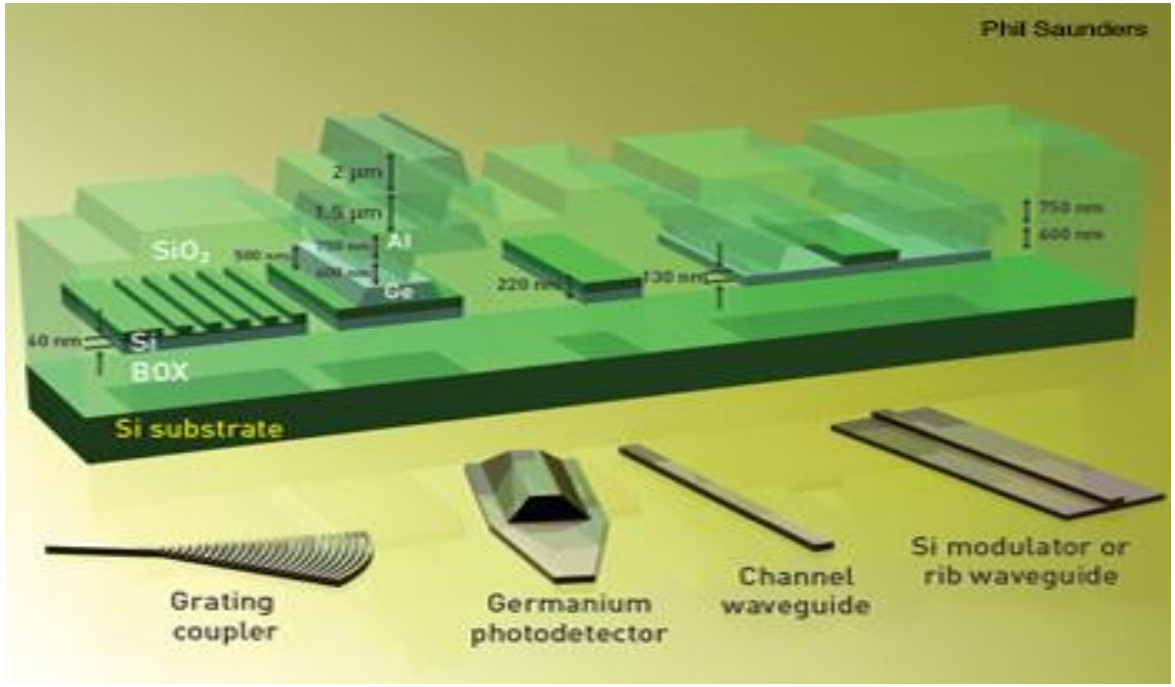
Si-Photonics Packaging Overview:

- Customer Voice- Data Center Switch Challenges
- Typical SiPh Packaging Structure- Module level and System level
- SiPh Module Integration approaches for DC Switch
- Tool Box Planning of SiPh Packaging

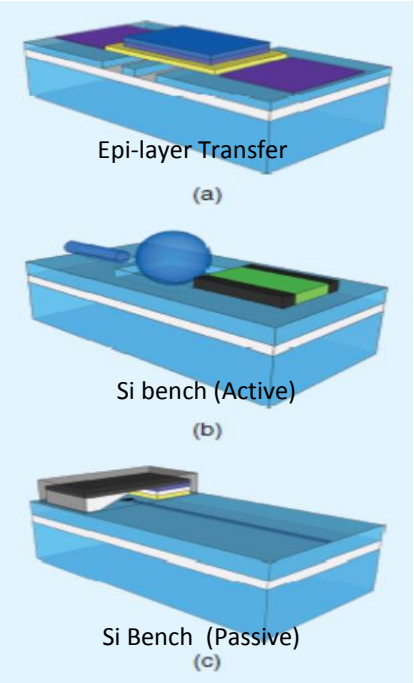
Silicon Photonics (SiPh)

- CMOS Compatible SOI-platform : Planner Wave guide (λ = 1.3 -1.5µm)
- Light Source : Discrete or Epi-Layer transfer
- E-O Modulator : Robust MZI Si-WG instead of Direct LD modulation
- Receiver : integrated with SiGe Photo Diode
- Optical coupling : micro structure instead of discrete lens to improve the eff.

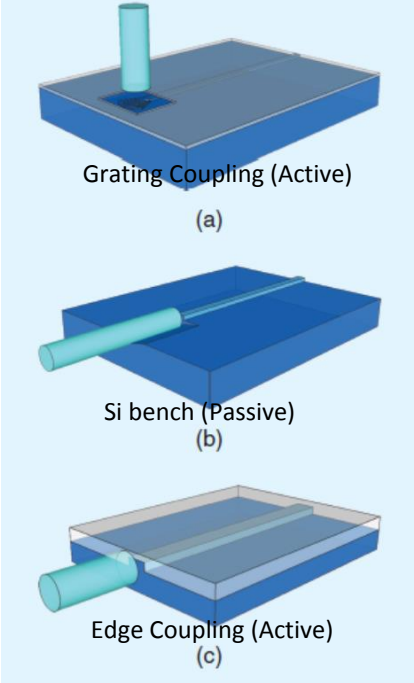
CMOS Photonic



Laser Bond Options

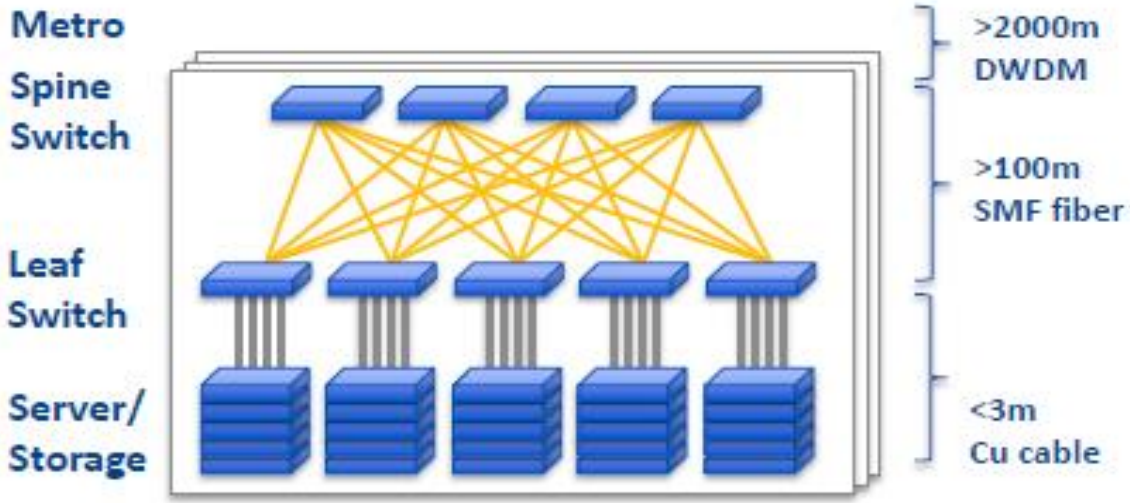


Fiber Attach Options

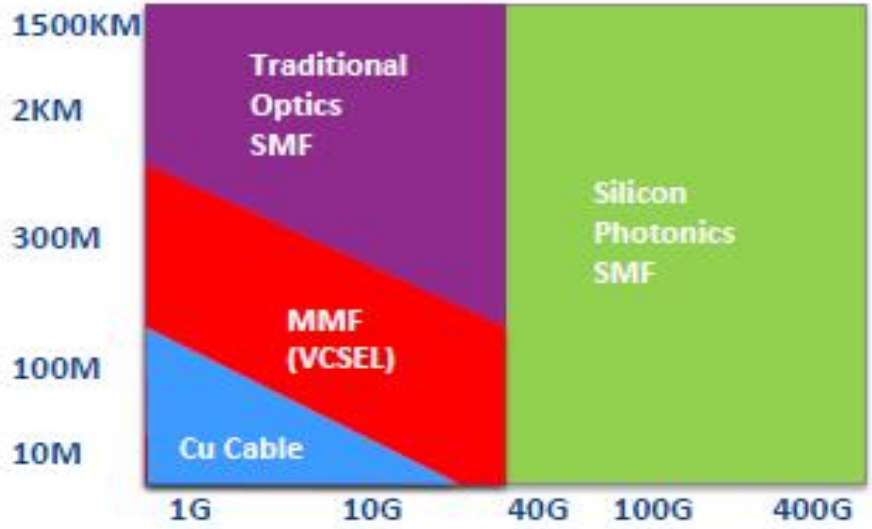


Data Center Architecture

- 2-tier leaf-spine network



- Distance vs. Data rate

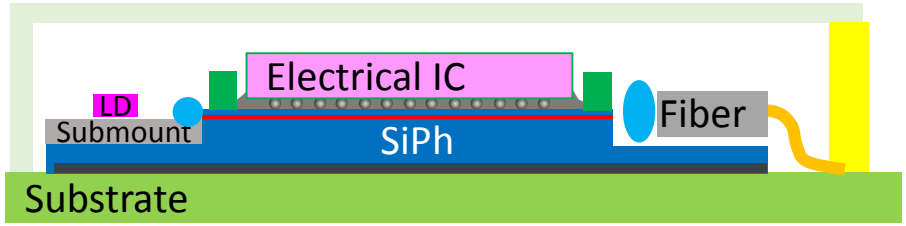


- Top of rack high switching capacity demand increased and more fiber optics are used
- Fiber optics (SMF) to support >100m interconnect and highest data rate with lower cost fiber

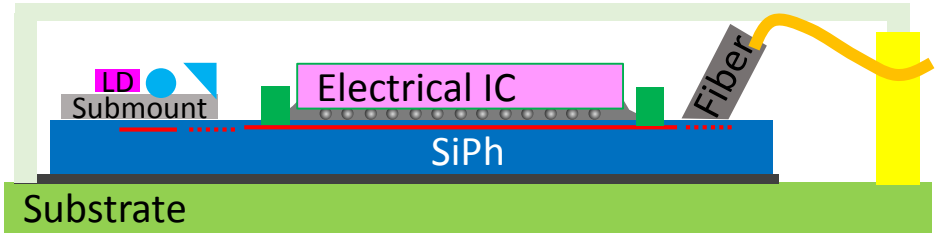
Typical SiPh Packaging Structure- Module level and System level

Module level- QSFP

QSFP SiPh module w/ edge coupling laser/fiber (>100G)

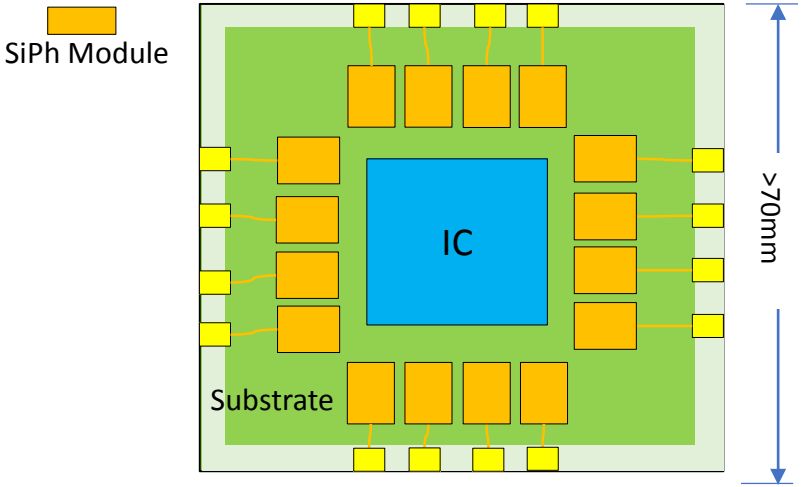


QSFP SiPh module w/ vertical coupling laser /fiber (>100G)



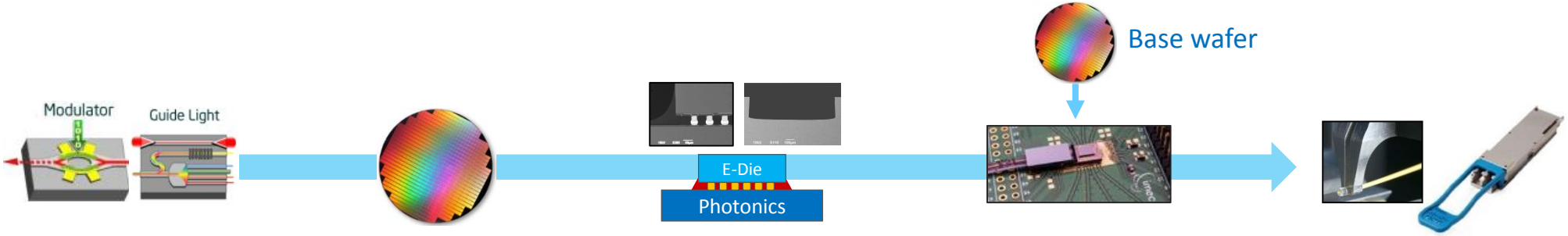
System level – Switch/ SiPh Modules

Integrated on Substrate (>400G)



Enter Strategy of SiPh

Foundry-OSATs ASIC model



Chip Design
SiPh / Electrical
Chip design

Foundry
SiPh / Electrical
IC Fabrication

OSAT/ CoW Platform

OSAT/ Optical Assy

OSAT/ Module Assy

Optical integration & Module level

Electrical integration & Wafer level

- Post-fab & Bumping
- Wafer sorting/ CoW test
- WL CoW assembly

ASE GROUP **Production x1 Q4'17**
Qual x1 Q4'18

- Laser diode attachment
- Packaging for Laser module
- WL optical test

ASE GROUP **In Development**

- Module assembly
- Functional testing

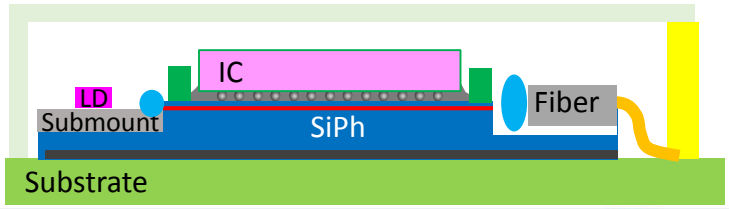
ASE GROUP **In Development**

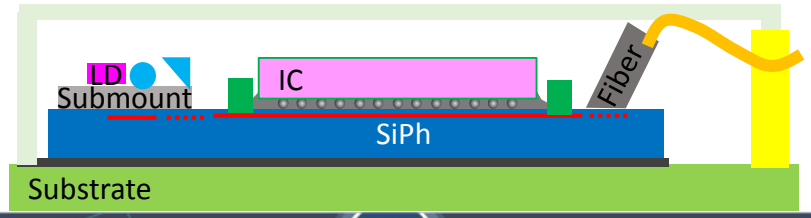
Phase-I Phase-II Phase-III

Tool Box planning of SiPh Packaging

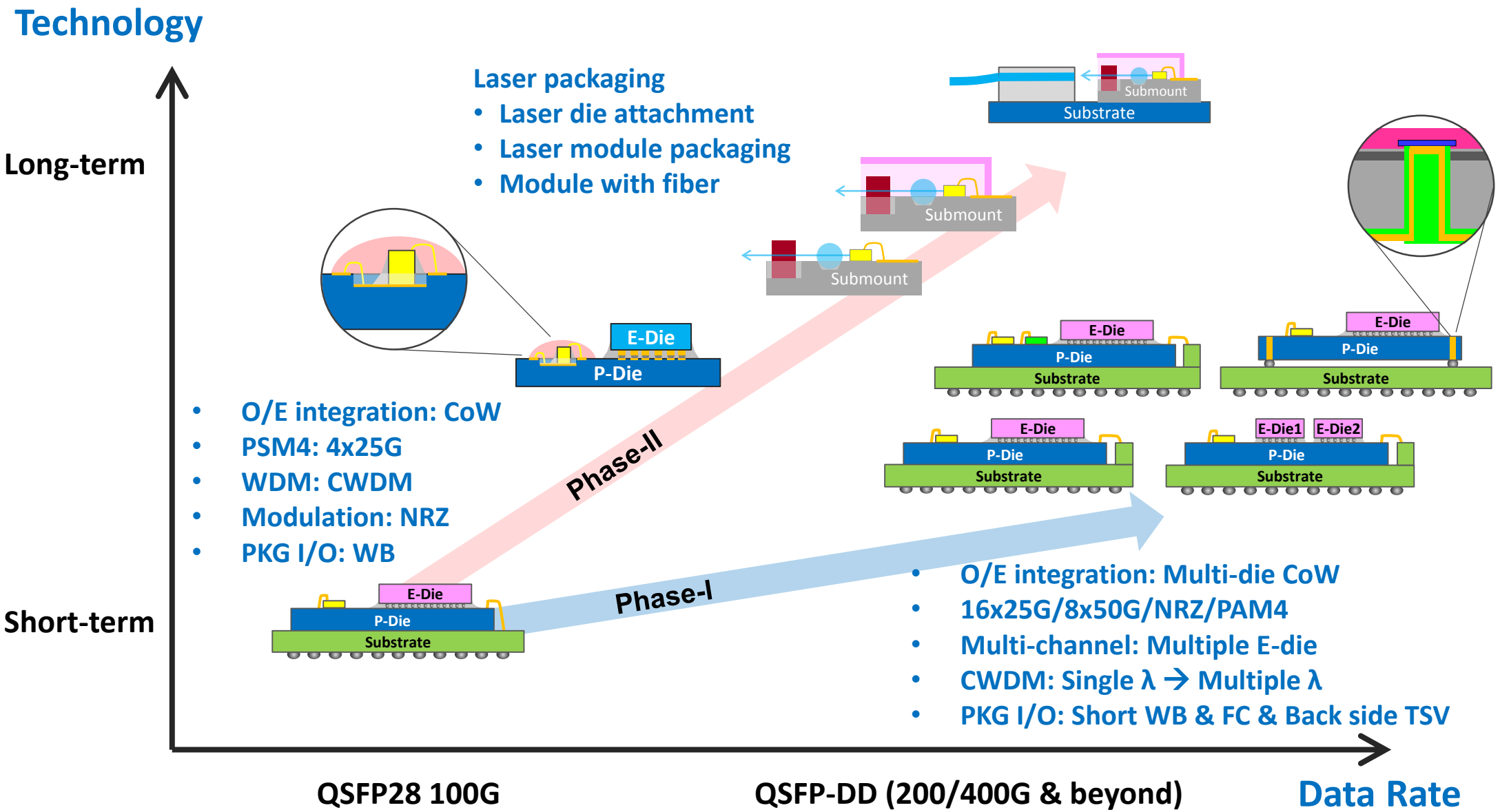
Ready | Developing | Evaluating

Key Elements	Silicon	SiPh, Driver /TIA, DSP, Switch
	Optical	LD, PD, Lens, Fiber array
	Final Packaging	Substrate, Metal housing
ASE Technology	Special wafer level process	DRIE trench/TSV, UBM + Bumping, PI DAM, CoC, PD DA/WB
	1st level ASSY.	CoCoS, LD Passive alignment, LD module active alignment, WL Optical testing
	2nd level ASSY.	Fiber active alignment - edge, Fiber active alignment - vertical
	Final ASSY.	Metal housing ASSY





SiPh Packaging Roadmap



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  - Sensors, GPU-Based AI, 5G and Cloud
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  - Tool Box of Passive integration for RF and PMIC
  - Tool Box of Si-Photonic Packaging
- **Concluding Remarks**

Concluding Remarks

- **Autonomous Driving System**
  - Drive IOE key technologies in place not only for economic, but Human Life
- **Key Technologies**
  - Sensors, AI, 5G and Optical I/O of DC
- **Extending the Packaging " Spectrum"**
  - Provide Electronic OSAT service and system integration
  - Extend to Wave Devices Packaging, from RF, MM-Wave and Light-Wave

Thank You

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