Three-Dimensional Packaging for Wide Bandgap Based Discrete and Multi-Chip Power Packages

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Outline

• Company Overview
• Motivation of 3D packaging techniques with wide bandgap power electronics
• Design and performance of X-5 multi-chip power module
• Design and performance of X-6 discrete package
• Summary
APEI, Inc. Core Technologies

- Multi-Chip Packaging
- Power Circuits & Systems
- High Reliability Modules
- SiC & GaN Device Expertise

High Density, High Performance Power Electronics

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Motivation for Wide Bandgap Power Electronics

Enabling Capability

- High Temperature Operation
- High Power Density
- Fast Switching; High Frequency

Key Benefits

- Reduce cooling requirements
- Reduce system volume/weight
- Reduce complexity
- Improve performance/reliability
- High current density
- High thermal conductivity substrate
- Reduce size of power filters/capacitors
- Reduce size/weight of power system
- Allows higher bandwidth for control loops reducing error in AC systems

3D Packaging Technologies

- High temperature multi-layer technologies reduce package size and increase reliability
- High current wire bondless interconnections
- Multi-layer packaging technologies reduce parasitics
Wide Bandgap Devices Enable Fast Switching Operation

• Both GaN and SiC allow High Frequency operation
  – Reduce switching losses
  – Smaller passives
  – Less expensive cooling systems

• Must Reduce Package Parasitics to take advantage of WBG characteristics
Design and Performance of the X-5 Power Module
Design of X-5 Power Module with Integrated Gate Driver

Specifications
• Full-bridge configuration
• 50+ A / 1200 V
• 225 °C maximum operation (T_{j\text{max}})
• 2 MOSFETs / 1 Schottky diode per switch position
• 58 mm × 41 mm × 13 mm (1/3 the volume of a deck of cards)

Package Components
• Metal-matrix composite baseplate
• AlN DBC Power substrate
• High temperature die and power substrate attach
• Integrated busboard → enables 3D Packaging
• Integrated gate driver
X-5 SiC MCPM Junction to Case Thermal Resistance

- Experiment $\Delta T_{j-c} = 17 \, ^\circ C$ and Model $\Delta T_{j-c} = 15 \, ^\circ C$
- The experimental and modeled $\Delta T_{j-c}$ are in good agreement
- A low junction-to-case thermal resistance of $0.18 \, ^\circ C/W$ was measured

Experiment

$\text{Total } P_{\text{dis}} = 95.5 \, W$

Spot 133 °C

Model

Spot 136 °C

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Low Parasitic Power Module for High Speed Switching

- 3D parasitic model using Comsol Multiphysics®
- One side of the full-bridge was analyzed due to the symmetric design
- Inductance/Resistance was modeled vs. frequency up to 1 MHz
- The X-5 exhibited low parasitics at high frequencies
- ~4 mΩ and ~16 nH at 500 kHz
- Inductance is roughly 1/2 of other commercial power brick style module [1]


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Ultra-Fast Switching From Low Parasitic X-5 / Gate Driver Integration

- Clamped inductive load
- 400 V / 30 A switching waveforms
- Rise time = 16.1 ns
- Fall time = 7.5 ns
- Switching Frequency = 1.2 MHz
- Minimal ringing and overshoot

Boost Converter Efficiency vs. Power
SiC Charger for Next Generation Toyota Prius Plug-in Hybrid

CHARGER SYSTEM DESIGN TARGETS

<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>Power Level</td>
<td>2.9 kW</td>
<td>3.3 kW</td>
<td>6.1 kW (Peak)</td>
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<tr>
<td>Volume</td>
<td>6.4 L</td>
<td>3.5 L</td>
<td>1.2 L</td>
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<tr>
<td>Mass</td>
<td>6.6 kg</td>
<td>3.5 kg</td>
<td>1.6 kg</td>
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<tr>
<td>Volumetric power density</td>
<td>0.45 kW/L</td>
<td>0.943 kW/L</td>
<td>5.0 kW/L</td>
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<tr>
<td>Gravimetric power density</td>
<td>0.42 kW/kg</td>
<td>0.943 kW/kg</td>
<td>3.8 kW/kg</td>
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<tr>
<td>Efficiency</td>
<td>–</td>
<td>94%</td>
<td>&gt;95%</td>
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</table>

> 10× Power Density

Design and Performance of the X-6 Power Package
Specifications

• Single die and co-pack
• 100+ A / 1200 V
• 225 °C maximum operation ($T_{j\text{max}}$)
• 30 mm × 21 mm × 7 mm

Package Features

• Compatible with SiC and GaN
• Electrically Isolated AlN DBC power substrate
• High temperature die and power substrate attach
• High current capable
• Low inductance (< 8 nH)
• Ultra-fast switching (< 4 ns)
• Low $R_{jc}$
  – 2 mm × 2 mm Die → 1.23 °C/W
  – 5 mm × 5 mm Die → 0.5 °C/W
• Modular for system integration
• Wire bonded or bondless versions

SiC MOSFET X-6 Package

On-State (@ 225°C)
Wirebondless X-6 Assembly

Housing
High temperature plastic
Injection molded

Fasteners
Low profile
“Captive” in plastic

Interconnects
*For wire bondless configurations
PCB, DBC, Thick Film

Contacts
Panelized & Etched

Substrate
DBC, DBA, AMB, etc.

Base Plate
Copper or MMC

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X-6 Configurations

- **PARALLEL**
- **HALF BRIDGE**
- **FULL BRIDGE**
X-6 Package Junction to Case Thermal Resistance

• Experimental $R_{j-c} = 1.23 \, ^\circ\text{C/W}$
• Modeled $R_{j-c} = 1.15 \, ^\circ\text{C/W}$
• The experimental and modeled $R_{j-c}$ are in good agreement
• ~50 % of the thermal resistance of the package is in the AlN layer of the DBC
• $R_{j-c}$ can be reduced further using DBC with a thinner AlN layer

Experiment

Model

P_{dis} = 48 \, \text{W}

Spot = 66 \, ^\circ\text{C}

P_{dis} = 48 \, \text{W}
X-6 Parasitic Modeling

X-6 Package
- Gate & Power LOOPS
- 5 & 10 mil WIRE BOND
- Dual Substrate FLIP CHIP

TO-254 Package
- Gate & Power LOOPS
- 5 & 10 mil WIRE BOND
- Shortened PIN LENGTH

Wire Bonded SiC TMOS
Wire Bondless GaN HEMT
TO-254 - SiC TMOS
Discrete Package Resistance Comparison

Power Loop

Gate Loop

Resistance (mΩ)

0 2 4 6 8 10 12 14 16 18 20

Power Loop

Gate Loop

GaN HEMT SiC TMOS TO-254

0.54 0.28 1.31 13.30 15.16 14.30

Current Density

A/mm²

0 >4

A/mm²

0 >4

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Discrete Package Inductance Comparison

<table>
<thead>
<tr>
<th></th>
<th>Power Loop</th>
<th>Gate Loop</th>
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<tr>
<td><strong>GaN HEMT</strong></td>
<td>7.50</td>
<td>8.54</td>
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<tr>
<td><strong>SiC TMOS</strong></td>
<td>7.83</td>
<td>6.74</td>
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<tr>
<td><strong>TO-254</strong></td>
<td>12.98</td>
<td>21.32</td>
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Wire Bondless GaN HEMT

Wire Bonded SiC TMOS

TO-254 - SiC TMOS
High Efficiency GaN HEMT Boost Converter

- 200 - 300 V Input / 400 V Output
- Switching Frequency = 100 kHz
- Turn on ~ 8.2 ns, Turn off ~ 3.7 ns
- Minimal Ringing
- Up to 5 kW
- > 99 % Peak Efficiency @ 100 kHz
- 97.5 % @ 1 MHz

Boost Converter Efficiency

- 200V Input, 100kHz
- 300V Input, 100kHz
- 300V Input, 1MHz

Boost Converter Turn-Off Event

Gate Voltage

Drain Voltage

3.72ns transition
20ns / Division

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Summary

• Wide bandgap power packages using 3D packaging technologies were presented
• The electrical and thermal characteristics of the X-5 and X-6 were introduced
• The SiC-based X-5 demonstrated > 95% efficiency and a 5 kW/L volumetric power density in next generation Toyota Prius charger
• The GaN-based X-6 exhibited ultra-fast switching (< 4 ns) and a high efficiency (> 99 %) in a boost configuration
Wide Bandgap HT-3000 Power Module

- Half-bridge +300 A / 1200 V
- Standard power module footprint
- Device neutral
- 225 °C maximum operation (T_{jmax})
- Minimized parasitics (< 7 nH)
- Low thermal resistance (< 0.1 °C/W)
- Low volume/weight (72 cm³ and 140 g)