Three-Dimensional Packaging for Wide Bandgap Based Discrete and Multi-Chip Power Packages

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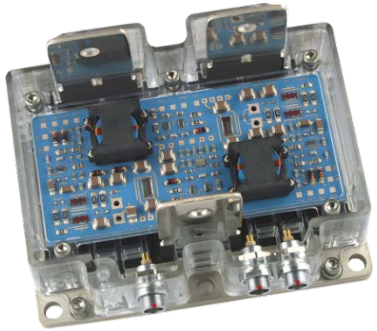
Outline

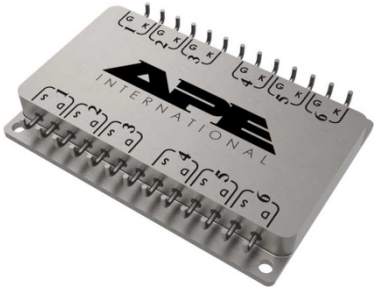
- Company Overview
- Motivation of 3D packaging techniques with wide bandgap power electronics
- Design and performance of X-5 multi-chip power module
- Design and performance of X-6 discrete package
- Summary

APEI, Inc. Core Technologies

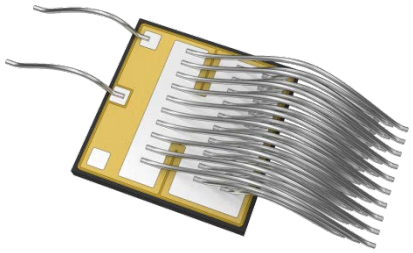


Multi-Chip Packaging

Power Circuits & Systems

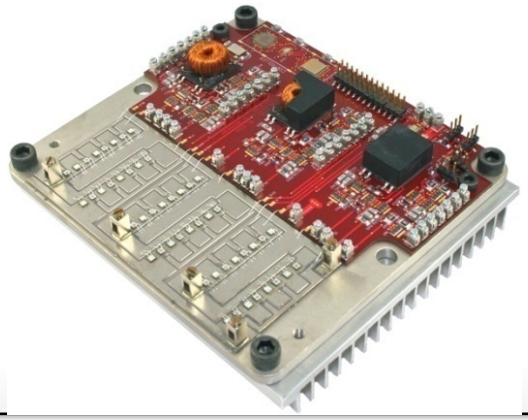


High Reliability Modules



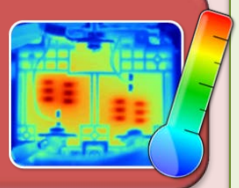
SiC & GaN Device Expertise

High Density,
High Performance
Power Electronics



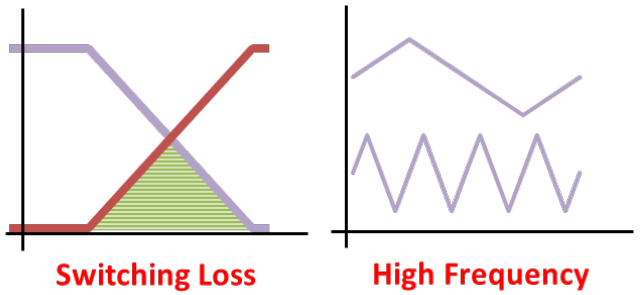
Motivation for Wide Bandgap Power Electronics

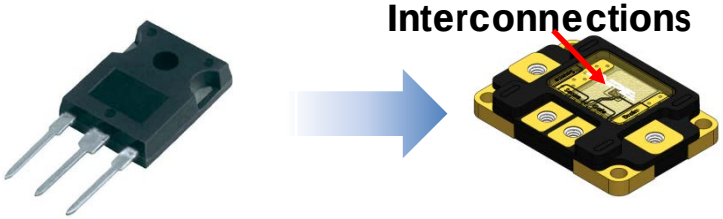
Enabling Capability	Key Benefits	3D Packaging Technologies
High Temperature Operation	• Reduce cooling requirements • Reduce system volume/weight • Reduce complexity • Improve performance /reliability	High temperature multi-layer technologies reduce package size and increase reliability
High Power Density	• High current density • High thermal conductivity substrate	High current wire bondless interconnections
Fast Switching; High Frequency	• Reduce size of power filters/capacitors • Reduce size/weight of power system • Allows higher bandwidth for control loops reducing error in AC systems	Multi-layer packaging technologies reduce parasitics

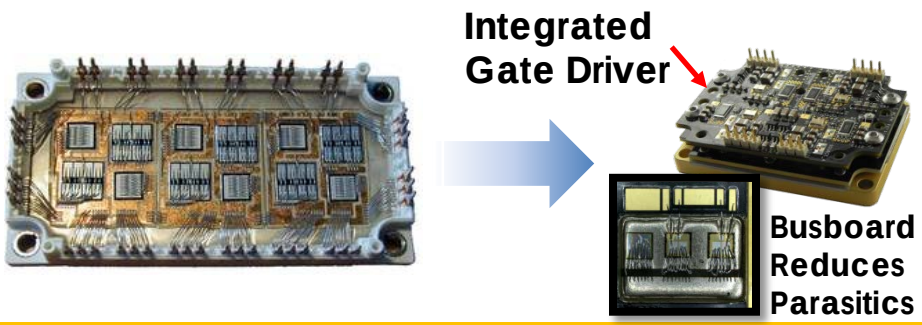


Wide Bandgap Devices Enable Fast Switching Operation

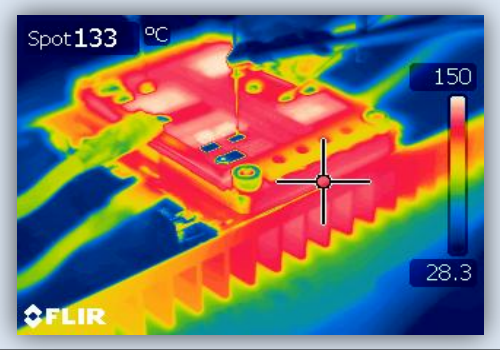
- Both GaN and SiC allow High Frequency operation
  - Reduce switching losses
  - Smaller passives
  - Less expensive cooling systems
- Must Reduce Package Parasitics to take advantage of WBG characteristics







Design and Performance of the X-5 Power Module



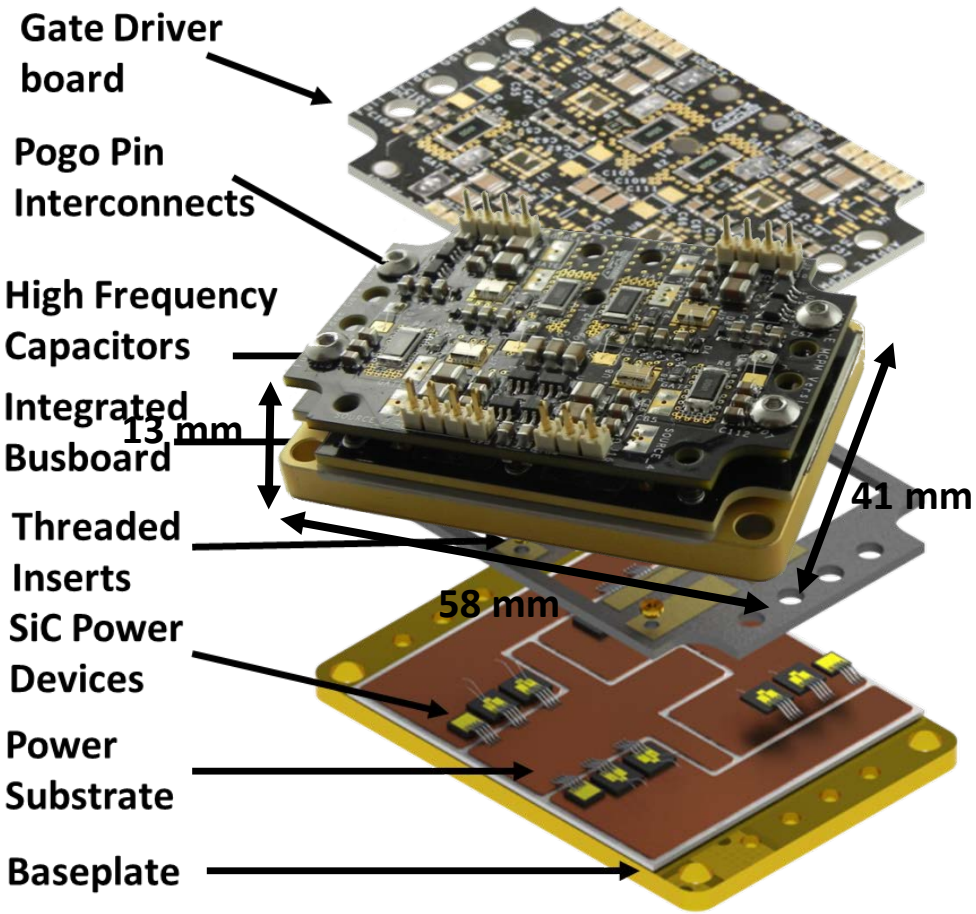
Design of X-5 Power Module with Integrated Gate Driver

Specifications

- Full-bridge configuration
- 50+ A / 1200 V
- 225 °C maximum operation (T_{jmax})
- 2 MOSFETs / 1 Schottky diode per switch position
- 58 mm × 41 mm × 13 mm (1/3 the volume of a deck of cards)

Package Components

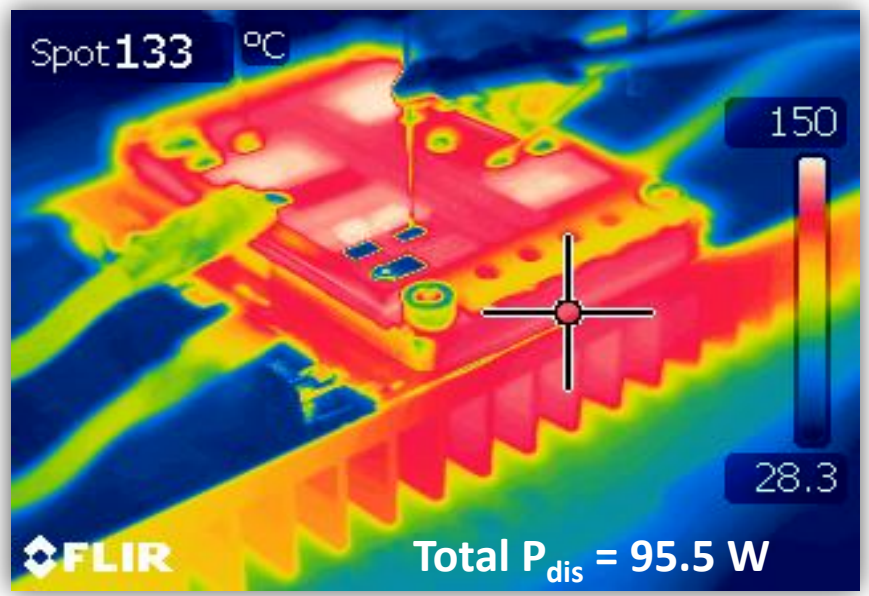
- Metal-matrix composite baseplate
- AlN DBC Power substrate
- High temperature die and power substrate attach
- Integrated busboard → enables 3D Packaging
- Integrated gate driver



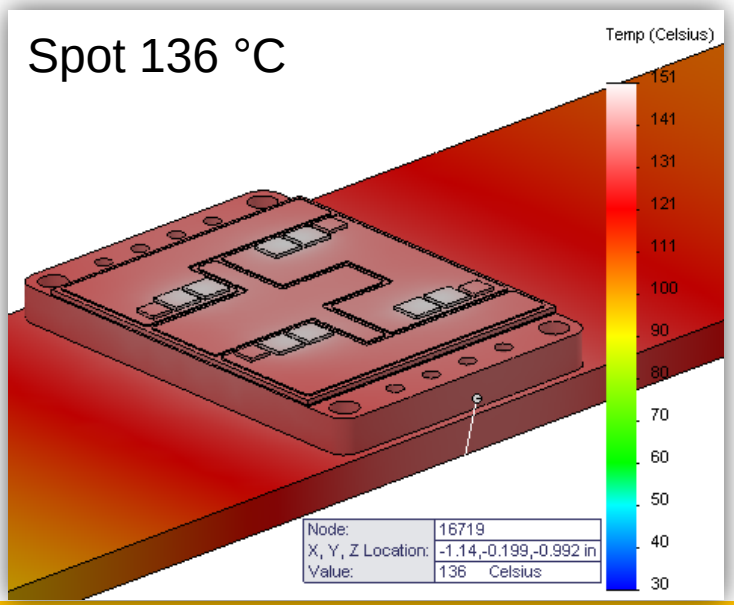
X-5 SiC MCPM Junction to Case Thermal Resistance

- Experiment $\Delta T_{j\text{-}c}$ = 17 °C and Model $\Delta T_{j\text{-}c}$ = 15 °C
- The experimental and modeled $\Delta T_{j\text{-}c}$ are in good agreement
- A low junction-to-case thermal resistance of **0.18 °C/W was measured**

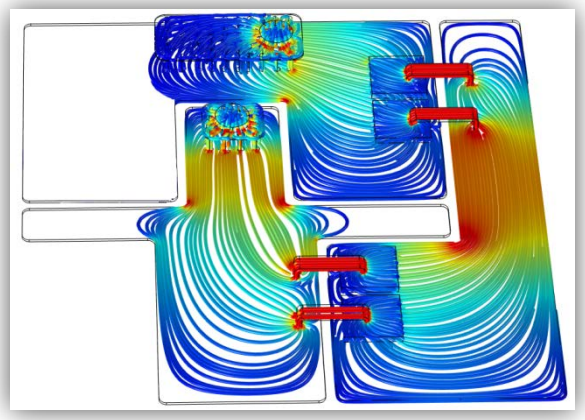
Experiment

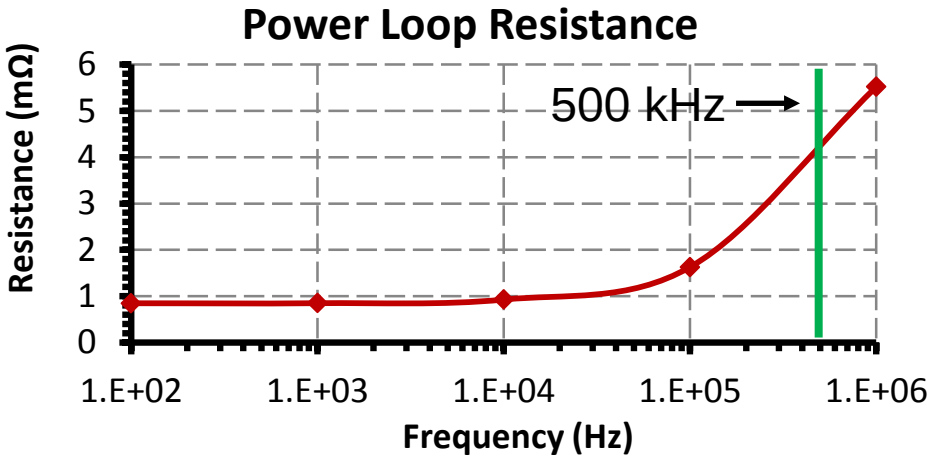


Model

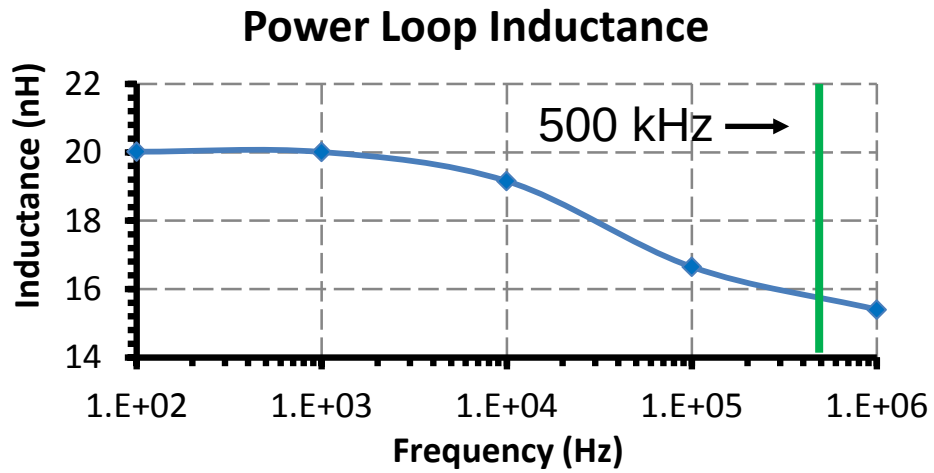


Low Parasitic Power Module for High Speed Switching



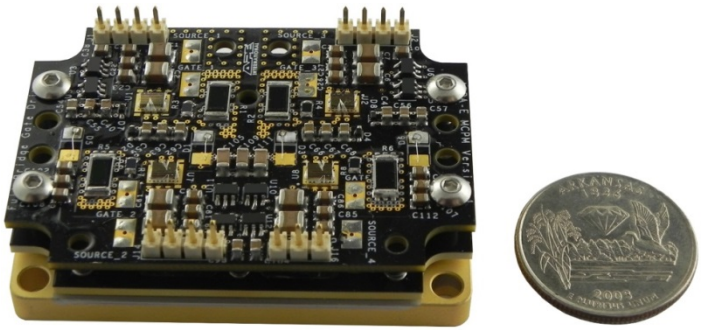


- 3D parasitic model using Comsol Multiphysics®
- One side of the full-bridge was analyzed due to the symmetric design
- Inductance/Resistance was modeled vs. frequency up to 1 MHz
- The X-5 exhibited low parasitics at high frequencies
- ~4 mΩ and ~16 nH at 500 kHz
- Inductance is roughly 1/2 of other commercial power brick style module [1]



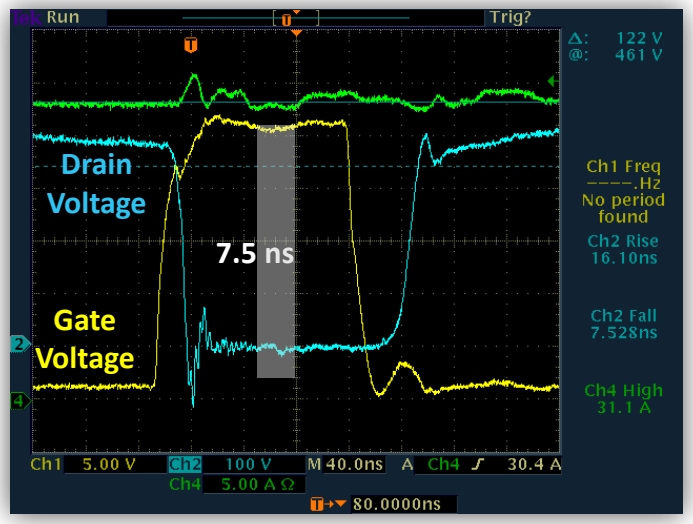
[1] http://www.semikron.com/products/data/cur/assets/SKM100GB12T4_22892020.pdf

Ultra-Fast Switching From Low Parasitic X-5 / Gate Driver Integration

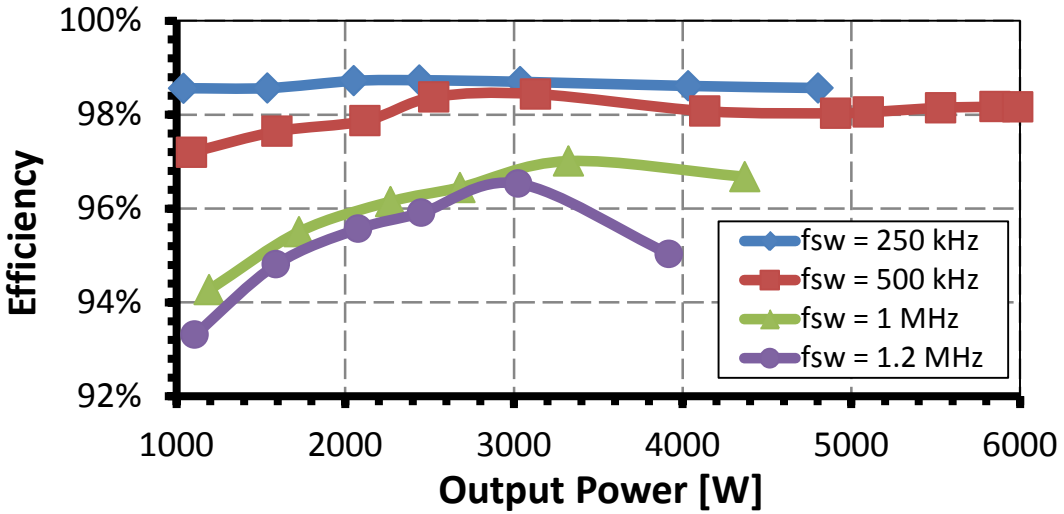


- Clamped inductive load
- 400 V / 30 A switching waveforms
- Rise time = 16.1 ns
- Fall time = 7.5 ns
- Switching Frequency = 1.2 MHz
- Minimal ringing and overshoot

Turn On Waveform

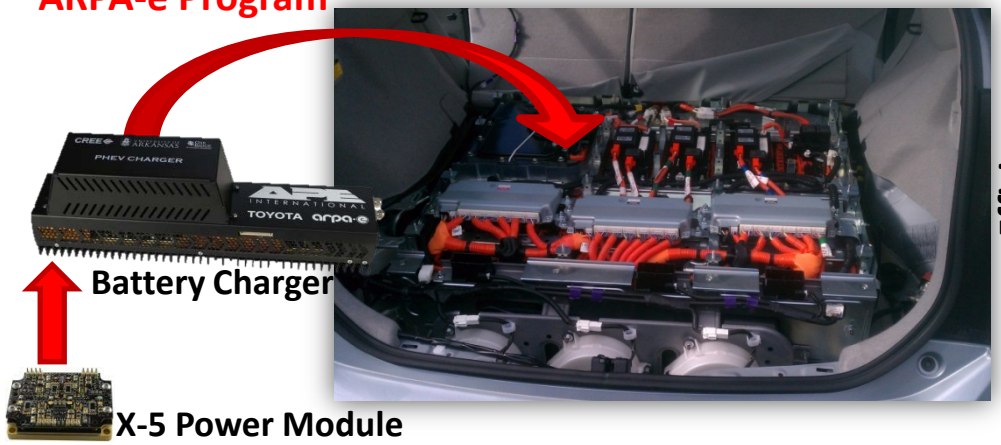


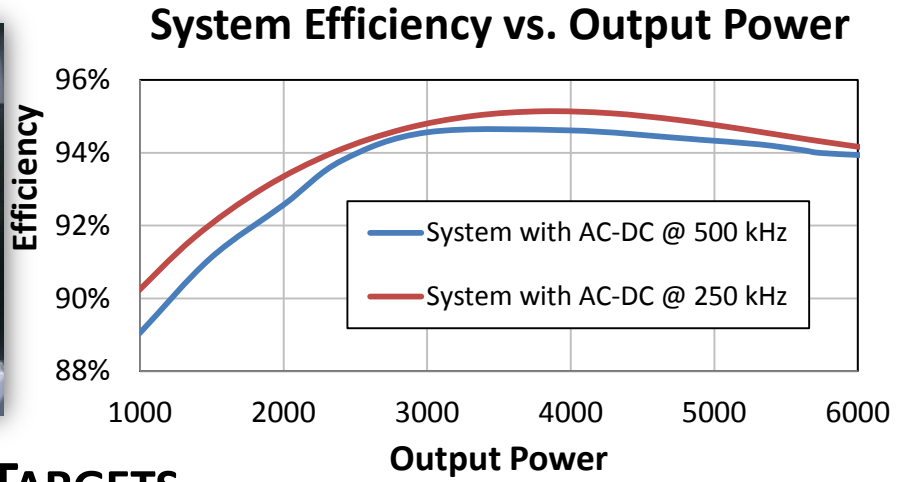
Boost Converter Efficiency vs. Power



SiC Charger for Next Generation Toyota Prius Plug-in Hybrid

Funded by DOE ARPA-e Program





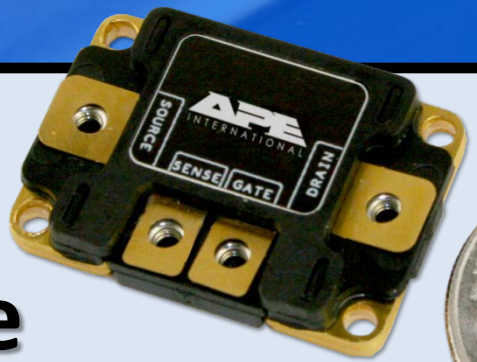
Charger System Design Targets

Specifications	2010 Toyota Prius PHEV Charger [2]	Preliminary DOE PHEV On-Board Charger Targets for 2022 [3]	APEI, Inc. Prototype SiC PHEV Charger
Power Level	2.9 kW	3.3 kW	6.1 kW (Peak)
Volume	6.4 L	3.5 L	1.2 L
Mass	6.6 kg	3.5 kg	1.6 kg
Volumetric power density	0.45 kW/L	0.943 kW/L	5.0 kW/L
Gravimetric power density	0.42 kW/kg	0.943 kW/kg	3.8 kW/kg
Efficiency	–	94%	>95%

> 10× Power Density

[2] Toyota, "Plug-in hybrid 2010 model revised (includes 2012 model) emergency response guide," 22 Feb. 2012.
[3] Department of Energy, "EV everywhere: a grand challenge in plug-in electric vehicles, " 2012.

Design and Performance of the X-6 Power Package



Design of X-6 Power Package

Specifications

- Single die and co-pack
- 100+ A / 1200 V
- 225 °C maximum operation (T_{jmax})
- 30 mm × 21 mm × 7 mm

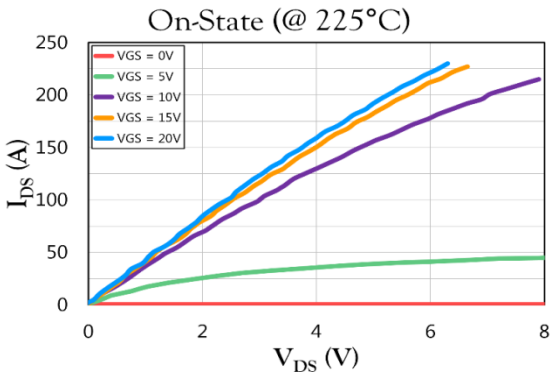
Package Features

- Compatible with SiC and GaN
- Electrically Isolated AlN DBC power substrate
- High temperature die and power substrate attach
- High current capable
- Low inductance (< 8 nH)
- Ultra-fast switching (< 4 ns)
- Low R_{jc}
  - 2 mm × 2 mm Die → 1.23 °C/W
  - 5 mm × 5 mm Die → 0.5 °C/W
- Modular for system integration
- Wire bonded or bondless versions

Wire Bondless Package

Wire Bonded Package

SiC MOSFET X-6 Package



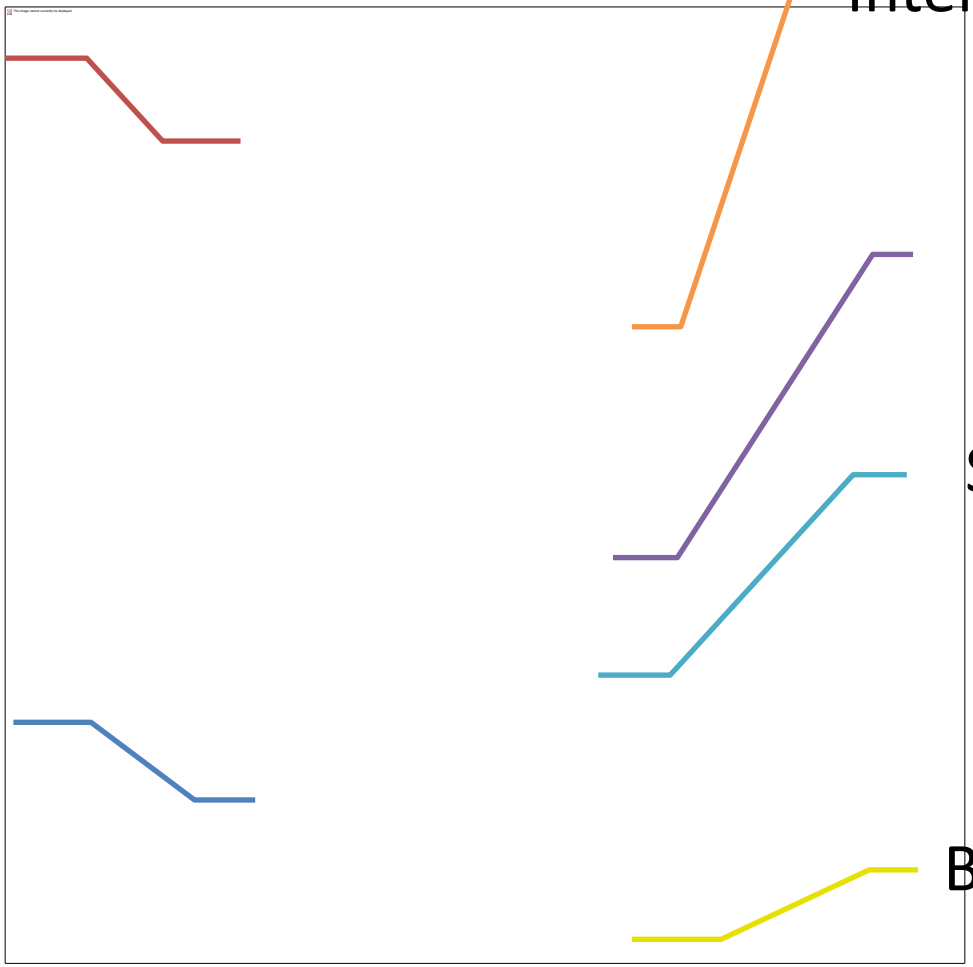
Wirebondless X-6 Assembly

Housing

High temperature plastic)
Injection molded

Fasteners

Low profile
"Captive" in plastic



Interconnects

*For wire bondless configurations
PCB, DBC, Thick Film

Contacts

Panelized & Etched

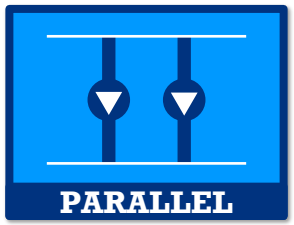
Substrate

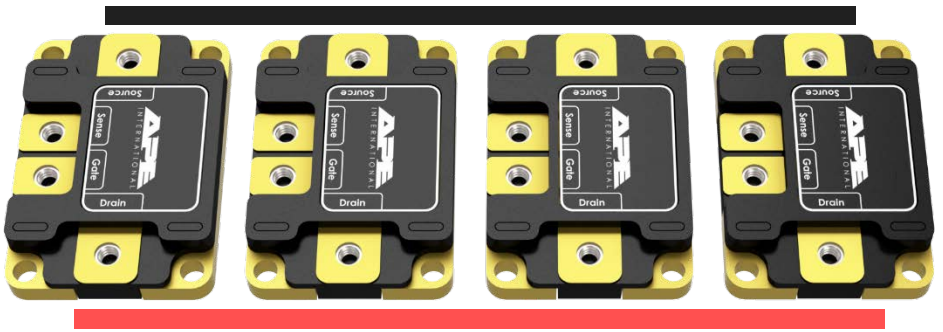
DBC, DBA, AMB, etc.

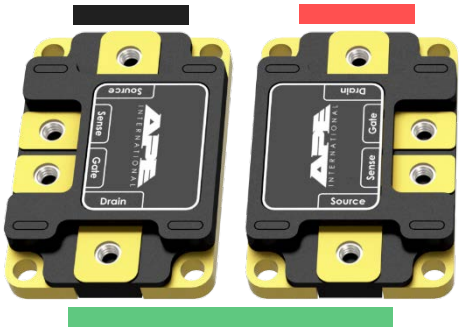
Base Plate

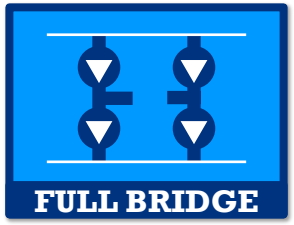
Copper or MMC

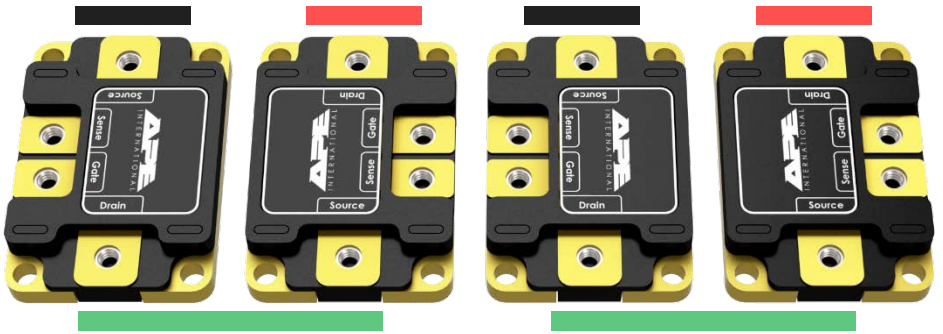
X-6 Configurations







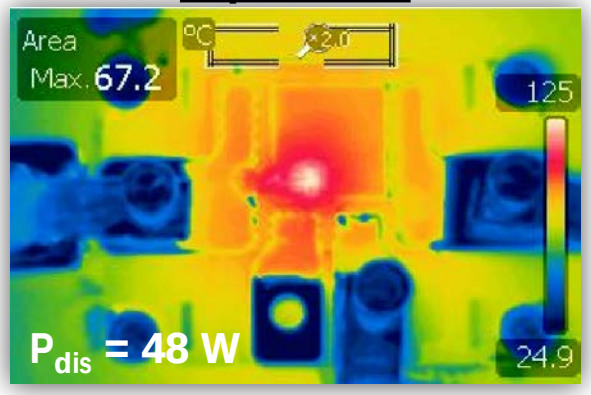




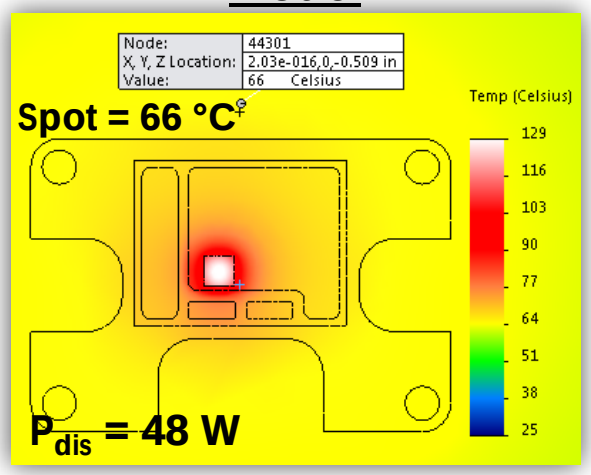
X-6 Package Junction to Case Thermal Resistance

- Experimental $R_{j\text{-}c}$ = 1.23 °C/W
- Modeled $R_{j\text{-}c}$ = 1.15 °C/W
- The experimental and modeled $R_{j\text{-}c}$ are in good agreement
- ~ 50 % of the thermal resistance of the package is in the AlN layer of the DBC
- $R_{j\text{-}c}$ can be reduced further using DBC with a thinner AlN layer

Experiment



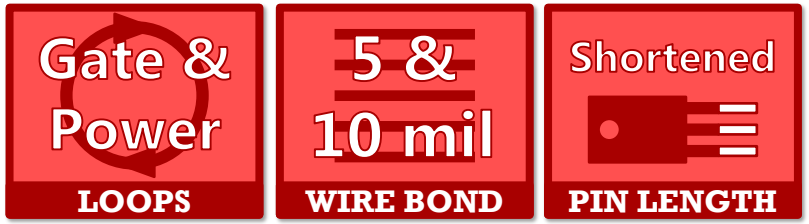
Model



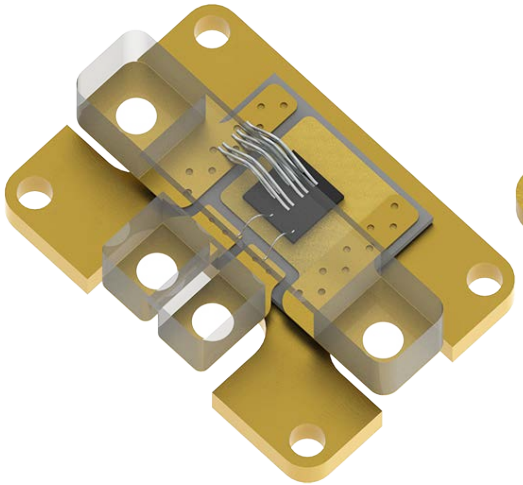
X-6 Parasitic Modeling

X-6 Package

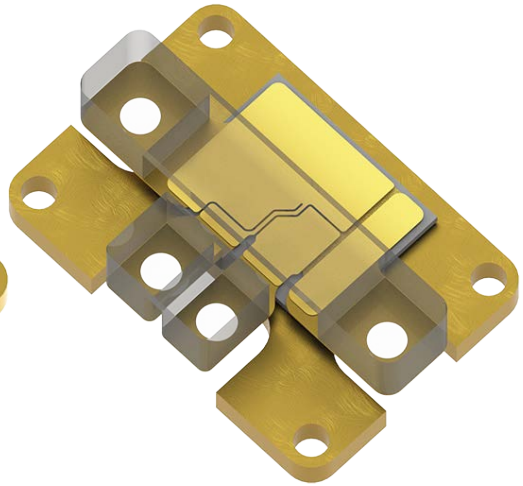
TO-254 Package



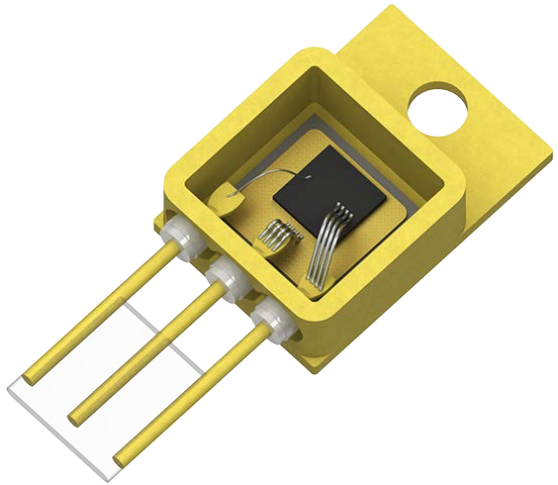
Wire Bonded SiC TMOS



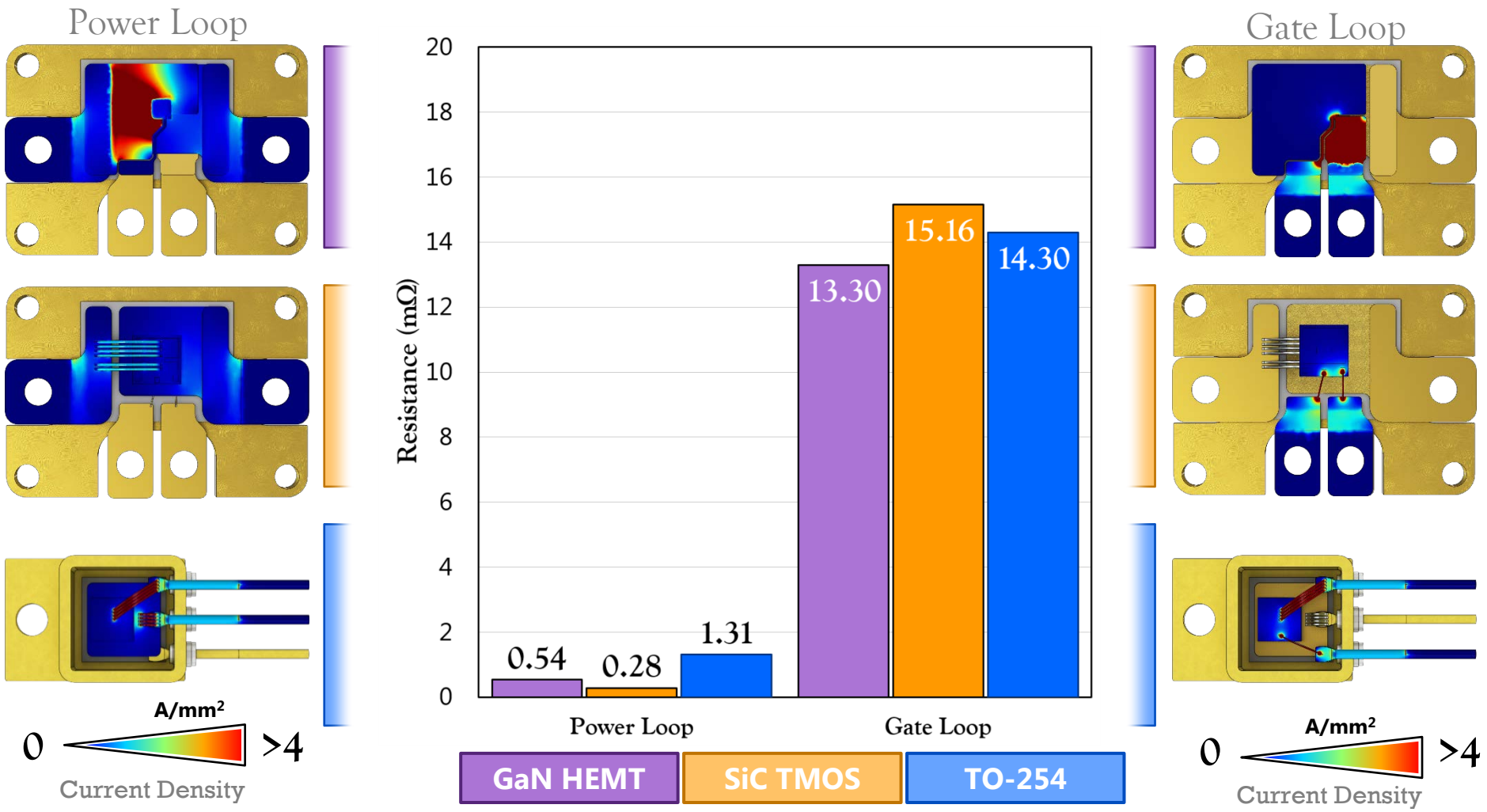
Wire Bondless GaN HEMT



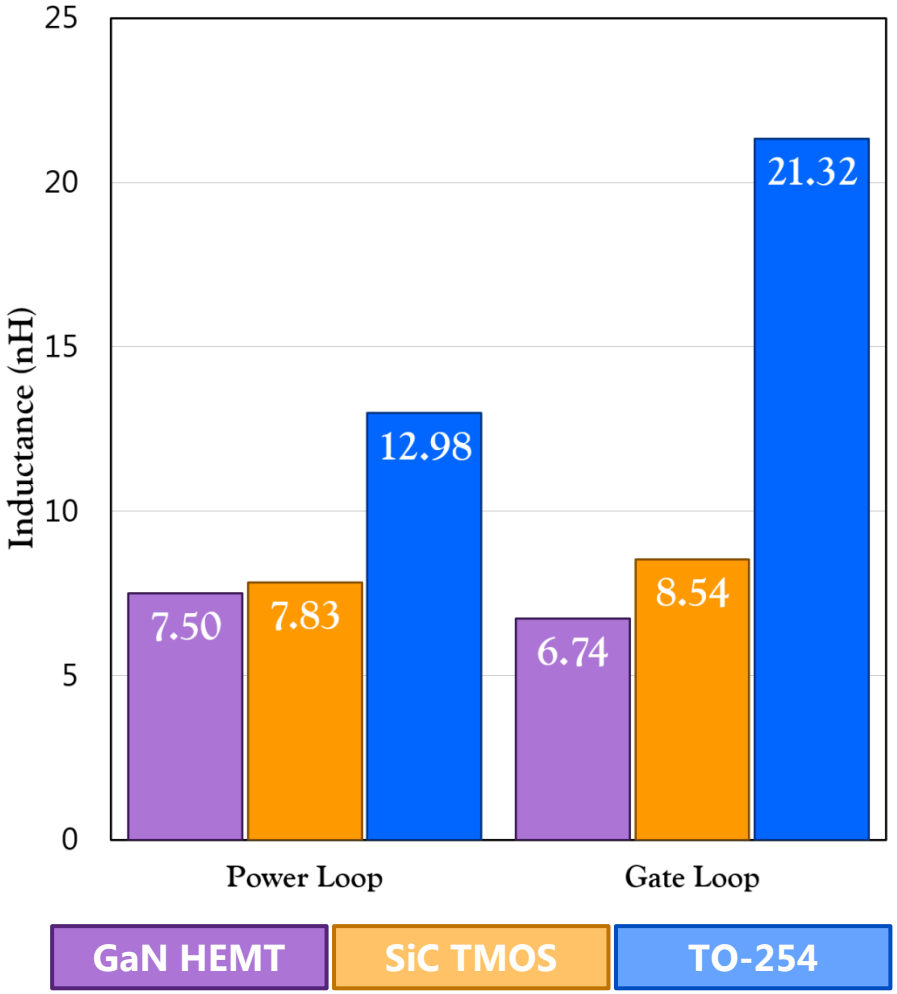
TO-254 – SiC TMOS

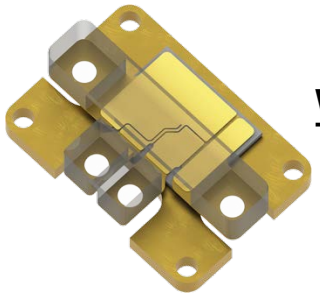


Discrete Package Resistance Comparison

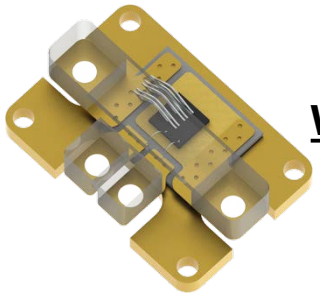


Discrete Package Inductance Comparison

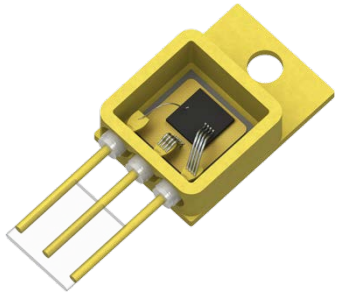




Wire Bondless GaN HEMT



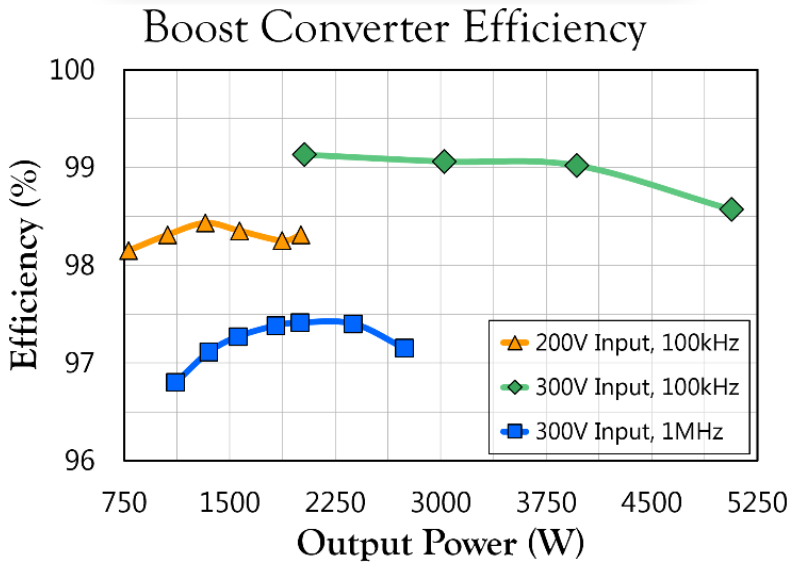
Wire Bonded SiC TMOS

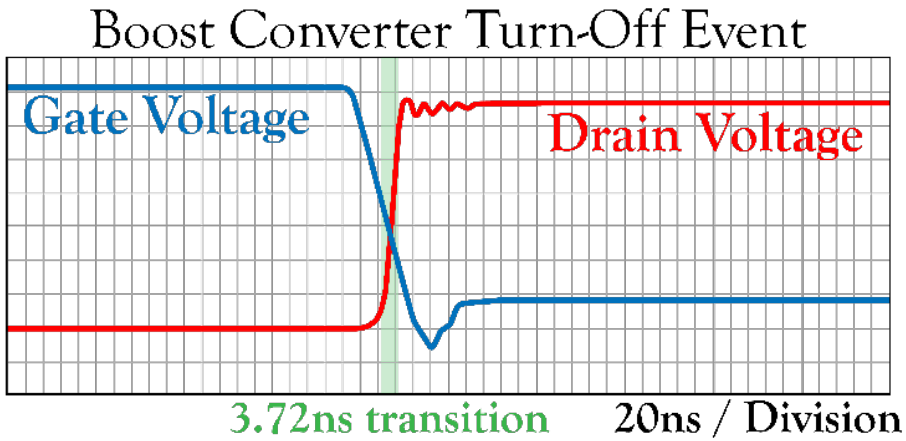


TO-254 – SiC TMOS

High Efficiency GaN HEMT Boost Convertor

- 200 - 300 V Input / 400 V Output
- Switching Frequency = 100 kHz
- Turn on ~ 8.2 ns, Turn off ~ 3.7 ns
- Minimal Ringing
- Up to 5 kW
- > 99 % Peak Efficiency @ 100 kHz
- 97.5 % @ 1 MHz

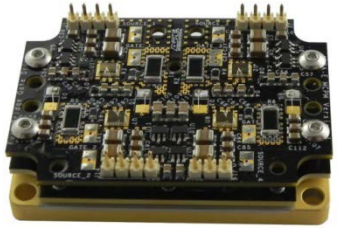




Summary

- Wide bandgap power packages using 3D packaging technologies were presented
- The electrical and thermal characteristics of the X-5 and X-6 were introduced
- The SiC-based X-5 demonstrated > 95% efficiency and a 5 kW/L volumetric power density in next generation Toyota Prius charger
- The GaN-based X-6 exhibited ultra-fast switching (< 4 ns) and a high efficiency (> 99 %) in a boost configuration

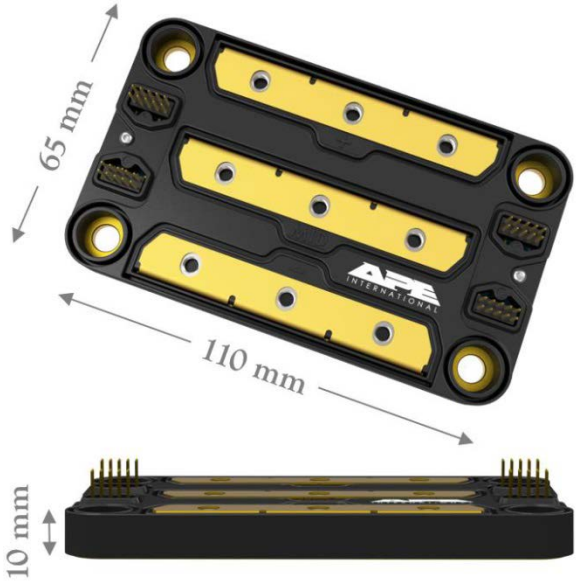
APEI's X-5 Power Module



APEI's X-6 Power Package

Connect With Us!

Wide Bandgap HT-3000 Power Module



- Half-bridge +300 A / 1200 V
- Standard power module footprint
- Device neutral
- 225 °C maximum operation (T_{jmax})
- Minimized parasitics (< 7 nH)
- Low thermal resistance (< 0.1 °C/W)
- Low volume/weight (72 cm^3 and 140 g)