Printed Interfacial Interconnects in High Power Modules

Douglas C Hopkins, Yang Xu, Haotao KE
Laboratory for
Packaging Research in Electronic Energy Systems
NSF FREEDM Systems Ctr / Advanced Transportation Energy Ctr
North Carolina State University
1791 Varsity Drive, Suite 100; Raleigh, NC 27606-7571
Tele: 919-513-5929, Fax: 919-513-0405
DCHopkins@NCSU.Edu

UnPaid Advertisement – PREES Update

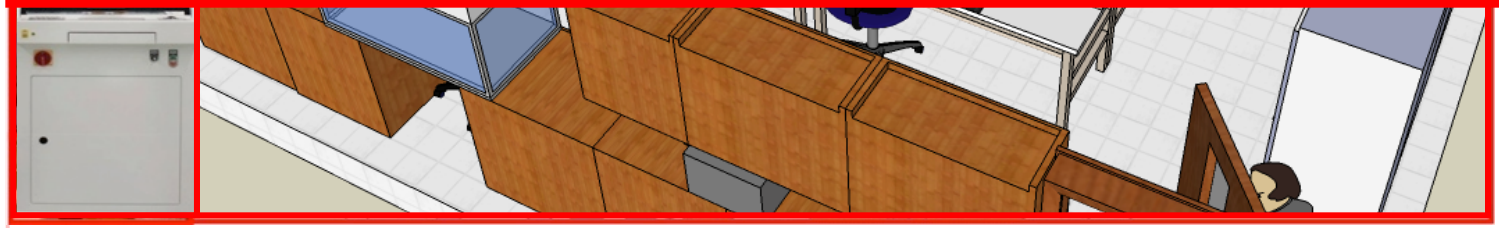
PREES Laboratory

NC STATE UNIVERSITY

Packaging Research in Electronic Energy Systems

800 sq. ft. EB-2, Rm.B-005

Also 800 sq. ft. in MRC 331.



DCHopkins@NCSU.edu

www.FREEDM.NCSU.edu/PREES

FREEDM systemscenter

Is "Additive Manufacturing" aka"3D Printing" a Solution looking for a Problem

AM builds on the premise of layering

- We already do a very good job keeping our Power Electronic structures planar, e.g. we have "multilayered" PCB, DBC and LTCC

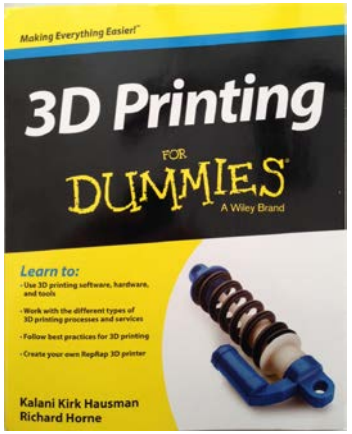
So why AM? Four factors that will impact how AM affects PE:

- Many new materials, particularly nano-materials and tailored composites
- New geometric structures
  - Move to more cubic aspect ratios ("growing upward")
  - Curved structures that can't be cast, stamped or machined
    - Net shaping and geometric integration into a final application
  - Complex internal structures (with integrated composites)

- Flexible and reduced parts, just-in-time, and replace/repair inventory
- Rapid Prototyping

IS 3-D PRINTING THAT MAIN STREAM?

ON THE COVER… A SHOCK ABSORBER, NOT A TOY.



RELEASED JAN 2014

Next Book: *Ditch the Vineyard – Expand Your Garage*
A 3D Approach to Retirement

For a more serious introduction:

"Additive Manufacturing Technologies - Rapid Prototyping to Direct Digital Manufacturing," I. Gibson, D W Rosen, B Stucker, Springer books, ISBN: 978-1-4419-1119-3, 2010

"A review on 3D micro-additive manufacturing technologies," M. Vaezi, H. Seitz, S. Yang, *Int J Adv Manuf Technol* (2013) 67:1721-1754, 25 Nov 2012.

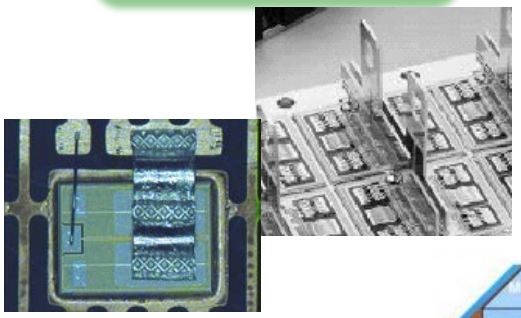
Interfacial Interconnects of Interest

ENERGY TRANSFER OF ALL THESES ENERGIES THROUGH THE INTERFACE

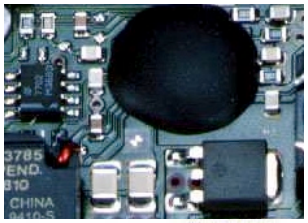
Electrical | Thermal | Mechanical*

…FOR EACH OF THE PACKAGING LEVELS

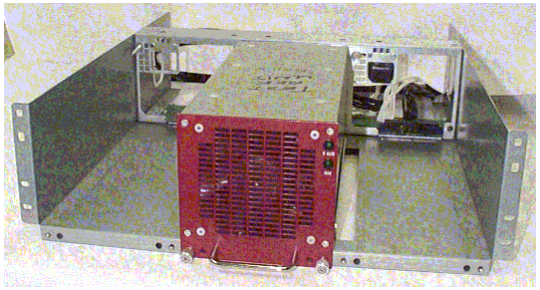
1st Level
Chip in Package
(Chip Lvl Pkg'g)

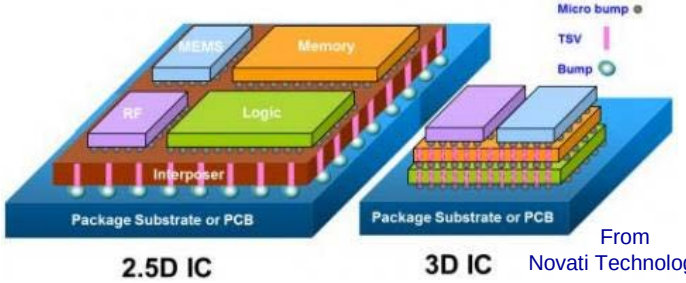


2nd Level
Package on Board
(Board Lvl Pkg'g



3rd Level
Board in Rack
(Box Lvl Pkg'g)





2.5D IC 3D IC

From Novati Technologies

* Includes hydraulics

FREEDM systemscenter

State-Of-Art in PE-AM

Very little work in this area

- Search "power electronics" & "interposer"; returns 160 results

Categories

- Silicon interposer
  - Through Silicon Via (TSV)
- Organic
  - Flex material like resin
- Thermal interface material

Silicon Interposer w/ Fluid Cooling

An integration process for silicon carrier with embedded thermal solution has been developed. The silicon carriers, having both electrical and fluidic interconnections, can act as substrates for chips mounting and then can be stacked over each other with a silicon interposer in between to form a cooling module for high power heat dissipation in 3-D packages.

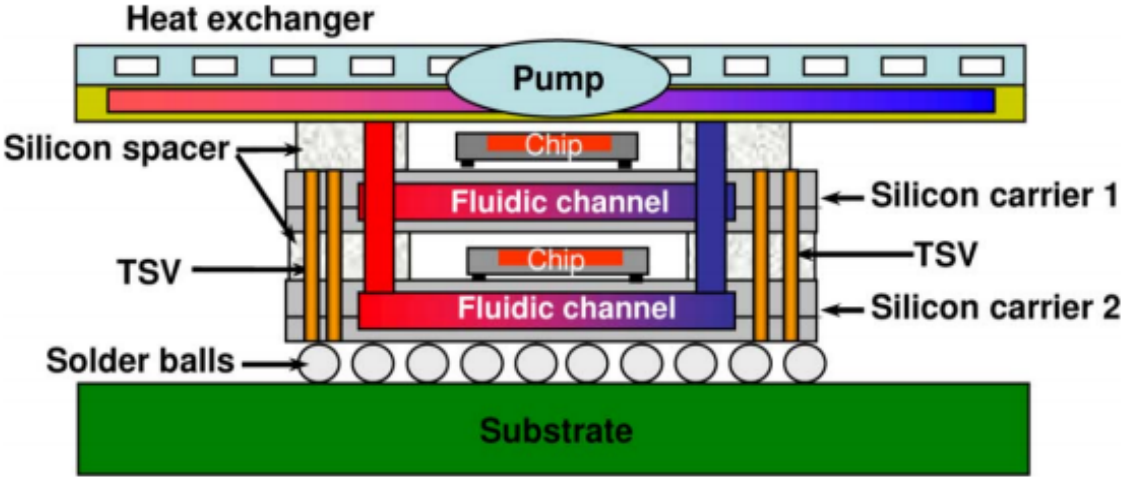


Fig. 1. Illustration of 3-D stacking of silicon carriers for high-power chips integration.

"Fabrication of Silicon Carriers With TSV Electrical Interconnections and Embedded Thermal Solutions for High Power 3-D Packages," Aibin Yu, Navas Khan, et.al., IEEE Trans on Components And Packaging Technologies, Vol. 32, No. 3, Sept 2009

In High band-width signaling

Silicon dice featuring novel I/O interconnections and embedded micro pin-fin heat sink were fabricated and flip-chip bonded to a Si interposer.

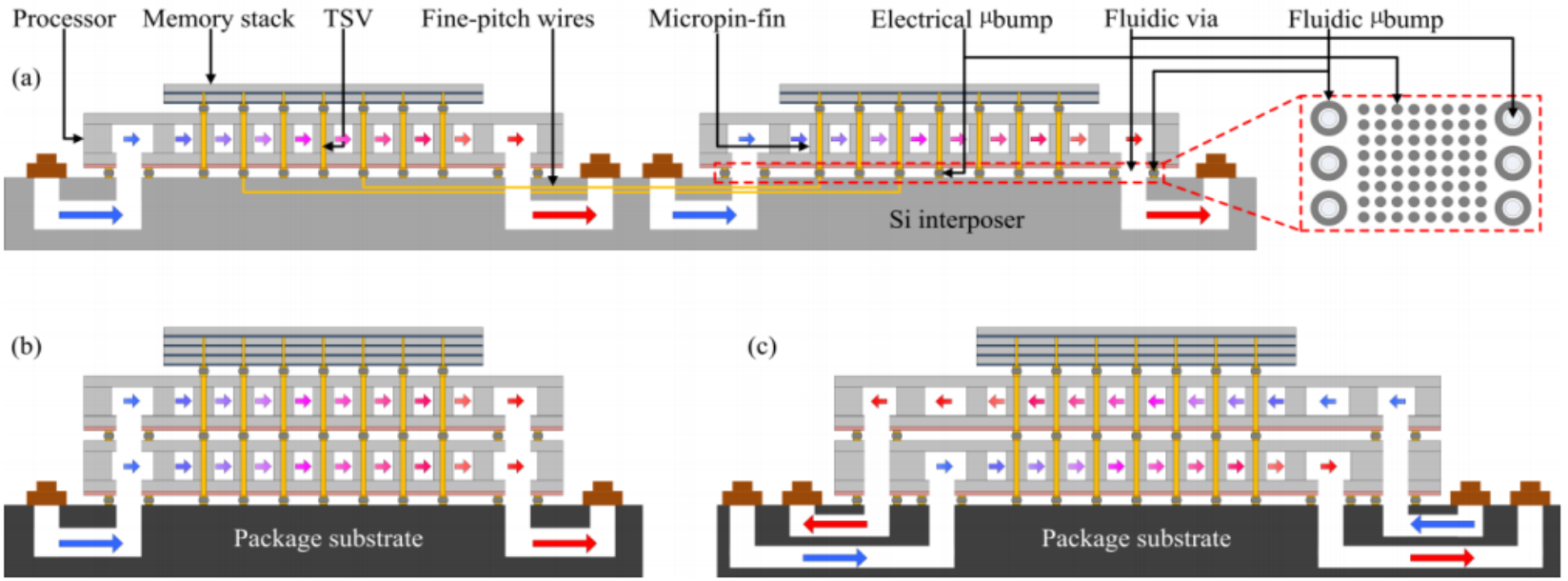


Fig. Fluidic and electrical microbumps enabling embedded microfluidic cooling and high-bandwidth signaling for a) 2.5D interposer system of two processors and two memory stacks; b) 3D IC stack of two processors and multiple memory dice; c) 3D system with independent microfluidic cooling for each processor

Design, fabrication and assembly of a novel electrical and microfluidic I/Os for 3-D chip stack and silicon interposer, Li Zheng, Yue Zhang and Muhannad S. Bakir, Electronic Components & Technology Conference, pp 2243-48, 2013

Three-Die Stack

Three dies are stacked between the heat sink and package substrate. Signals and power are routed from PCB to the package substrate through ceramic ball grid array (CBGA) joints, and then distributed utilizing 'controlled collapse chip connection' (C4) bumps. The dies are bonded using micro connects. Through-silicon via (TSVs) provide electrical connectivity among the layers.

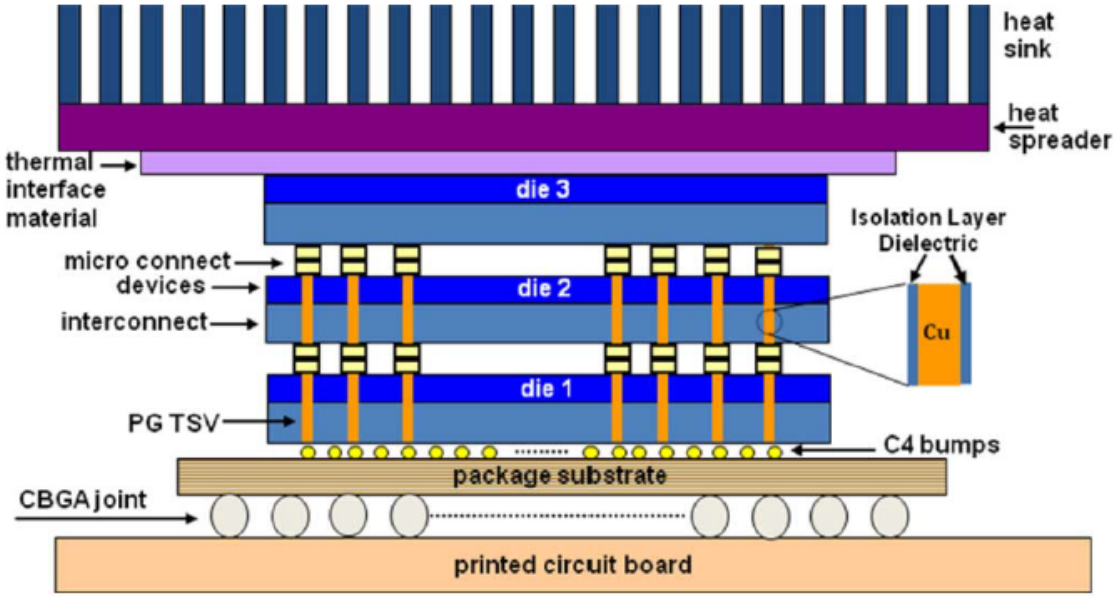
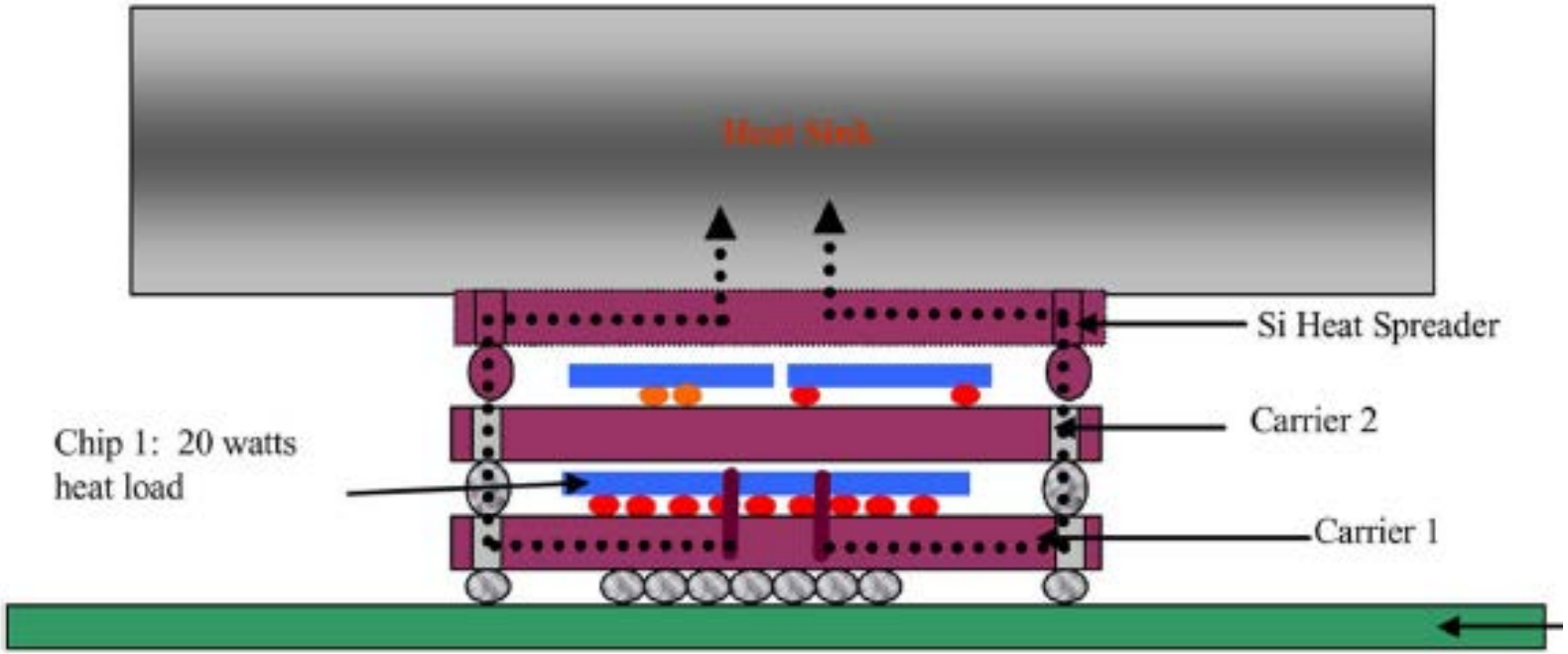


Fig. 1. Illustrative 3-D system assuming face-to-back metallic bonding with microconnects.

Power Delivery Design for 3-D ICs Using Different Through-Silicon Via (TSV) Technologies, Nauman H. Khan, et.al, IEEE Trans on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 4, April 2011

A 3-D stacked package with Si interposers was developed to integrate one ASIC and two memory chips in a package.

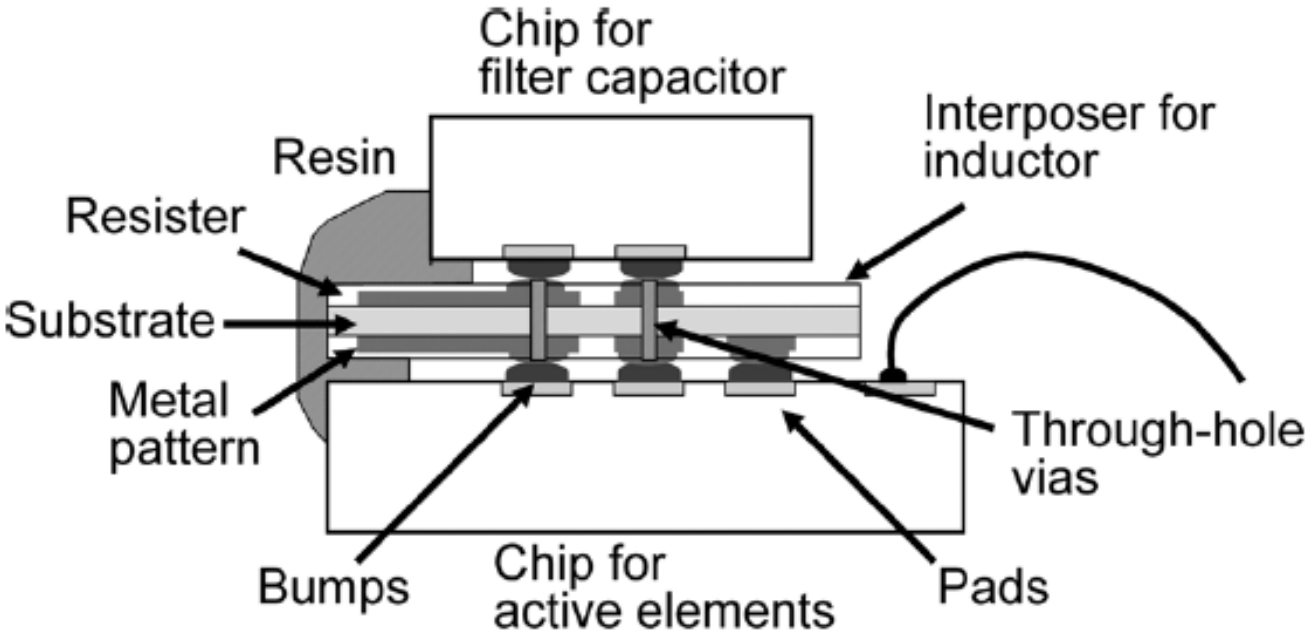
- Electrical connections in the silicon interposer were formed by through silicon via.
- Silicon interposer has much higher thermal conductivity than organic interposer, therefore the package thermal resistance is lower.



"Development of 3-D Stack Package Using Silicon Interposer for High-Power Application," Navas Khan, Seung Wook Yoon, et.al., IEEE Transactions on Advanced Packaging, Vol. 31, No. 1, Feb 2008

Organic On-Chip Buck Converter

An on-chip buck converter which is implemented by stacking chips and suitable for on-chip distributed power supply systems achieves a maximum power efficiency of 62% for an output current of 70 mA and a voltage conversion ratio of 0.7 with a switching frequency of 200 MHz

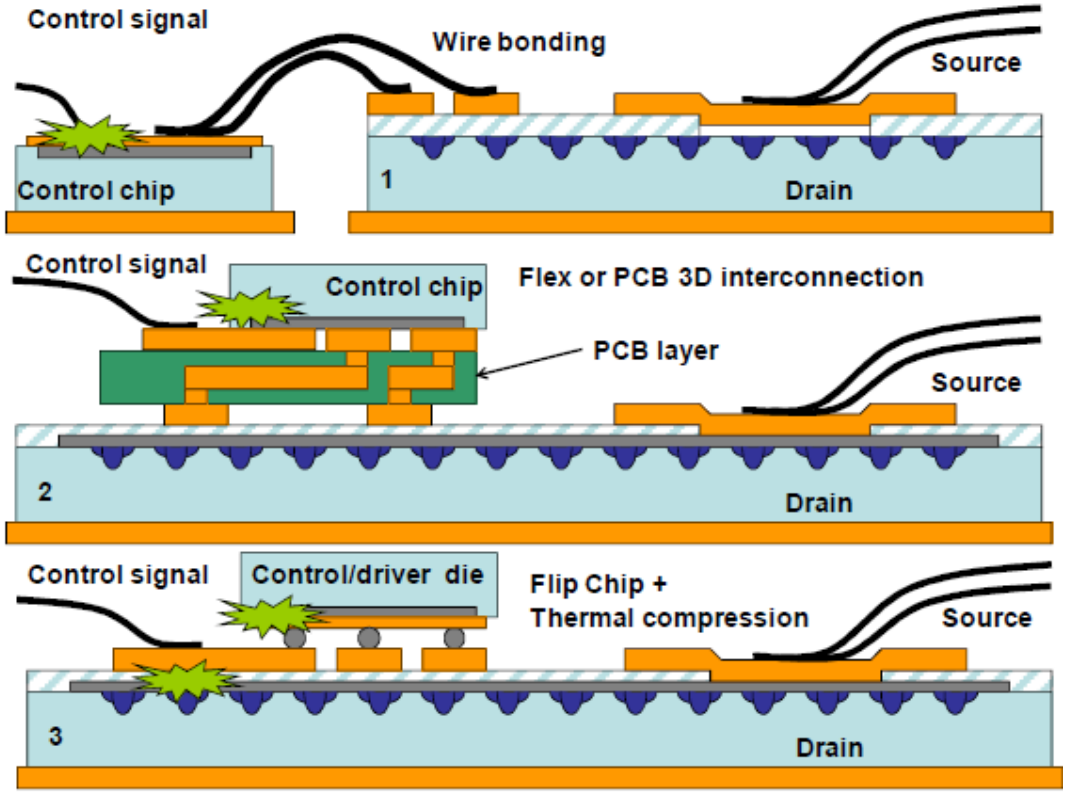


"Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs," Kohei Onizuka, *et.al., IEEE J. of Solid-State Circuits, Vol. 42, No. 11, November 2007*

Driver on Chip - PSysP

This paper presents a three dimensional interconnection solution based on the idea to flip chip the gate driver directly on the surface of the power device, simplifying and optimizing the packaging and the interconnections among the two devices and improving the overall performances.

"A novel Power System in Package with 3D chip on chip interconnections of the power transistor and its gate driver," Simonot Timothé, et.al., Proc. of the 23rd Int'l Symp on Power Semiconductor Devices & IC's, San Diego, CA, May 23-26, 2011



Possible interconnection solutions between the power die and its driver

TIM Interposer

The thermal resistance between semiconductor and heat sink as a consequence of the thermal interface material in use is of major importance. It has to be as small as possible and, in best case, may not change throughout the predicted lifetime. The primary concerns are: Improving thermal conductivity, Minimizing the contact resistance, and Long-Term Stability

"Improved Thermal Transfer For Power Modules," Dr.-Ing. Martin Schulz, Infineon Technologies (Article Power Electronics Europe 03/2013)

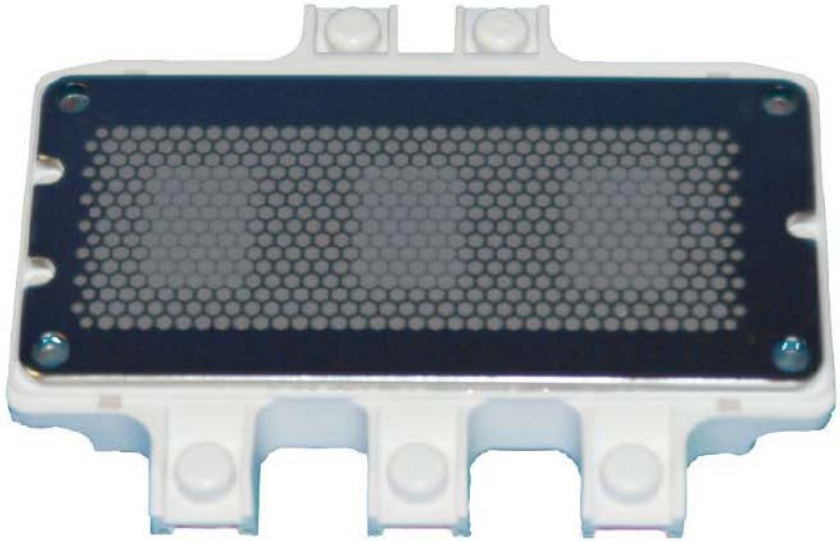
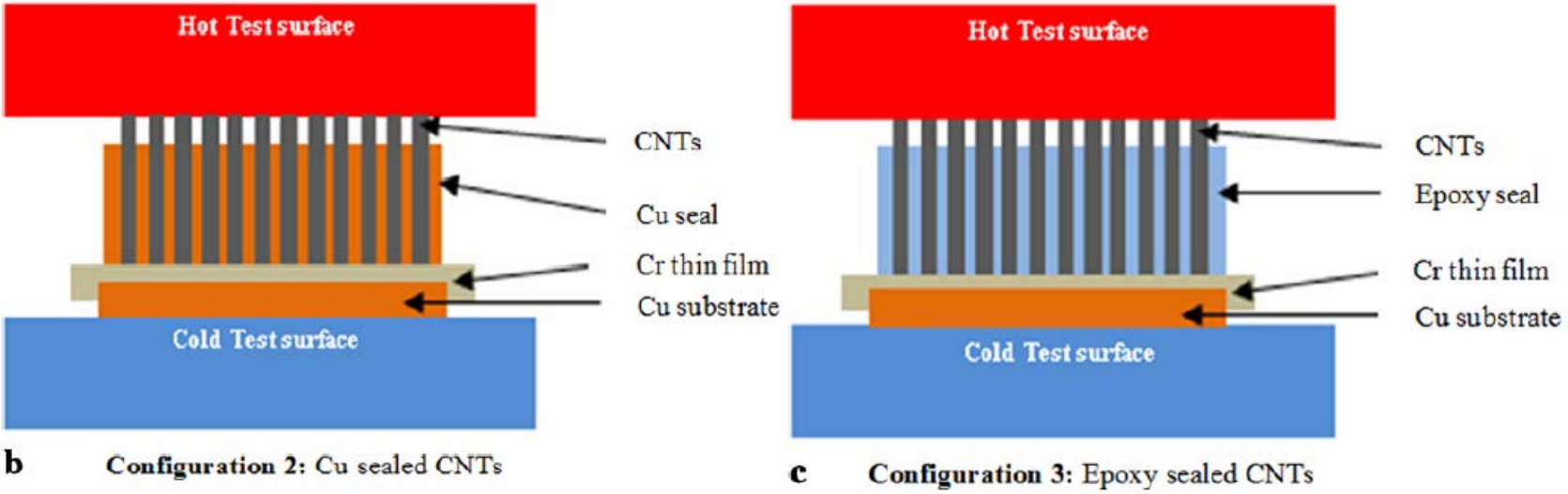


Figure 4: EconoPACK™ 4 with TIM applied. Stencil printing enables the application of locally optimized volumes using inhomogeneous patterns.

Use of CNT as Thermal Interposer

PECVD was used to synthesize vertically aligned CNTs. The measured thickness and length was ~100 nm and 200–300 nm, respectively.

- The strength of the CNTs was increased by filling the gaps between tubes using Cu and epoxy sealant.
- The observed results suggested the use of epoxy sealed CNTs as efficient TIM material in solid state device packaging industries.

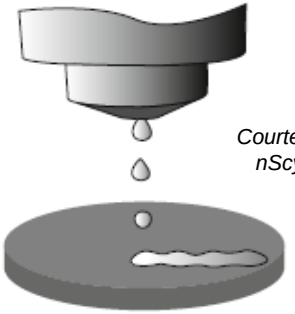


"Thermal resistance of CNTs-based thermal interface material for high power solid state device packages," Y.T. Lee · S. Shanmugan · D. Mutharasu, Appl Phys A, DOI 10.1007/s00339-013-7676-5

Classification of Relevant AM Processes

Non-Contact (Droplet)

Dispenses small droplets
Creates fine geometries
Up to 0.5mm from surface
Up to 50µm thickness, Platable
Multi-jet w/ multi-material



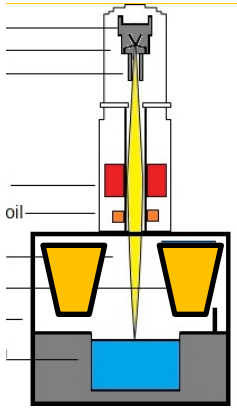
Courtesy of nScyript

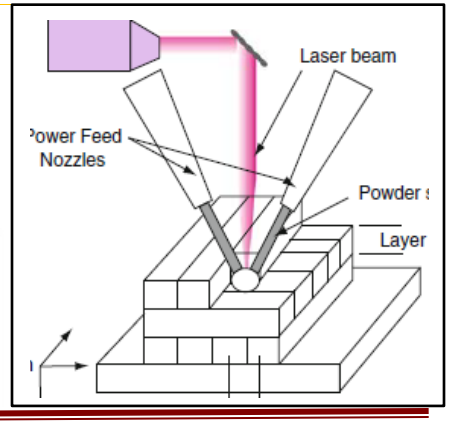
Near-Contact (Extrusion)

"Direct Write"
Extrudes ink/paste
Requires flat surface/contours
Dia.: 100µm - >1.5mm, Platable

Fused Deposition

"Discrete particle, Beam, SL, Laser Sintering, …"
Fused metals, sintered polymers, etc.
From a vat of material or creation of *composites*
Dia: ~200µm – …mm (e.g. welding fillet)



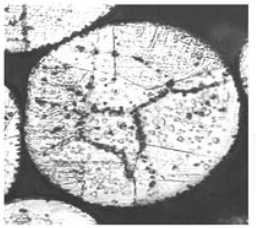


MATERIALS: OFE Copper

Material/Parameter	EBM Copper	OFE (C10100) Copper
Density (g/cm^3)	8.84	8.90
Conductivity (% IACS)	97	102
Tensile strength (KSI (MPa))	25 (172)	32 (220)
Yield strength (KSI (MPa))	11 (76)	10 (69)

New

Reuse

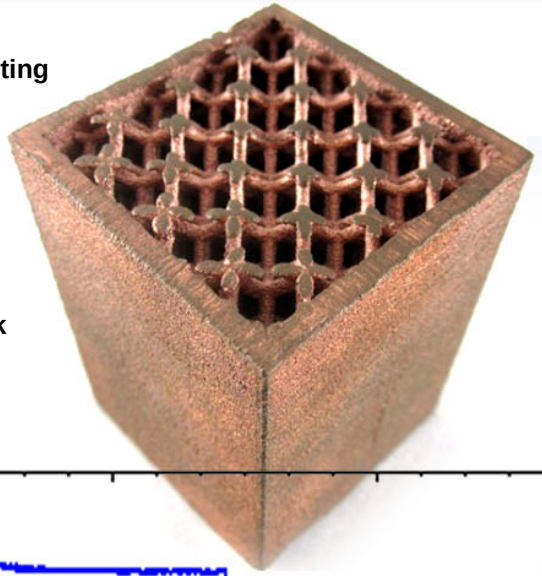


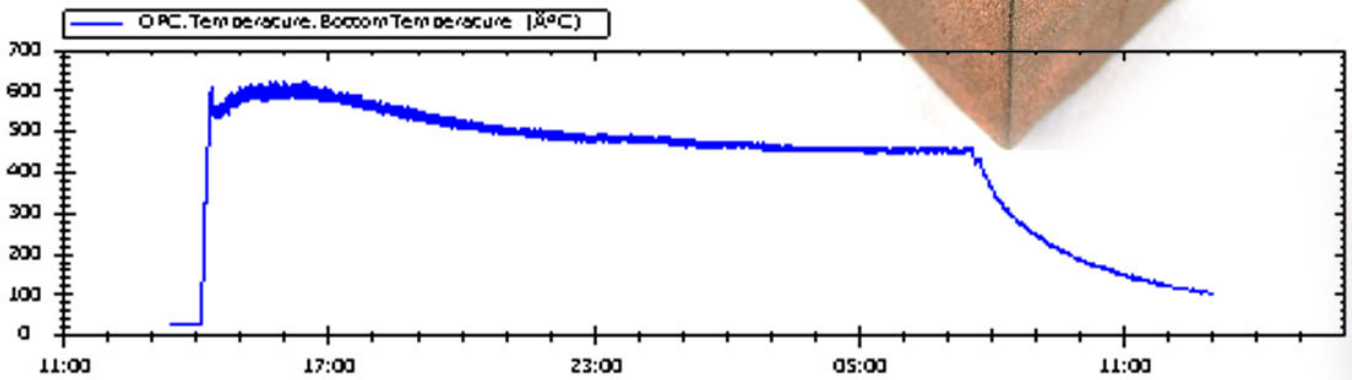
Applications:

Normally Conducting Radio Frequency Photoinjectors

Optimized Thermal Management

The Coolest Rook EVER

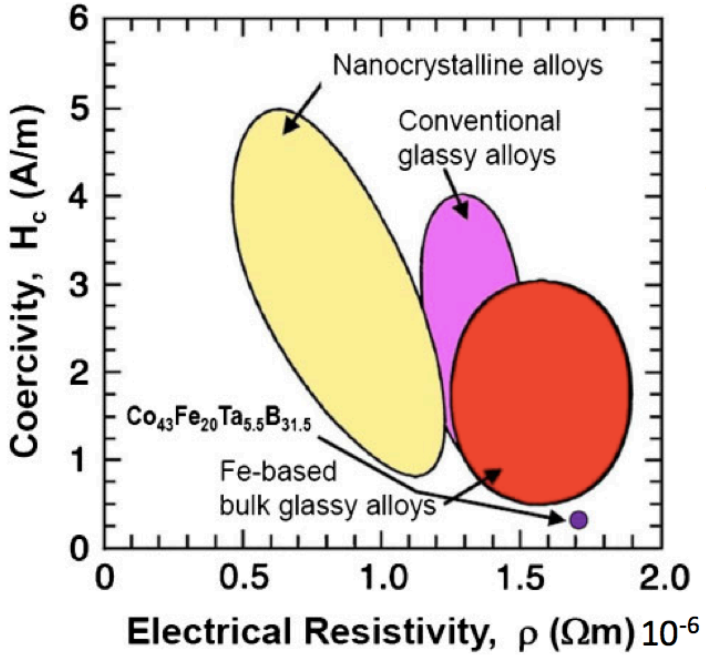




Future Magnetics Opportunities

exmet Amorphous metals without limitations.

Coercivity and resistivity



Prepared for Douglas Hopkins, NC State.

Electrical steel (order of magnitude) :
$H_c = 10^2$ A/m
$\rho = 10^{-7}$ Ωm

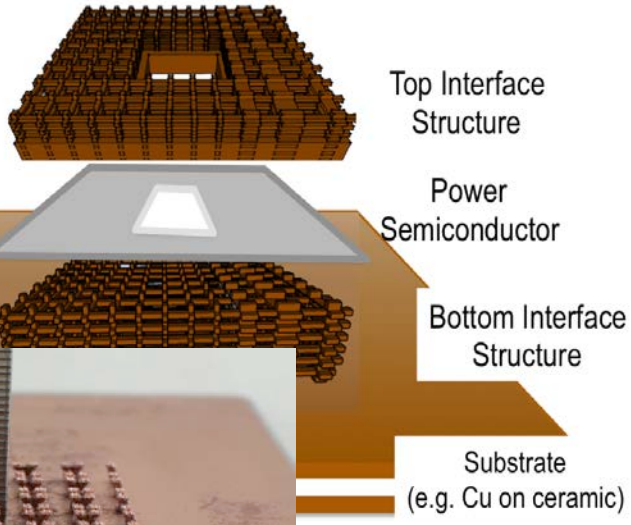
exmet Amorphous metals without limitations.

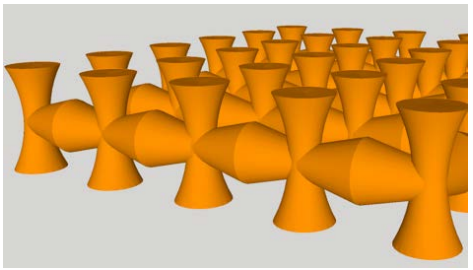
Coercivity and resistivity 2

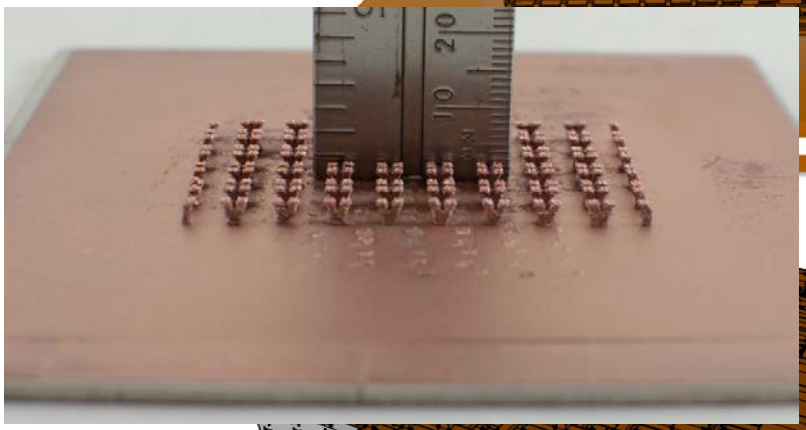
Prepared for Douglas Hopkins, NC State.

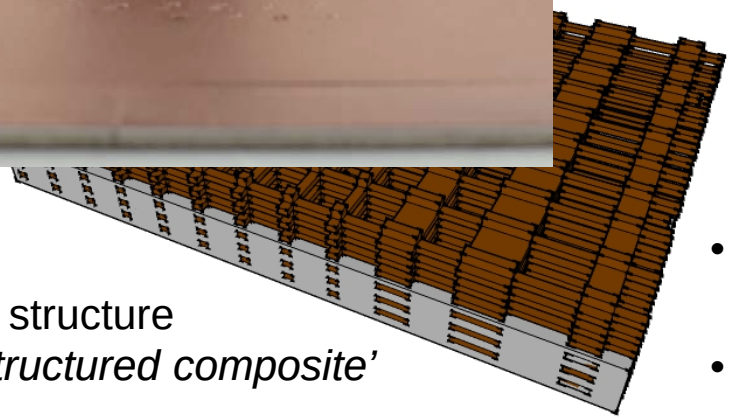
An Interfacial Power Die Interposer

Controlling the Mechanical interface while impacting the Thermal performance



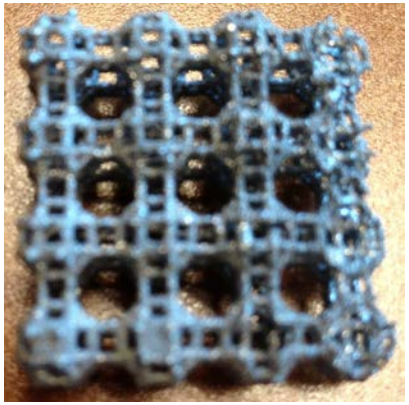






Solder fill of structure creates a *'structured composite'*

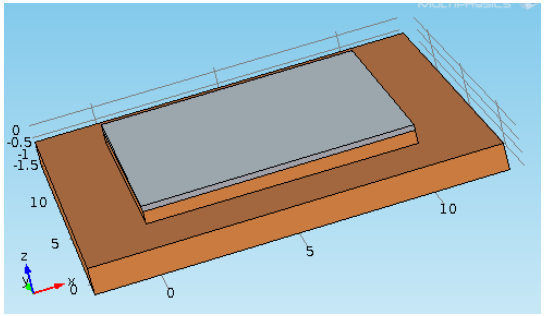
Vary the wire thickness, spacing, distributed density, contour, and cavities

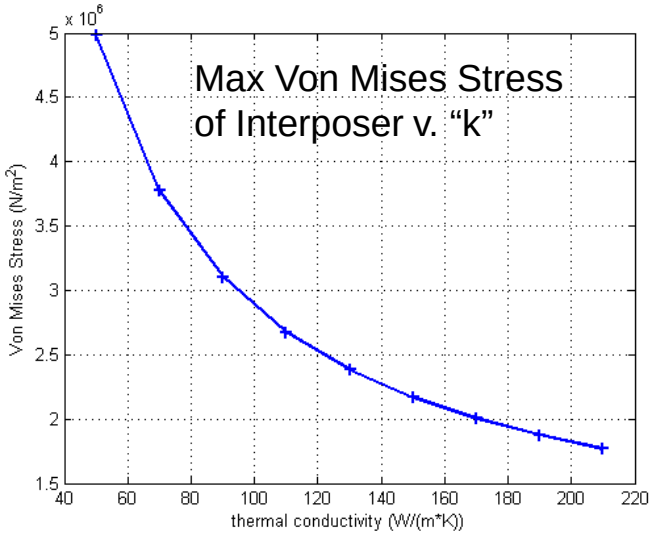


- 150µm - 200µm wire diameter
- Cu, Al, Ti, Ag…

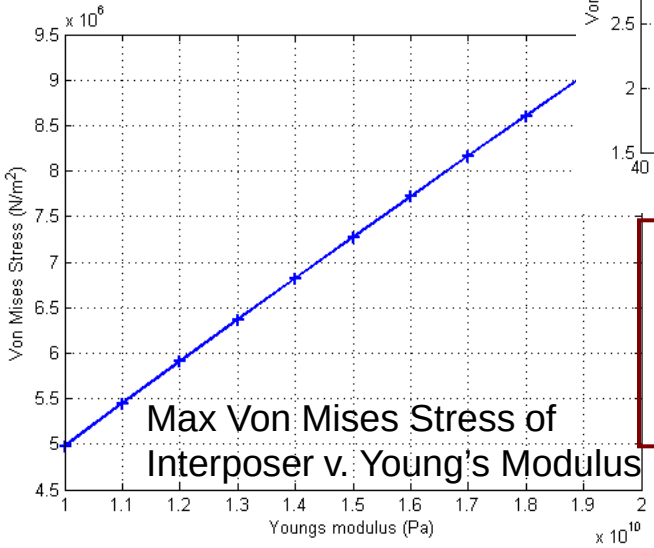
Creating Structured Composite Interposer

Material Property	Cu	Sn60Pb40	units	Variable Range	VonMises Stress [N/m^2]
Coef Therm Expan, *CTE*	$1.7x10^{-5}$	$2.1x10^{-5}$	[1/K]	$0.1x10^{-5} – 2.1x10^{-5}$	$1.6x10^{6} – 5x10^{6}$
Modulus, *E*	$1.1\ x10^{5}$	$1\ 0x10^{3}$	[MPa]	$1\ x10^{4} – 2\ x10^{4}$	$5x10^{6} – 9.5x10^{6}$
Thermal Conductivity, *k*	400	50	[W/mK]	50 - 210	$5x10^{6} – 1.75x10^{6}$

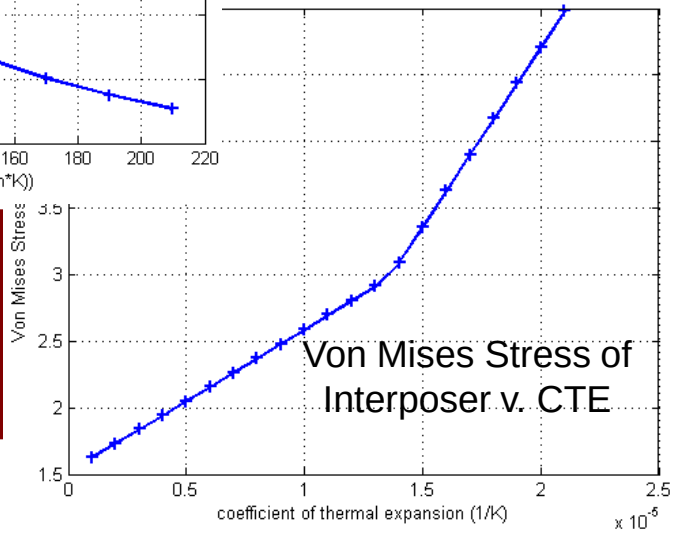




Note: if Interposer is all copper (i.e. Si chip sits directly on Cu), the max stress is 8.22 MPa



ADJUST SOLDER LAYER TO SIMULATE INTERPOSER



Rapid Prototyping for High Temperature?

Many materials are being rapidly developed for 3D printing. A classification of interest uses multiple forms of curing printed organics. Example: UV cure is combined with Thermal cure to allow flexible object creation with post strengthening.

Measurement	Condition	Metric
Tensile Strength	ASTM D 638	66 - 68 MPa
Tensile Modulus	ASTM D 638	7,600 - 11,700 MPa
Elongation at Break (%)	ASTM D 638	1.4 - 2.4 %
Flexural Strength	ASTM D 790	124 - 154 MPa
Flexural Modulus	ASTM D 790	8,300 - 9,800 MPa
Impact Strength (Notched Izod)	ASTM D 256	13 - 17 J/m
Heat Deflection Temperature UV Postcure only UV Postcure only UV + Thermal Postcure (120°C)	ASTM D 648 @ 66 PSI @ 264 PSI @ 66 PSI	 65 - 66 °C 65 °C 267 - 284 °C
Hardness, Shore D		
Co-Effcient of Thermal Expansion	ASTM E 831-93 TMA (T<Tg, 0-20 °C) TMA (T<Tg, 90-150 °C)	 33 - 44 (x10-6 m/m °C) 81 - 98 (x10-6 m/m °C)
Glass Transition (Tg)	DMA, E"	71 - 83 °C

Shown is data for Acura® Bluestone™ nanocomposite for use with solid-state stereolithography systems

Note the >267˚C HDT after a Thermal post cure.

Thermal curing is required in materials that are metal loaded. Also, UV composites are used for printing, while Thermal curing provides strength.

Summary

Interposers are commonly considered primarily for chip-to-chip stacking applications, such as TSV (Thru Silicon Via), or stacked packages for 'low temperature' applications.

Interposers for electrical, thermal and mechanical (including hydraulic) energy translation can now be considered. Interposers can be multiple-energy and non-planar through 3D printing.

Printed Interposers can be used in modularization for creating customized coupling or attachment between modules for tailored end-use products.