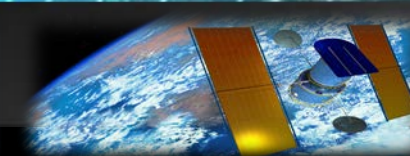


Power Packaging Considerations for High End Servers

Rick Fishbune

IBM Distinguished Engineer
IBM STG/ISC Power Technology



TOPICS

- 3D Packaging Considerations
- High Performance Computing Server Example
- iNEMI DC-DC Project

Quotes to remind you of our ability to predict the future

**“Those who have knowledge, don’t predict.
Those who predict, don’t have knowledge.”**

- Lau Tzu, 6th Century BC Chinese Poet

“Computers in the future may weigh no more than 1.5 tons. ”

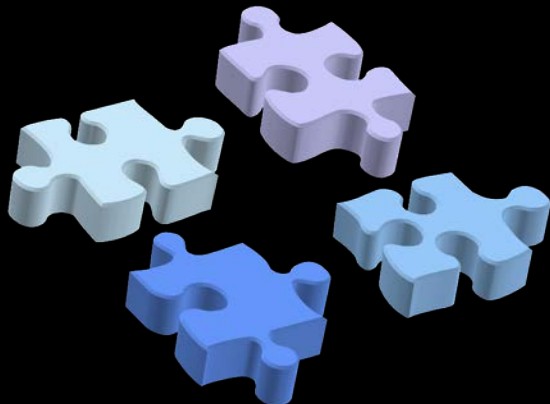
- Popular Mechanics, 1949

“There is no reason anyone would want a computer in their home. ”

- Ken Olsen, founder of DEC, 1977

“I believe OS/2 is destined to be the most important operating system, and possibly program, of all time.”

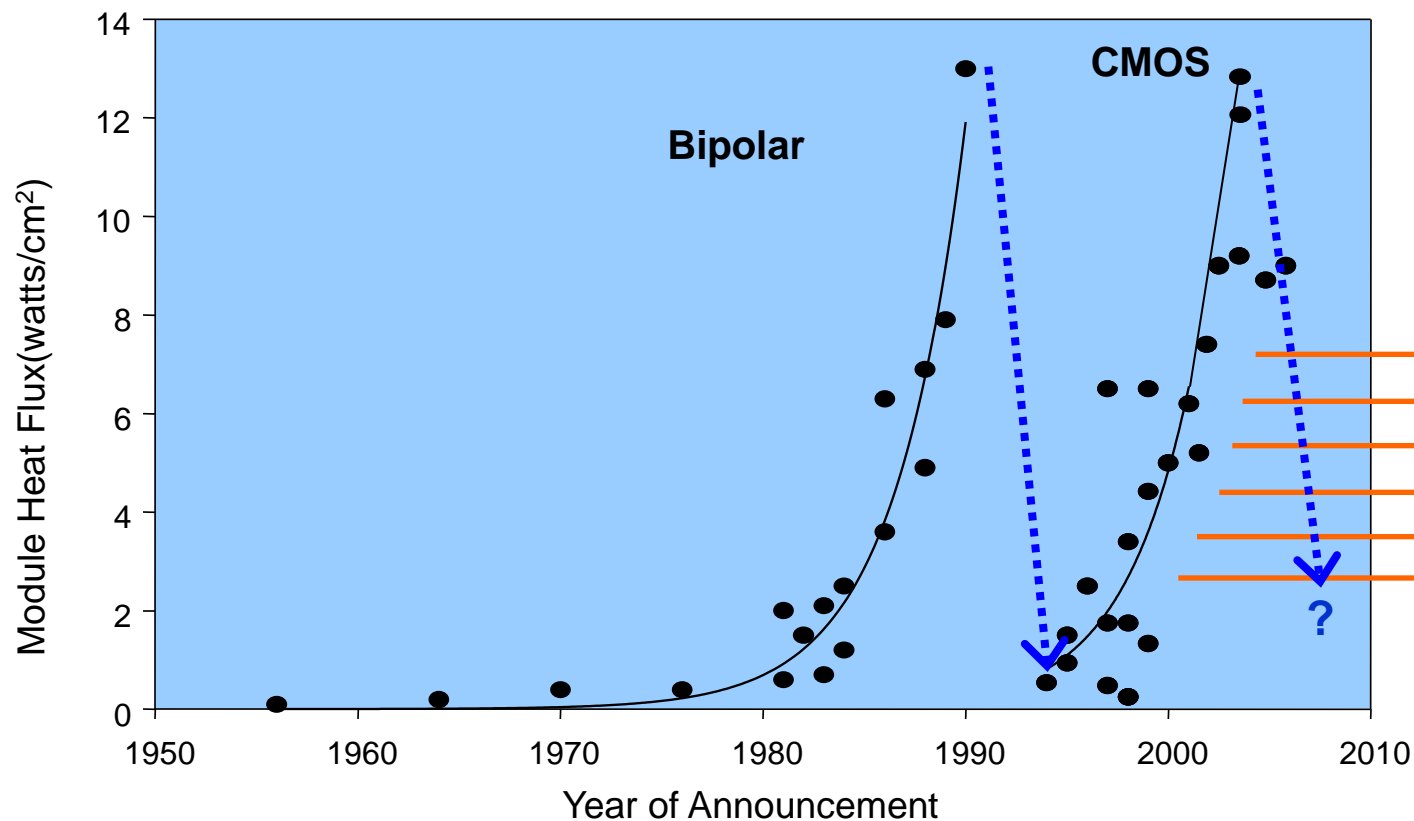
- Bill Gates, 1987



“Everyone is asking me when Apple will come out with a cell phone. My answer is, ‘Probably never’ ”

- David Pogue, NY Times, 2006

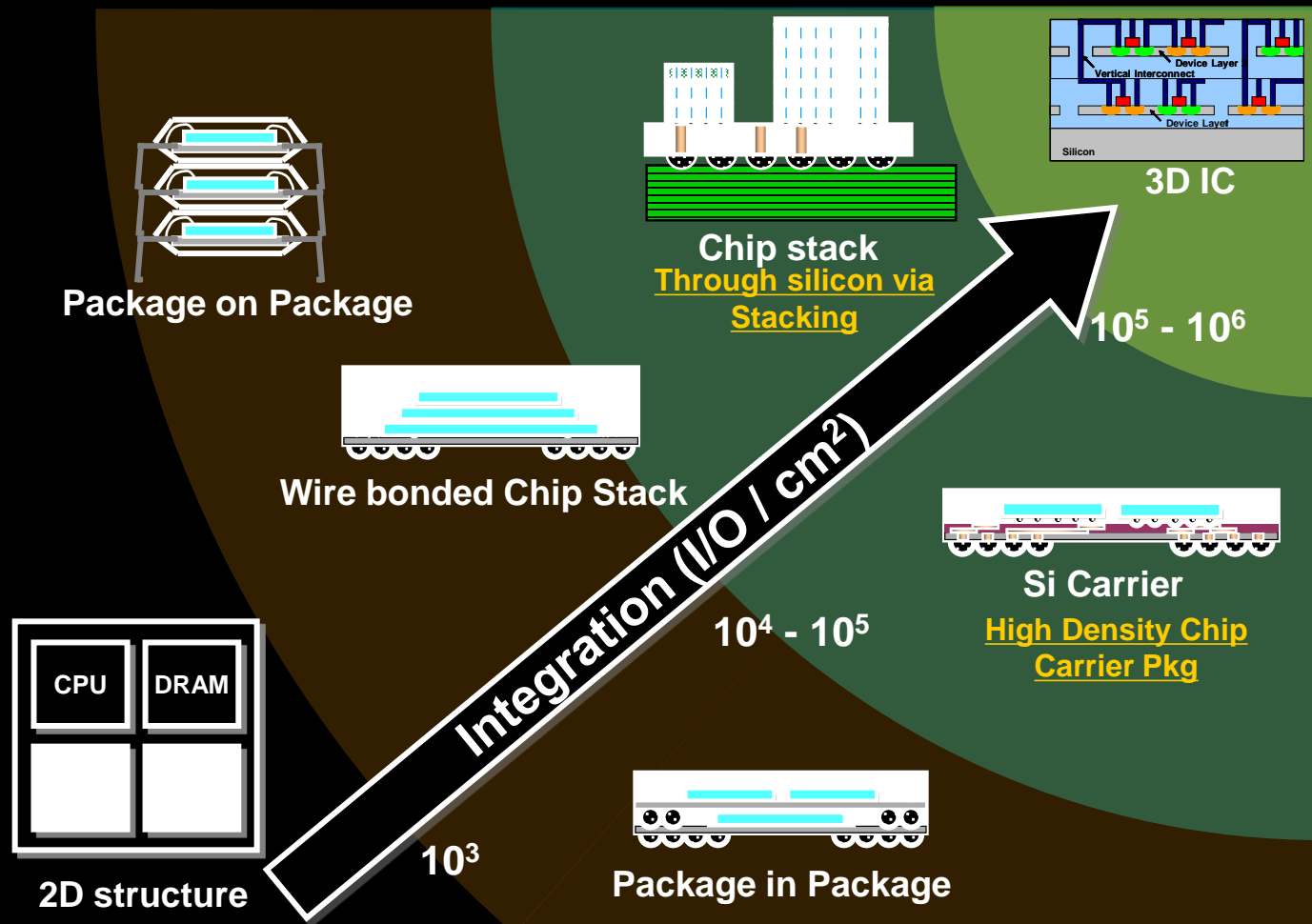
Transition to 3D CMOS



Opportunity
for 3D Si

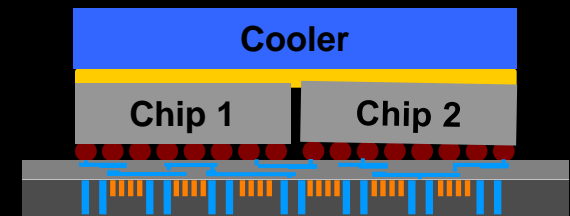
Emerging 3D Silicon Integration

- Another way to extend Moore's Law

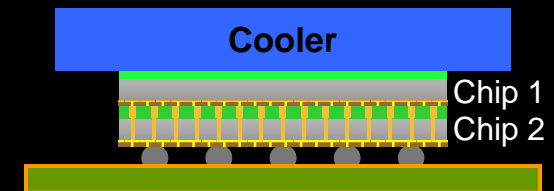


3D Structures and Cooling Approaches

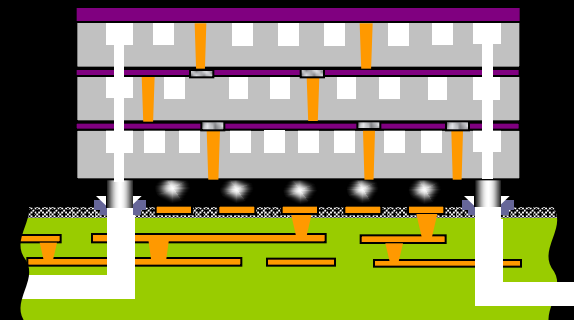
- **Chips on a Si carrier**
 - Have direct access to the back of each chip
 - Mechanical issues predominate over thermal issues
 - Must develop a very good thermal interface material thick enough to handle chip non-planarity
- **Stacked chips of moderate power**
 - Can be cooled from the back of the stack
 - Must improve conductivity through complex stack with many thermal interfaces
- **Bring cooling into the stack**
 - Far more complex, but might allow higher stacks



Cooling one layer of chips on a Si carrier

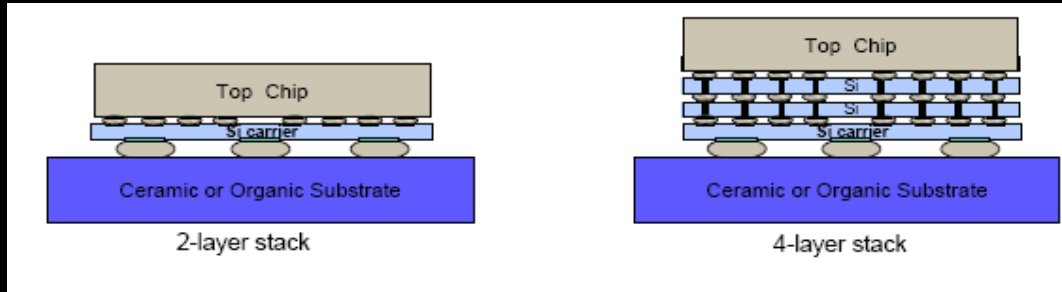


Cooling a chip stack from the back

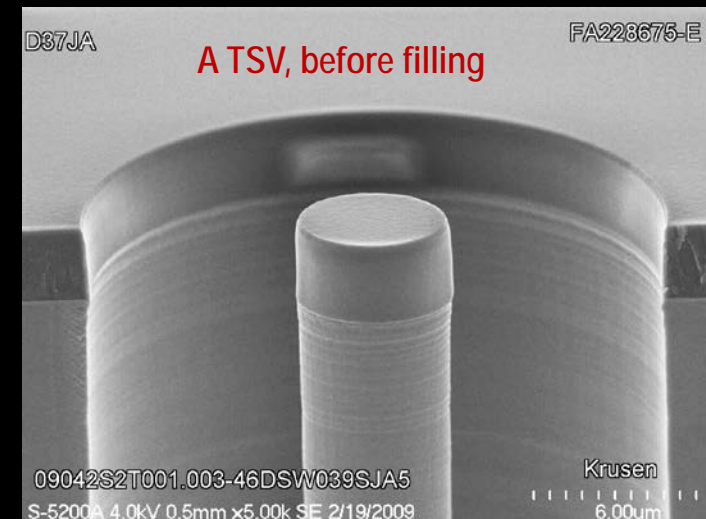
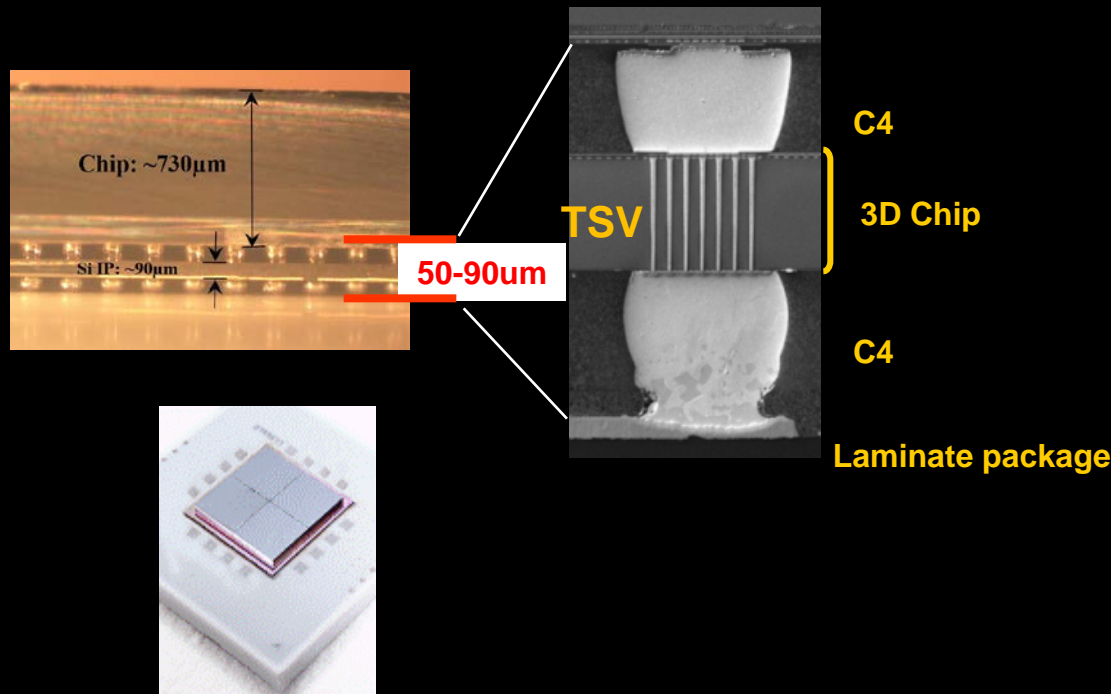


Bringing liquid cooling into chip stack

Thru – Silicon Vias (TSV)



Current through base interconnect increases as number of stacked chips increase – **critical to understand flow through each ball**

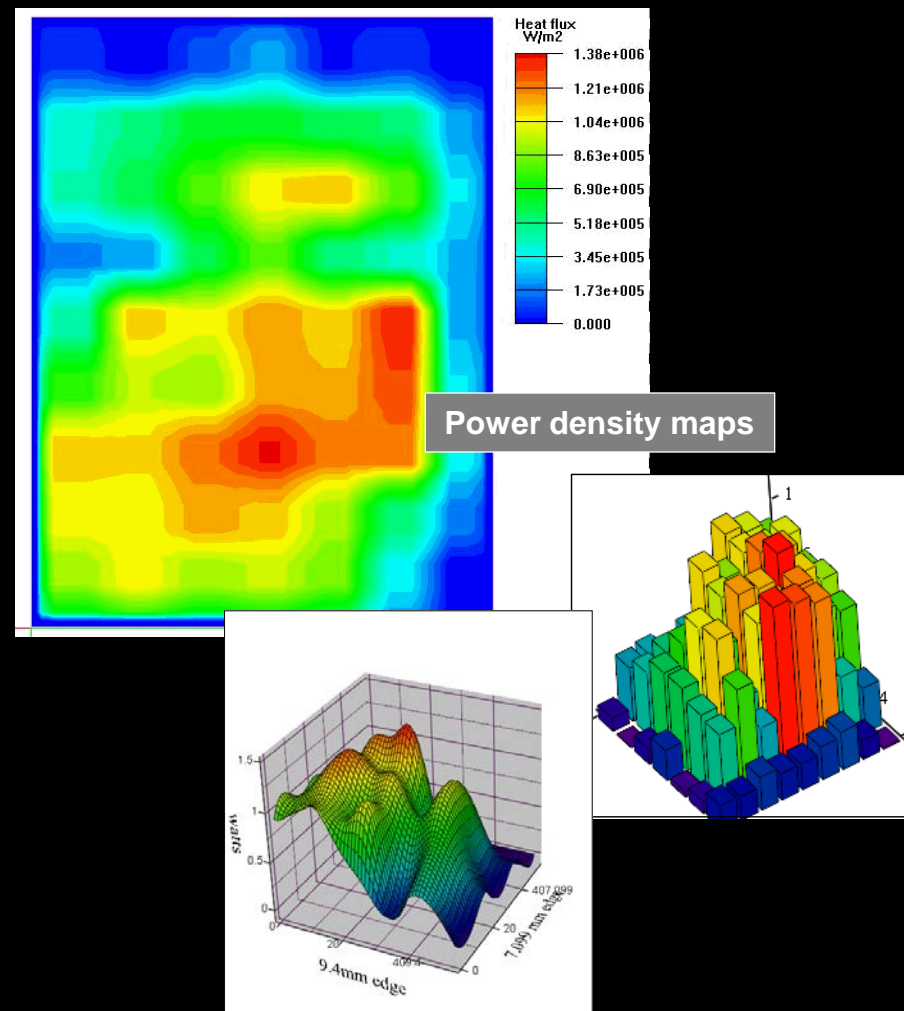


Power Density Maps per Layer

Detailed knowledge is important

- Understanding the power density
- Understanding the impact of higher temperatures and gradients
- Having the ability to bring the appropriate amount of technology to the application

T_{amb}	T_{j_nom}	Thermal Resist. C/W	TIM cond.
25	57.5	0	Uniform heating
25	64.1	0.15	Best can do grease
25	91.9	0.76	2 mil PCM interface



An Example of Power Packaging Challenges in High End Servers

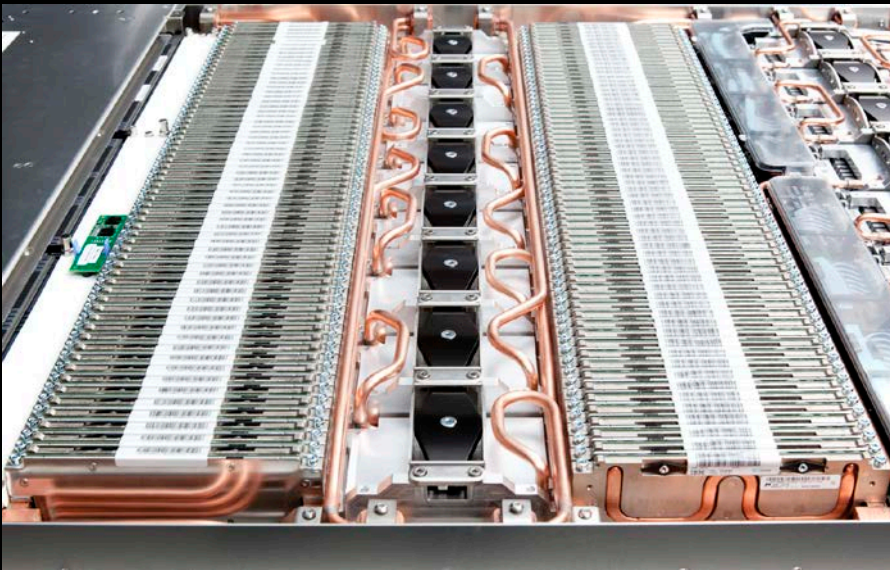
IBM High End Server System



**Each Compute Drawer Uses ~19kW
Single Rack System Rated up to 235kW**

Part of The Compute Drawer

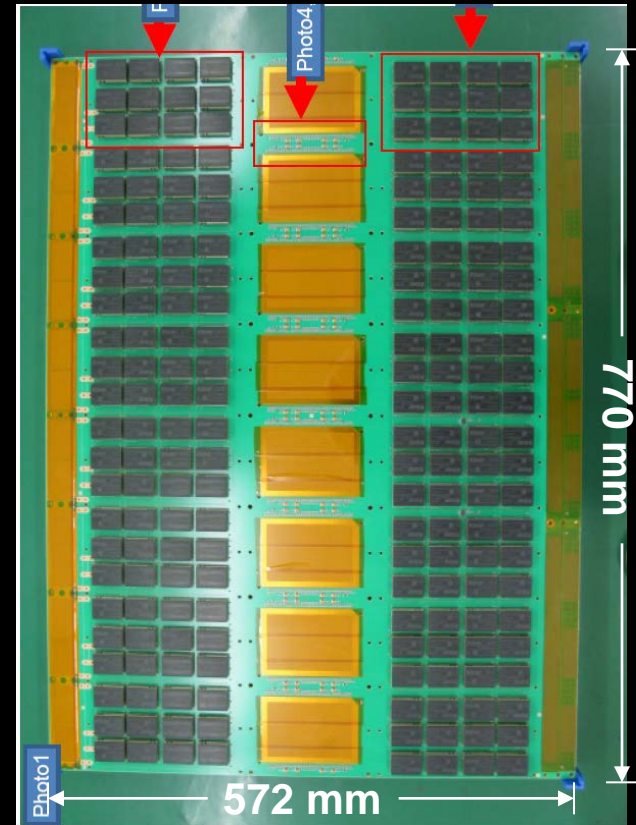
Top Side



Densely packaged with eight *QCMs
and 128 DIMMs

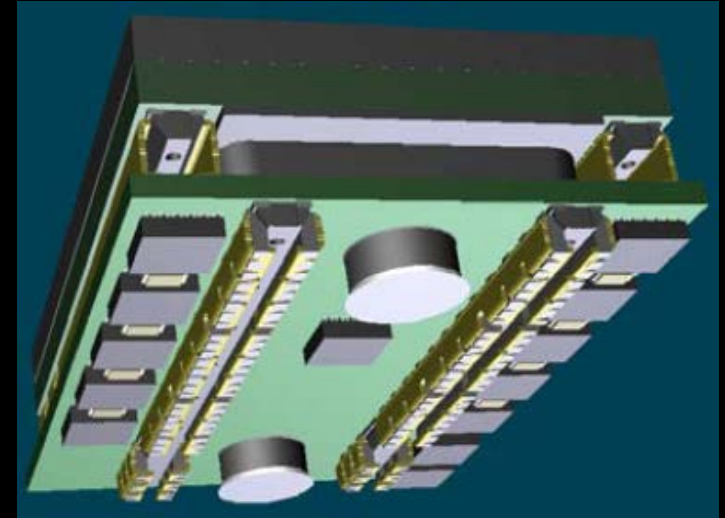
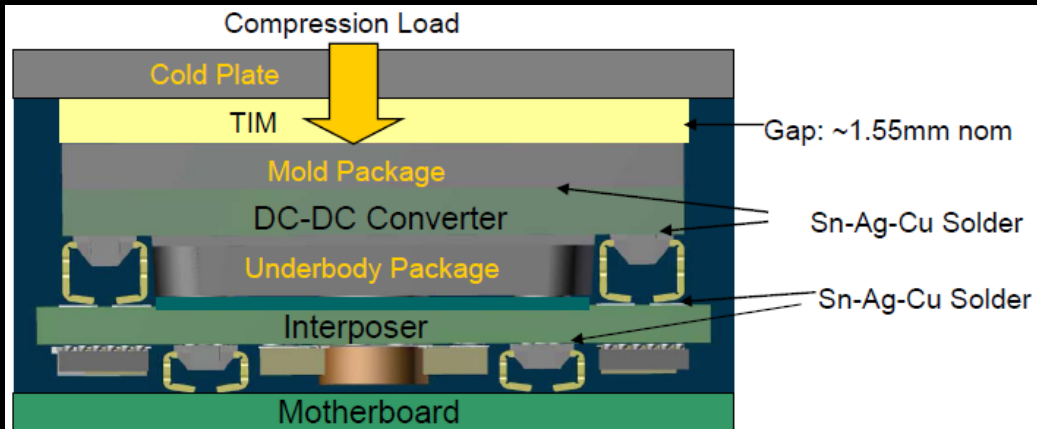
*QCMs = Quad-core modules

Bottom Side
Cold Plate & TIM Removed



Power is N+2 redundant per
voltage level per octant
192 total power converters

Power Packaging Concern Areas (192x per drawer)



1. High compression loading force required for thermal bond to cold plate
2. Effect of multiple reflows on metal interfaces
3. Effects of multiple reflows on adhesive interfaces
4. Effects of long time above liquidous due to large size of the card (~300 sec)
5. Vulnerability of bare dice to physical damage
6. Verification of good solder attach to card (44 layer motherboard)
7. Rework of the power package
8. Long term electromigration concerns due to current density

Application Space Trends

- Changes in Application Conditions, Typically:
 - Increasing Operating Temperatures
 - Increasing Interconnect Currents
- Shrinking Interconnect Sizes
 - Increases Current Density Values
- Die Size Changes
 - Larger Die: Increases Total Power / Ground C4 Counts
 - Smaller Die: Can Drive Reduction in Number of Connections
- RoHS Compliance: Pb – Free Interconnects
 - Pb / Sn Bumps Replaced with Sn / Ag Bumps

Can Electromigration be an Issue?

Electromigration

- **Electromigration** (EM) is the transport of material caused by the gradual movement of the atoms in a conductor due to momentum transfer driven by conducting electrons.
 - It causes a net atom transport along the direction of electron flow.
 - The atoms pile up at the anode, voids are generated at the cathode
 - The typical failure of a solder joint due to electromigration will occur at the cathode side.
 - Due to current crowding, voids form first at corners within a solder joint.
 - As the voids extend, electrical failures can result.
 - Electromigration also influences the formation of intermetallic compounds.

Similar mechanism as BEOL* EM, here driven less by geometry and more by the low melting point of the solder materials.

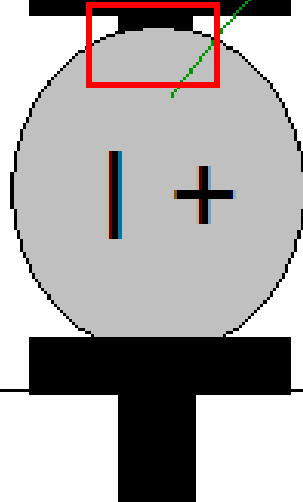
BEOL* = Back End of Line



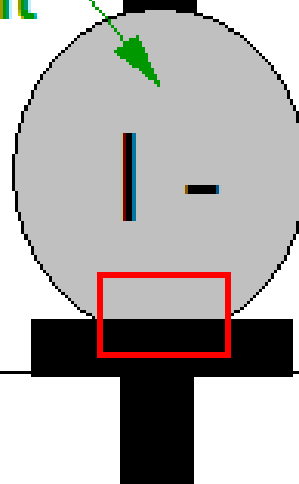
Electromigration Schematic

Electron
Flow

Current
Flow



Positive Bump
Power



Negative Bump
Ground

Chip / BLM Side

- BEOL Design
- BLM Thickness / Type
- C4 Solder Composition

Substrate Side

- Pad Metallurgy
- C4 Solder Composition
- Presolder Composition
- Substrate Design

Fails occur at transition point to solder!

Black's Law for Electromigration

$$t_{50} = \frac{A}{j^n} e^{\frac{\Delta h}{kT}}$$

Δh = Activation Energy
0.7 – 1 eV Typical

n = Current Density
Exponent
1.5 – 2 Typical

Performance Governed By:

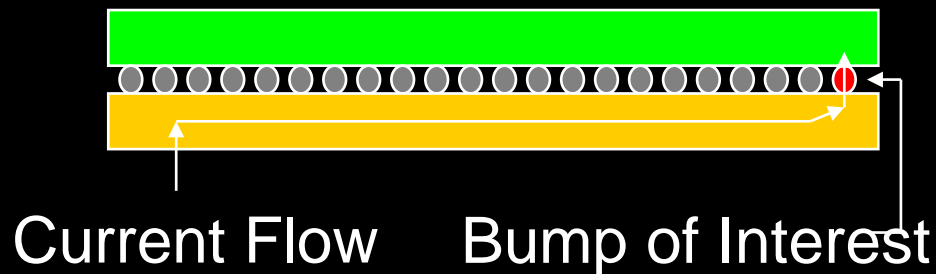
Application Temperature

Current Density (Local & Global)

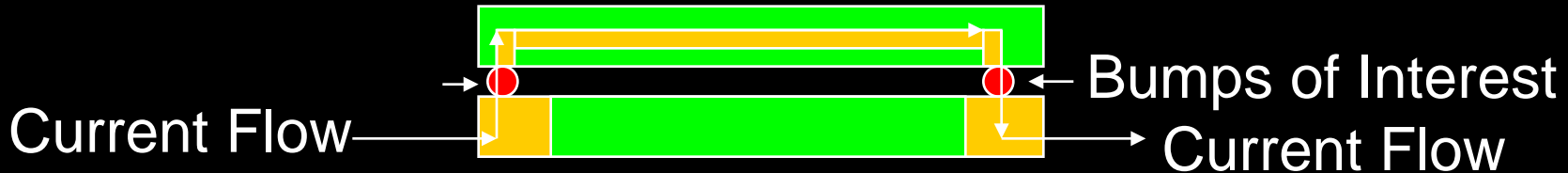
Materials System

Electromigration Test Vehicle Current Flow

Side View

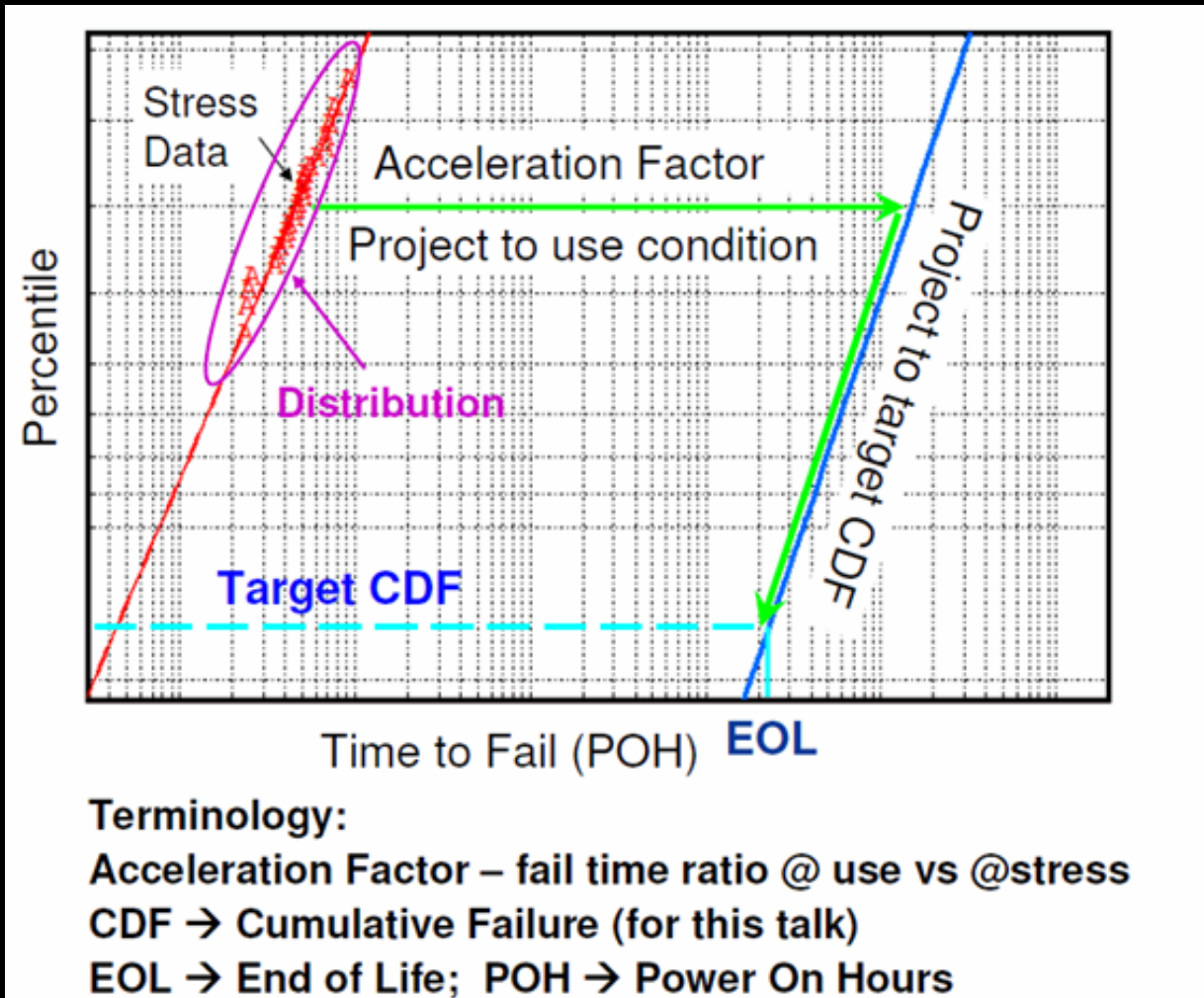


Edge View



Test Vehicle isolates current path to single ball of interest
Measure: Bump Resistance (4 wire Kelvin measurement)
Bump Temperature

General Reliability Testing Strategy



Projection Methodology Maintains Sigma from Accelerated Testing

Design Properties of Power Interconnects -- Example

Materials	Design Specifications
Solder Bump Alloy	SAC305
Solder Bump Diameter	300µm
Interposer Substrate Finish	OSP
Interposer Substrate Thickness	1.5 mm
Lead Finish	Ni, Au, Pd
Motherboard Thickness	6.35 mm (44 layers)

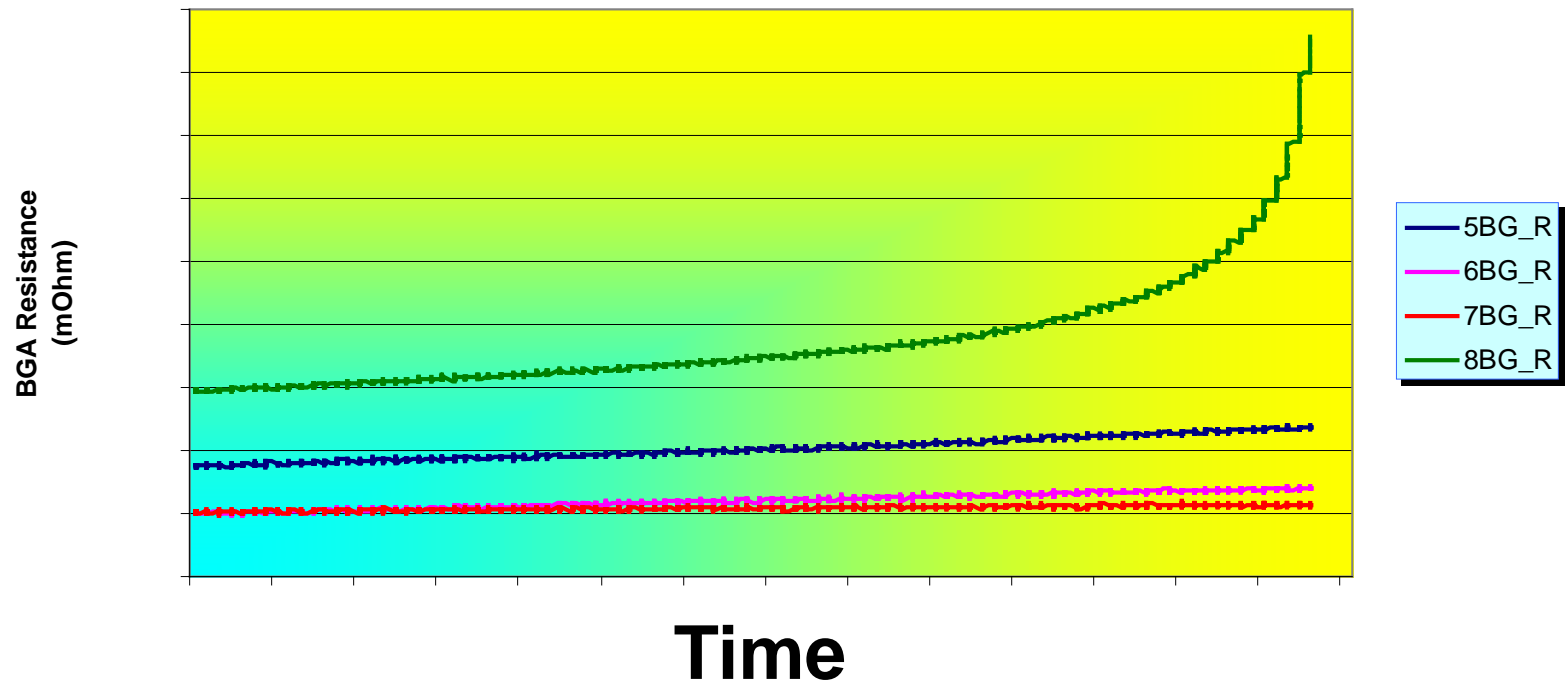
Design of Experiment

Test #	Ambient Temperature (° C)	Joule Heating (~ ° C)	BGA Temperature (~ ° C)	Current (A)	Current Density (A/cm ²)
1	125	12	137	6	0.85x10 ⁴
2	125	19	144	9	1.27x10 ⁴
3	135	12	147	6	0.85x10 ⁴
4	135	19	154	9	1.27x10 ⁴

Monitor delta-R of interconnect joint

BGA Interconnect Resistance Change

Test Run 4: 9A, 135°C



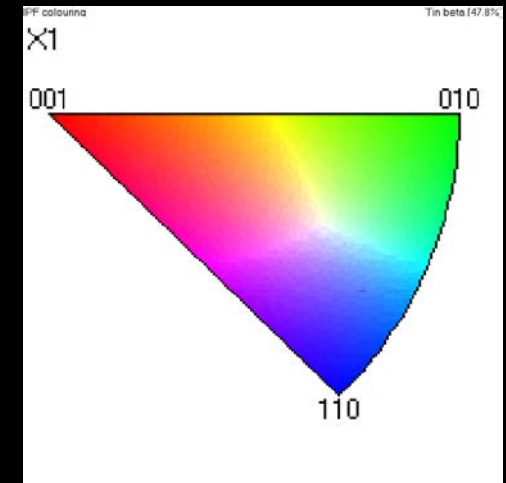
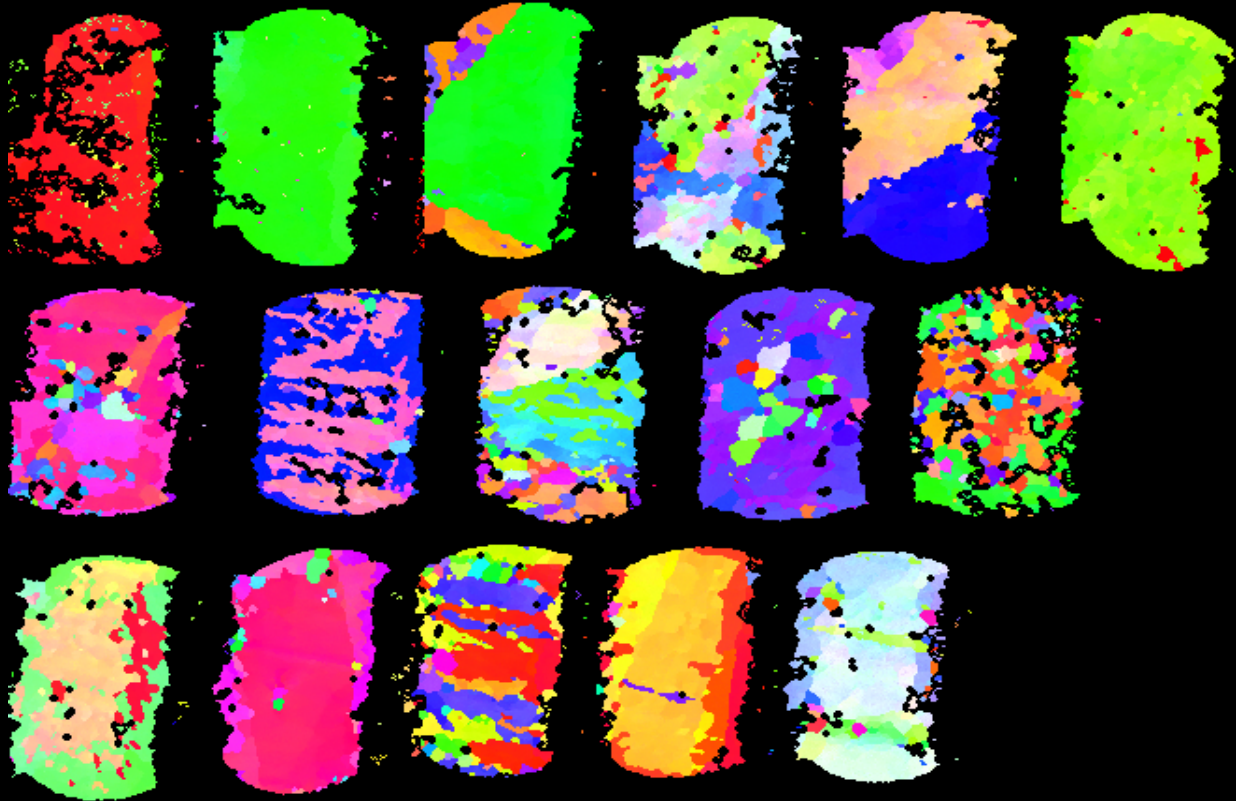
EM Test Results

- Question: Is the successful demonstrated EM life test using Black's law sufficient to prove the long term reliability of the interconnect?
- Answer: Maybe, maybe not

Why not?

Dependence Upon Grain Orientation

Sn Grain Orientation: C4 Bump Samples



=200 μm ; Map2; Step=1 μm ; Grid680x460

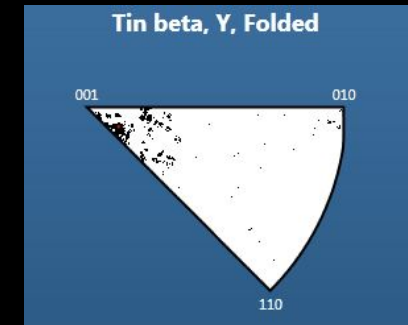
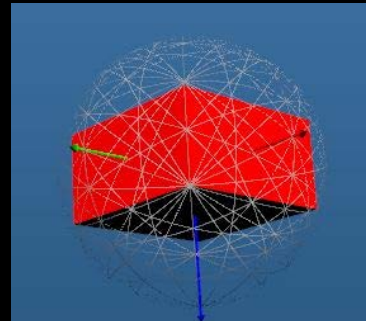
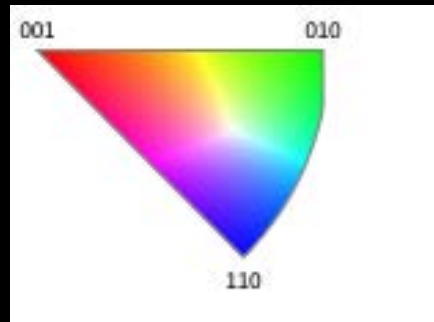
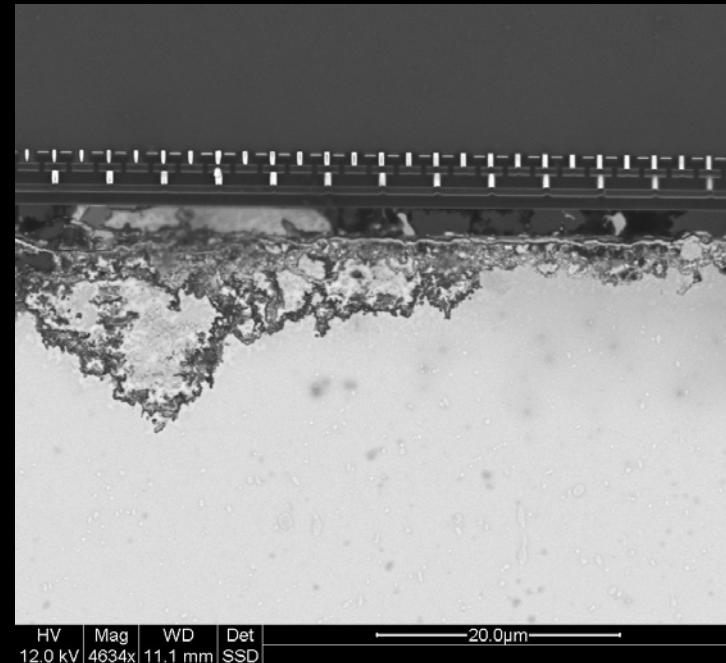
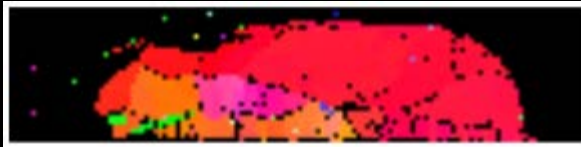
- **Electron Backscatter Diffraction (EBSD) Analysis Sampling of C4 Bumps**
 - **Shows Some Grains at 001 Orientation**

C4 stands for Controlled Collapse Chip Connection; used in die to substrate connection

Electromigration Studies

- Early Failure Samples Analyzed

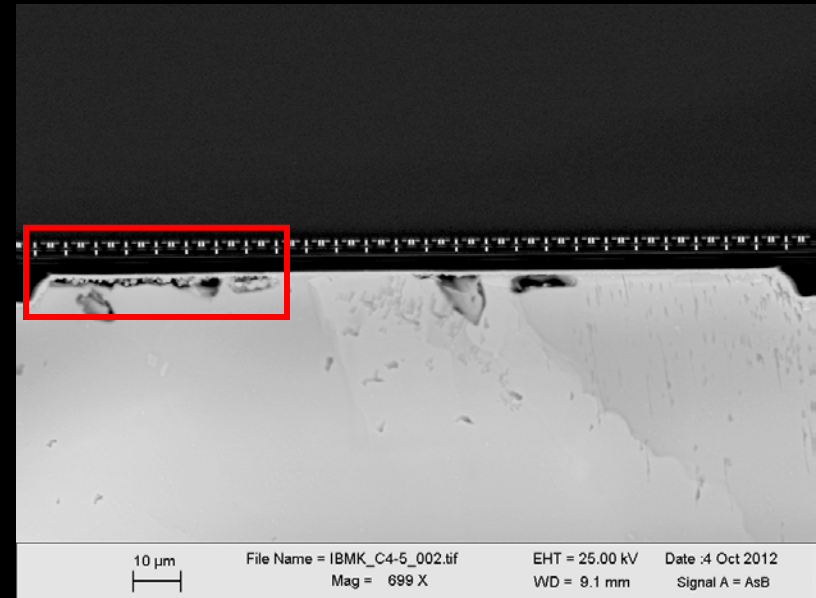
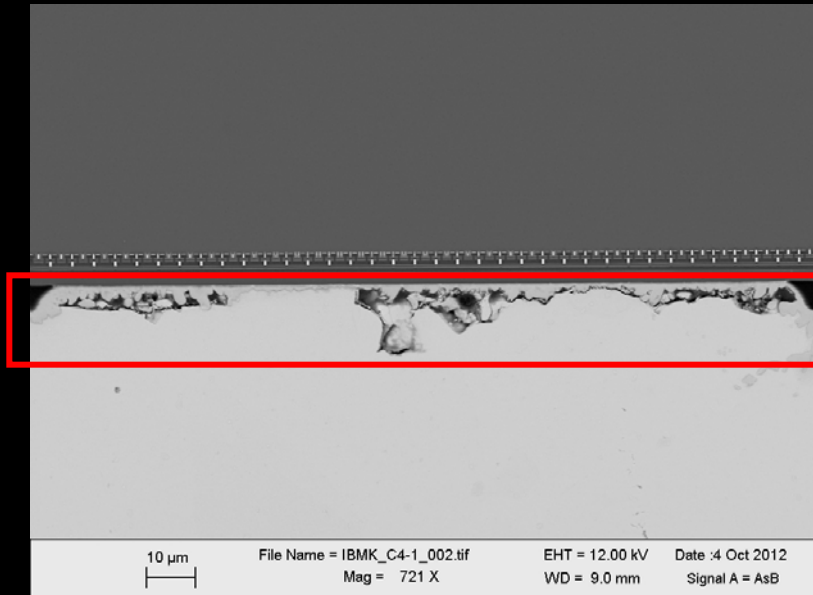
Failures all showed a grain structure with a 001 orientation!



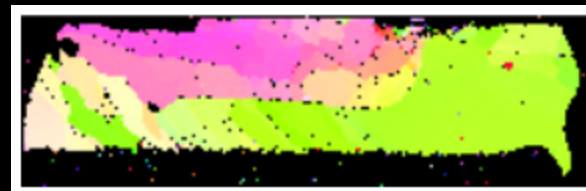
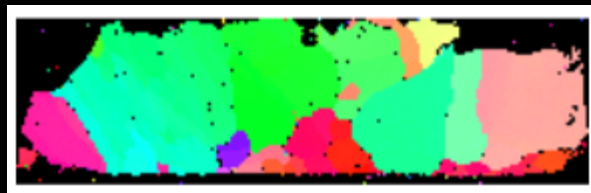
EBSD / SEM Analysis by J. Advocate, Y. Guo, B. Backes

Electromigration Studies

- Analysis of Long Lifetime Non - Failing Samples
 - Samples Show “Typical” EM Damage



- Long Life EM Bumps Do Not Have (001) Orientation!



EBSD / SEM Analysis by J. Advocate, Y. Guo, M. Jones

Conclusions

- Packaging Considerations for High End Servers must include:
 - Design package to minimize parasitics and uniform current flow
 - Review compression loading forces due to TIM & cold plate
 - Analyze the effect of multiple reflows on interconnects & adhesives
 - Consider the impact of long time above liquidous for large cards
 - Control thermal ramp rates during solder attach
 - Verify good solder attach to thick motherboards (44 layers)
 - Analyze / develop rework of the package
- In addition to traditional life tests such as accelerated thermal cycling, bias temperature & humidity, etc., an Electromigration (EM) analysis shall be done to verify whether EM concerns exist
 - Be aware of the impact that grain orientation may have on the expected life. Guard against (001) grain orientation.
 - Insure high power interconnects are redundant / fault tolerant
- Packaging & 3Di are critical to systems scaling
 - The board must be more Si – like
 - We need research in new materials, new system integration schemes, new test methodologies, and new fault tolerant schemes

DC-DC Power Module Phase 1 (Spec Development) Project

Problem statement: A modular DC-DC power supply is needed to provide low cost, higher efficiency to the datacenter/rack system.

Project Leader(s): Randy Malik, IBM (Rmalik@us.ibm.com); Rick Fishbune, IBM (fishbune@us.ibm.com)

Background or Context	Project Goals	Start:	7/2013	End:	6/2014
<ul style="list-style-type: none">Because of Higher cost of AC UPS if used in modular form, lower efficiency and reliability issues with AC systems, DC distribution at 380V DC is being considered to power the datacenters of the future. Although Telco already uses DC distribution, the 48V DC bus voltage is not sufficient to deliver sufficient power with the existing distribution cables for the future Telco systems.	<ul style="list-style-type: none"><u>Deliver a technical specification.</u>This will provide the participants with a specification that includes a complete assessment of the High Voltage DC – DC module and safety certification requirements that can be used to build a prototype module				
Key Learnings & Project Results	Next Steps & Timeline (if applicable)				
<ul style="list-style-type: none">The team is currently drafting the initial specification and plans on having the first draft complete by mid-March.Identified and reviewed standards that may have aspects that could be applied/need to be considered for inclusion in applicable specifications (eg. ETSI EN 300 132-3-1)	<ul style="list-style-type: none">Once the initial draft is complete, it will be reviewed and commented upon by suppliers and updated with their comments before being finalized by end of June.Phase 2 involves building and testing the prototypes to meet the electrical and mechanical specification. Based on measured results of the prototypes, the final electrical specification will be established regarding efficiency, power delivery, mechanical specification module size, and packaging.This will be done by building the module and testing the modules to meet the electrical requirements.Estimated Timeline: June 2014- 4th qtr 2015 (?)				

Acknowledgments

- I would like to acknowledge and thank the following IBM colleagues for their technical contributions and input to this work.
 - Subu Iyer – IBM Fellow – IBM Microelectronics Division
 - Jerry Bartley – IBM Distinguished Engineer
 - Thomas Wassick – Microelectronics Package Reliability
 - Yakup Bulur – IBM Power Technology Qualification Engineer
 - Eric Swenson – IBM Power Technology Qualification Engineer

- Excerpts From "The Charge of the Light Brigade"
By Lord Alfred Tennyson, Crimean War 1854

'Forward, the Light Brigade!
Was there a man dismay'd?
Not tho' the soldiers knew
Some one had blunder'd:
Theirs not to make reply,
Theirs not to reason why,
Theirs but to do and die:
Into the valley of Death
Rode the six hundred.

Cannon to right of them,
Cannon to left of them,
Cannon behind them
Volley'd and thunder'd;
Storm'd at with shot and shell,
While horse and hero fell,
They that had fought so well
Came thro' the jaws of Death,
Back from the mouth of Hell,
All that was left of them,
Left of six hundred.



BACKUP SLIDES