Increase Power Density and Performance Using 3D Packaging

Emerging technologies for 3D packaging at the printed circuit board scale

Presented by
PSMA Packaging Committee
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Tyndall National Institute

Power Sources Manufacturers Association
The Multinational Power Electronics Association

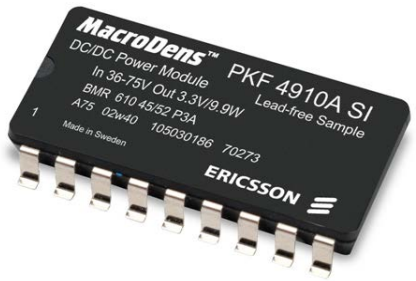
Overview of *3D Power Packaging* Phase 1 Report

- PSMA contracted Tyndall National Institute to conduct a study of trends in 3D packaging for power
- This paper study led to the Phase 1 report recently published
- The study considered integration of components into:
  - Chip scale packages using stacking, transposers, integration, etc.
  - ***PCB mountable module type packages***
  - High Power Modules > 1 kW
- Additive Manufacturing, including 3D printing, is covered in the report

This presentation focuses on the findings from the study for 3D power packaging at the PCB scale

3D Power Packaging at the PCB Scale

- There are few examples of 3D packaging in commercially available power modules
  - This is expected to change as wide band gap semiconductors are adopted
  - Wide band gap devices offer the promise of higher density and efficiency, however, current packaging technology limit that promise

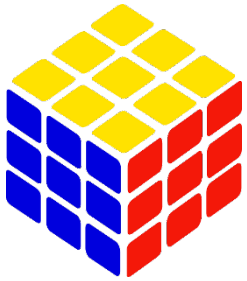


Molded,10W, 1991

Molded 2014, up to 1.2 kW

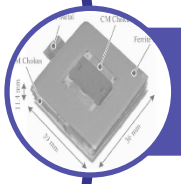
- Advances in packaging technology are recognized as key to leveraging the switching speed of GaN and SiC

Areas of Technology Innovation



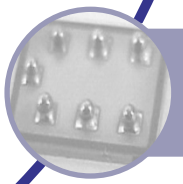
Embedding of active or passive components within Printed Circuit Boards

Embedding magnetics with Printed Circuit Boards



Integrated Filters

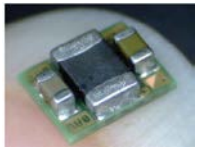
Enhanced Cooling

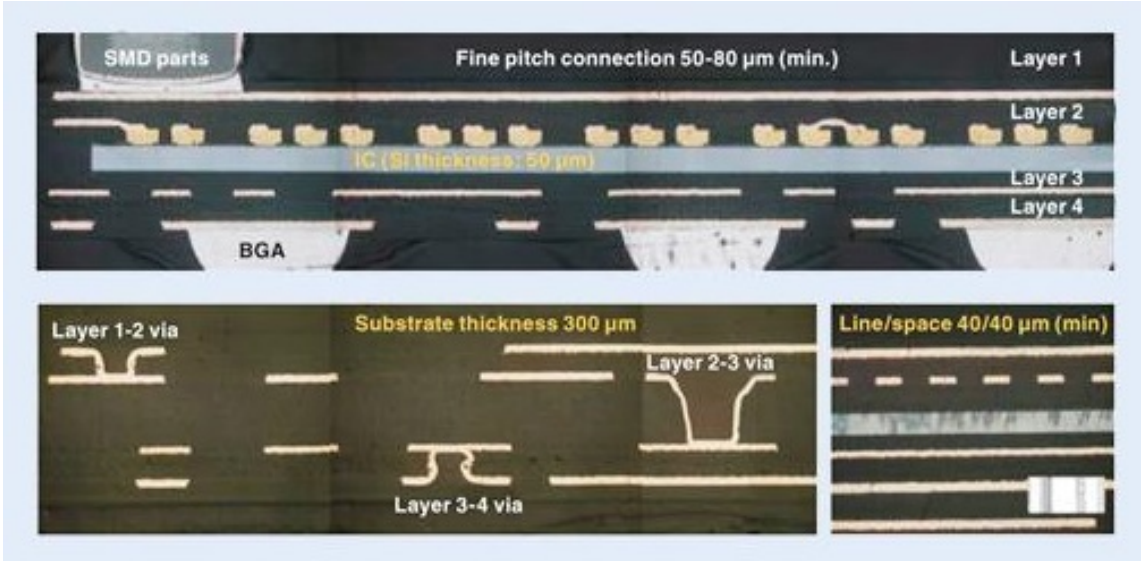


Integrated Power Electronic Module (IPEM) efforts at CPES

Embedded Active Components

- Significant progress has been made through two EU Framework Programmes, “HIDING DIES” [FP6] and “HERMES” [FP7]
  - HIDING DIES developed the technology for embedding components
  - HERMES focused on commercialization of the technology
- TI’s MicroSIP is the 1st commercial dc-dc produced with HERMES ‘face down approach’
  - ROHM/TDK created a 2nd source using SESUB process

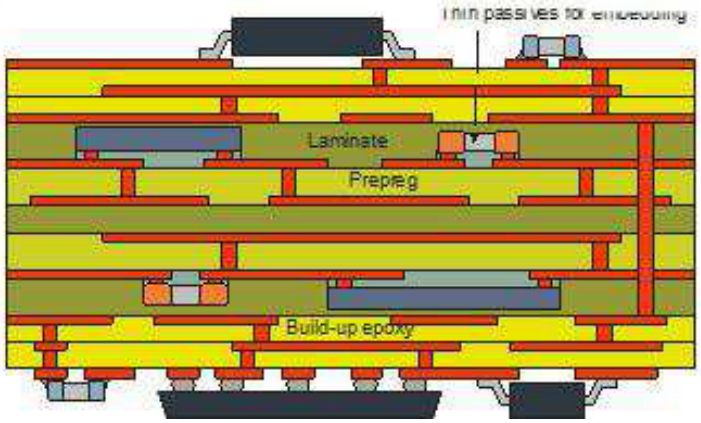




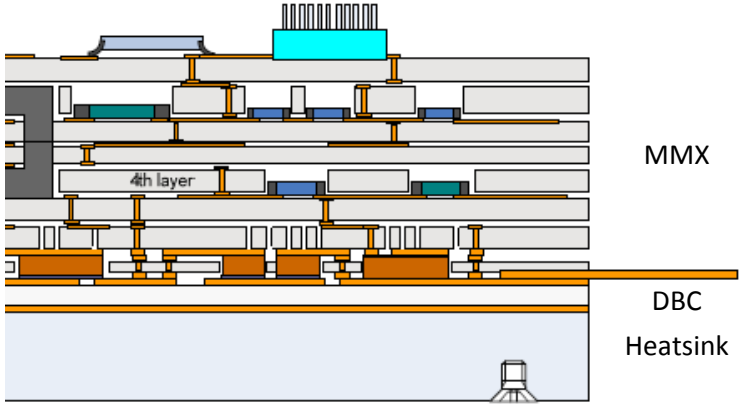
Cross section of "SEmiconductor embedded in SUBstrate" (SESUB)[1,2]

Embedded Active Components

- Example of HERMES face-down technology with two embedded core FR-4 PCBs, Prepreg layers, and external components[3]



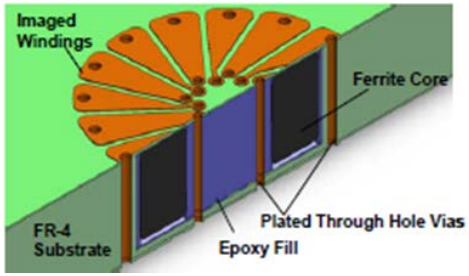
- Conceptual view of Crane Aerospace & Electronics embedded components in fusion bonded Multi-Mix® assembly; fusion bonding eliminates Prepreg layers

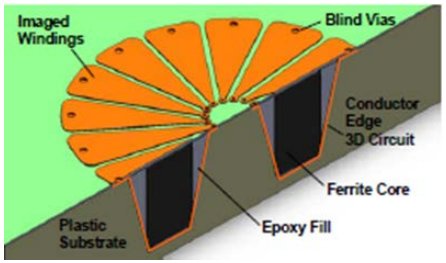


- Other embedding technologies available in the industry
  - Nanium's embedded wafer level package (eWLP)
  - Integrated Module Board (IMB) from Imbera
  - Amkor's Embedded Die/Passives in Substrate
  - SiPLIT from Siemens
  - DrBlade from Infineon
  - i2 Board®, p2 Pack® from Schweizer

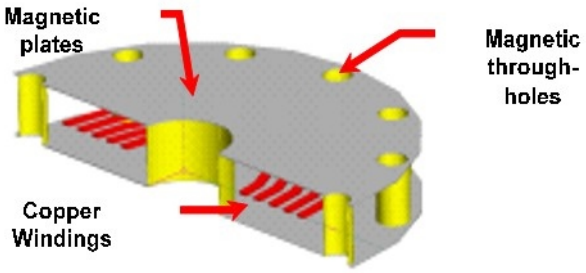
Embedded Magnetics

Two technologies for embedding magnetics[4,5] are Plated Through Hole (PTH) and Blind Via (BV) as shown in the following figures:



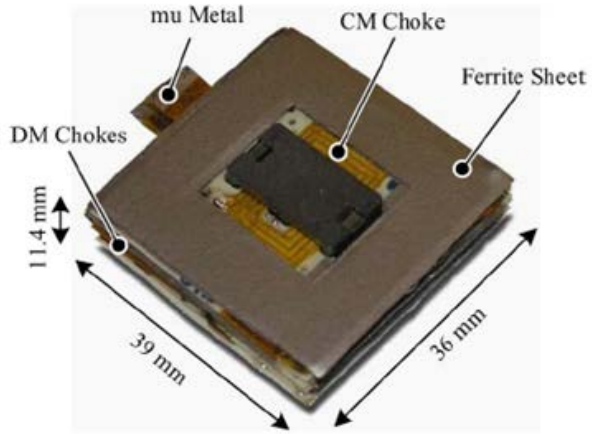


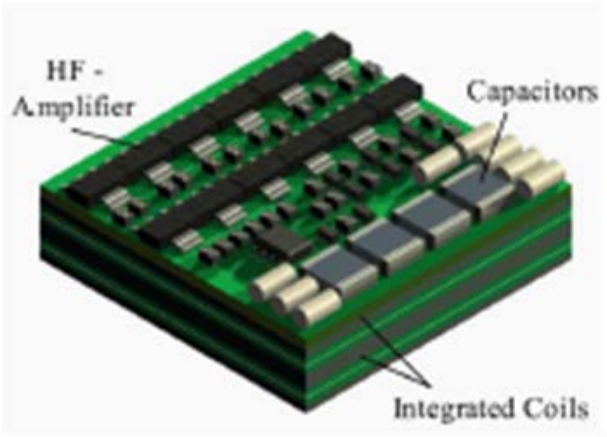
An approach[6] developed by Tyndall uses plated thin film magnetic cores and thin film magnetic materials in through vias



Integrated Filters

- Researchers at the Power Electronics Systems Laboratory at ETH Zurich have proposed 3D integrated passive and active EMI filters[7]

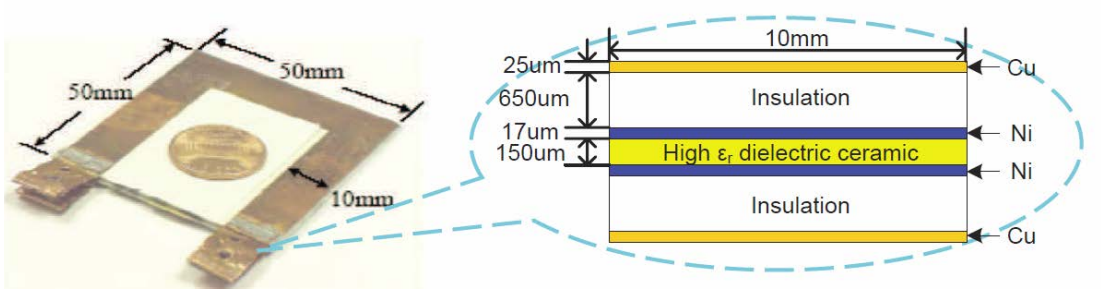




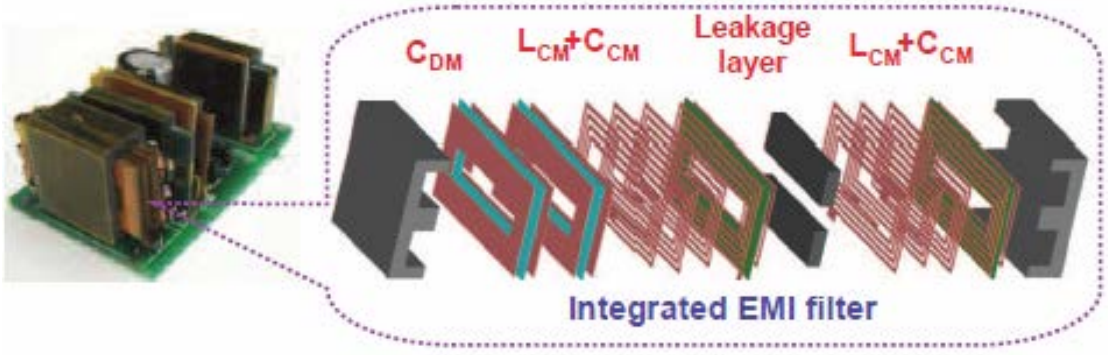
- The passive filter (left) achieved a 24% reduction compared to the discrete solution
- The combination of active and passive solutions (right) achieved a 40% reduction

Integrated Filters

- Researchers at CPES have also reported on benefits of integrated EMI filters

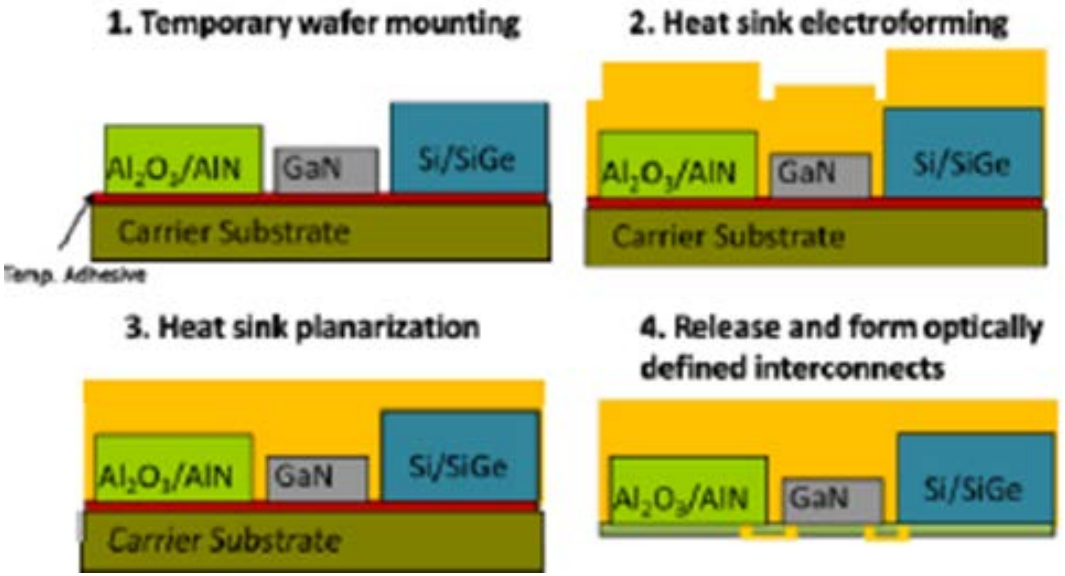


- The planar differential-mode filter above was originally proposed in 2002[8]
- An integrated CM and DM filter (below) was proposed for an electronic ballast application[9]



Enhanced Cooling

A process developed for a mixed technology RF amplifier called an Integrated Thermal Array Plate (ITAP) shows promise for power electronics application[10]



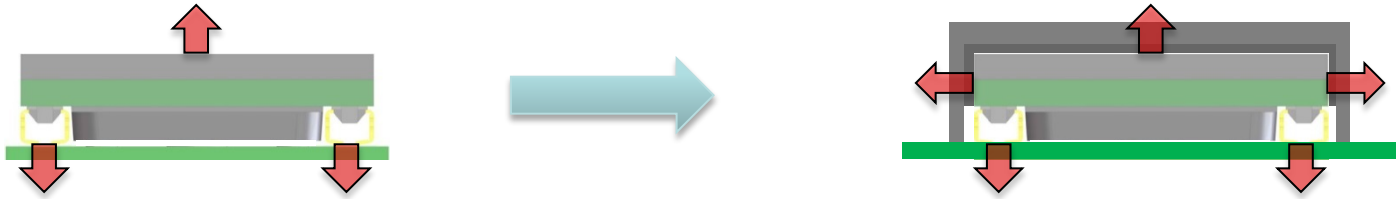
In this process ICs, passives, and semiconductor components are held on a temporary carrier and a metal heatsink is electroformed around them

Overmolded Modules

An overmolded PWB based power module was previewed by Vicor at the APEC 2013 plenary

- A 380 V - 48 V unregulated bus converter released in Jan of 2014 is rated at:
  - 1.2 kW
  - 98% efficiency
  - 1820 W/in^3
- Additional products reported for Q2 2014 release claimed to demonstrate up to 3 kW/in^3

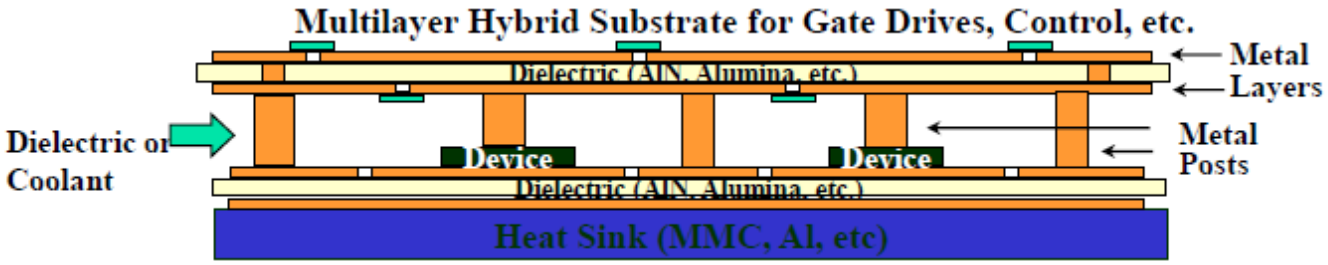
The overmolded packaging approach also provides 3D cooling benefits[11]



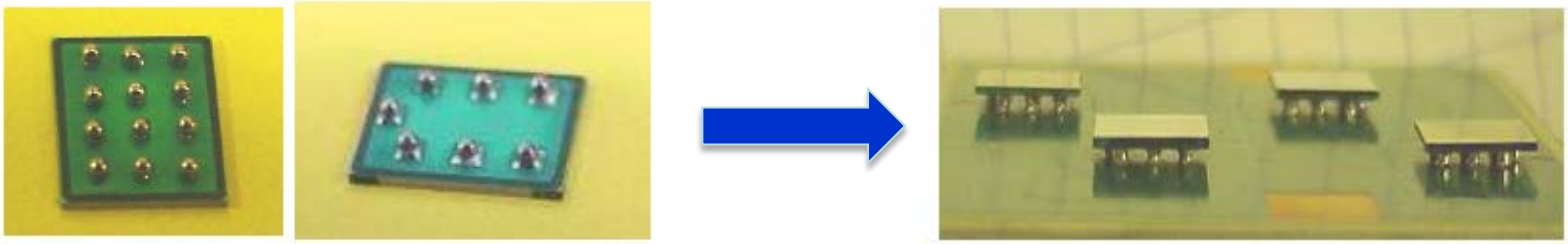
3D Power Packaging at CPES

- Research at CPES has explored 3D, non-wirebond, packaging over the last decade as part of its Integrated Power Electronics Modules (IPEM) thrust
- Calata[12] et. al. presented four CPES 3-D power packaging approaches

1. Metal post interconnected parallel plate structure (MPIPPS)



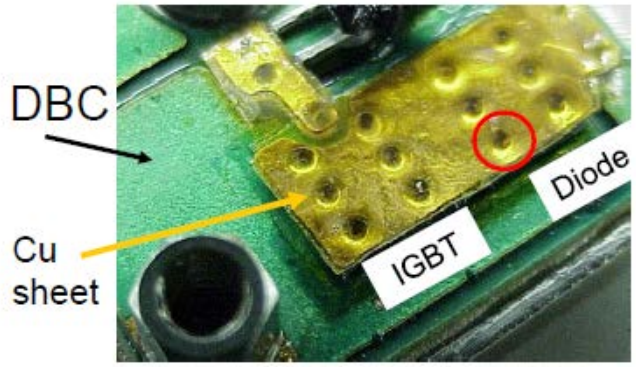
2. Stacked solder bumping



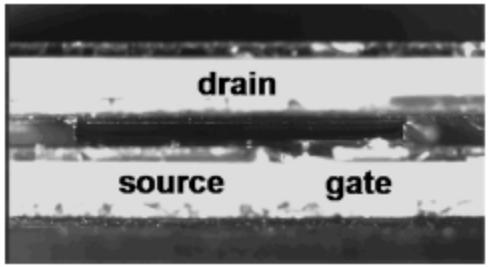
3D Power Packaging at CPES

- 3D Power Packaging Approaches from CPES (continued)

3. Dimple Array Interconnect (DAI)

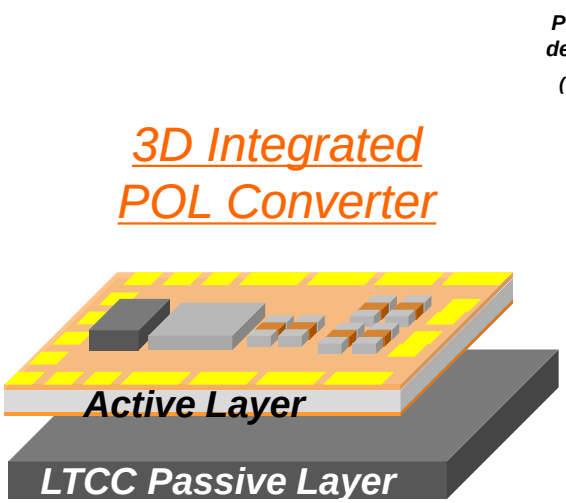


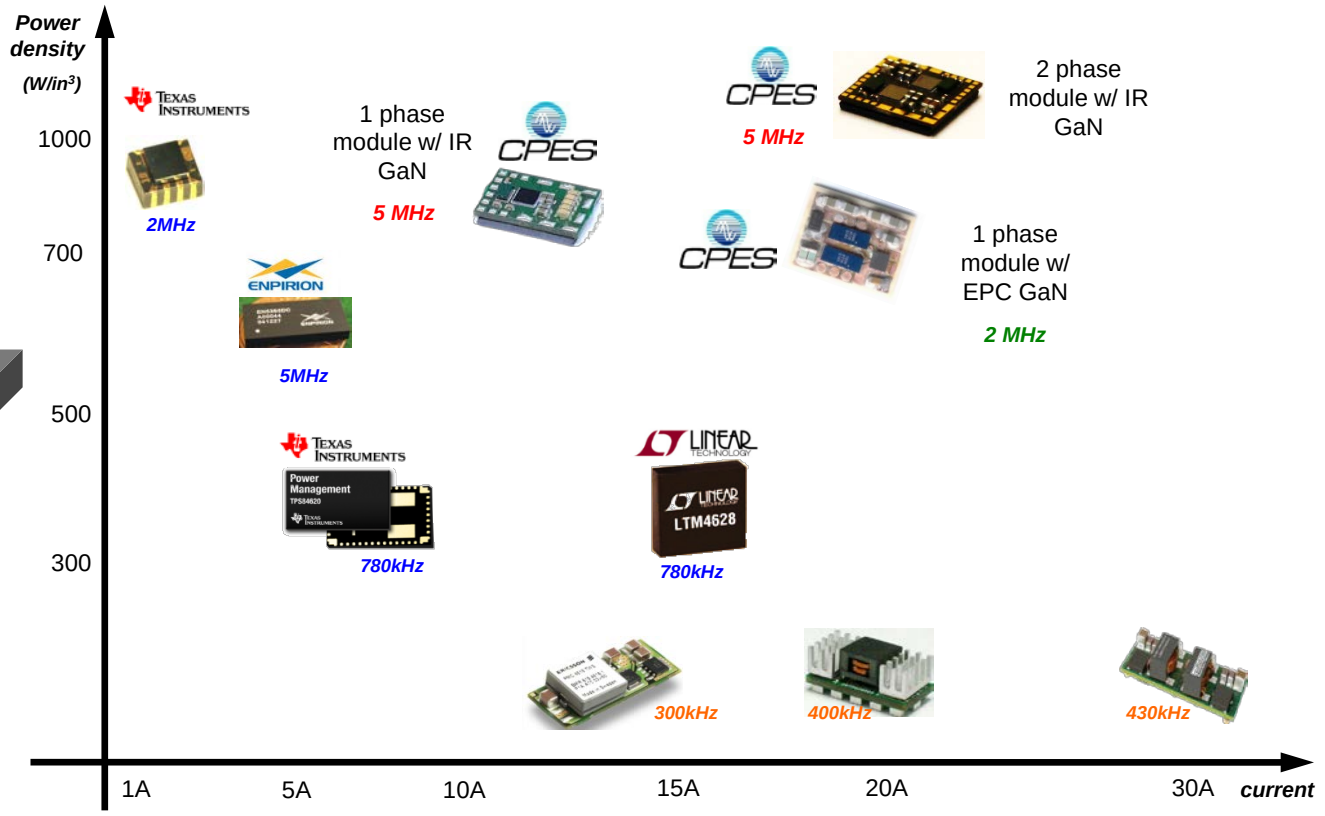
2. Double side cooled direct solder interconnect



3D Power Packaging at CPES

- Development progress on 3D POLs at CPES was presented in the 2013 APEC Industry Session IS 1.5, 3D Packaging for Power[13]





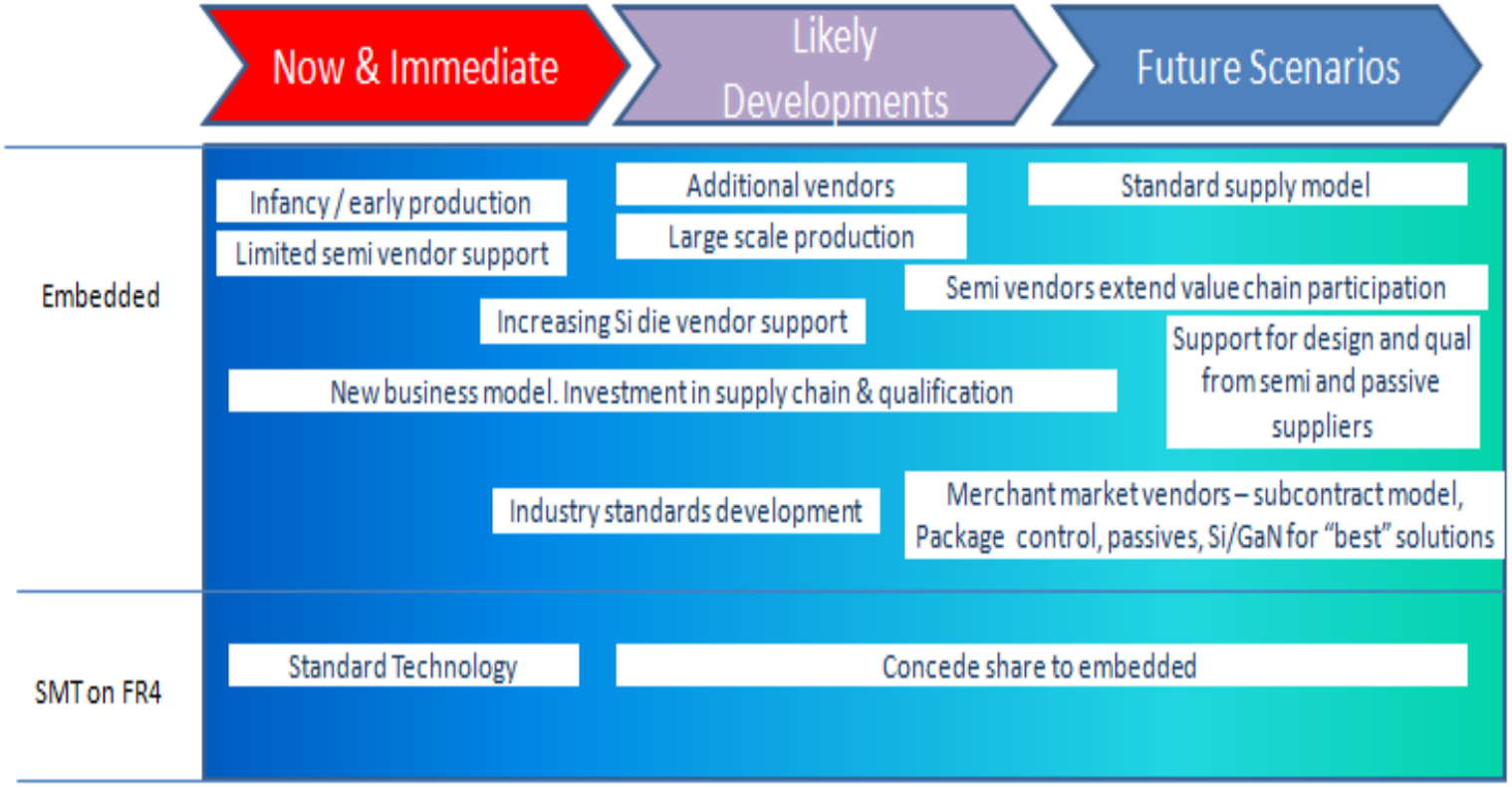
Disruptive Technologies and Events

Disruptive technologies have emerged that are expected to drive 3D packaging technologies at the PCB scale in the near future

- **Wide bandgap devices:** Commercial availability of SiC and GaN
  - Benefits are limited by parasitics with current packaging technologies
  - Embedded components in FR4 are a possible solution
- **High power boards:** 3 kW - 5 kW per board to meet data center demand by 2020
- **Cooling:** Increased use of heat pipes; phase change or liquid cooling to select high power components and residual air elsewhere

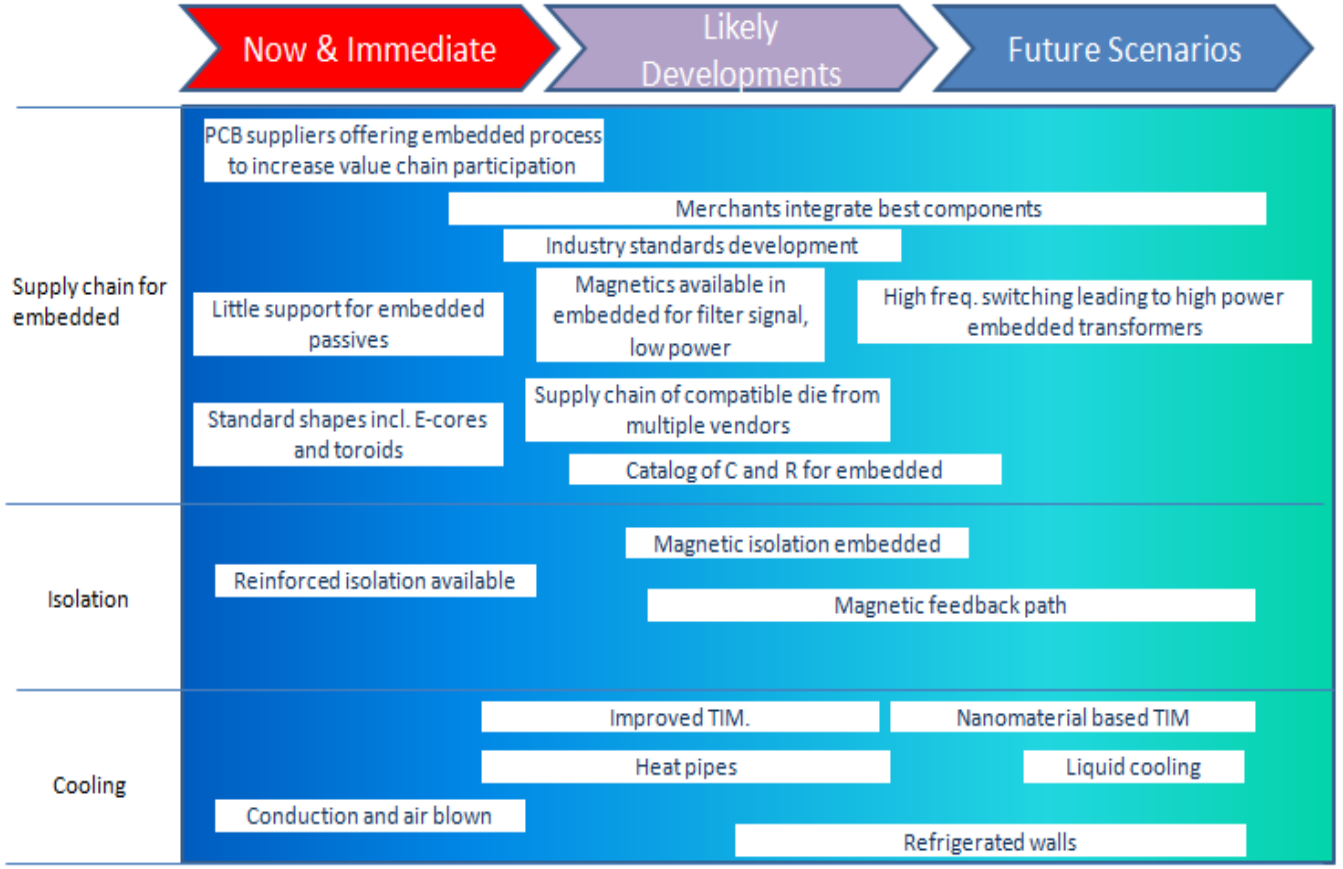
Water board (Schweizer)

PCB Scale 3D Packaging Roadmap (1/2)



Power packaging at the PCB scale is forecast to transition from SMT on FR4 to embedded technology

PCB Scale 3D Packaging Roadmap (2/2)



- **Supply chain demand for compatible passives and magnetics**
- **Thermal interface and cooling technology will become more integrated**

Conclusions

- **Emergence of wide bandgap semiconductors is generating technology “pull” from innovations in microelectronics packaging**
- **Embedding technologies currently gaining a foothold at the chip scale are expected to expand strongly into PCB scale**
- **Overmolding is likely to continue as a technology used for enhancement of handling and thermal performance**

Next Step: Phase II

- Proposed Phase II intended to provide in depth study of Phase I topic(s)
- Phase II topic(s) determined by industry feedback
- Timeframe – May 2014 to March 2015
- Target completion date for Phase 2 report – APEC 2015
- Target APEC 2015 for presenting final report in Seminar/Workshop and Industry Session

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Thank You

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