Thermal Management Challenges and Opportunities for Heterogeneous Integration

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Madhu Iyengar, Principal Engineer, Google
Chair, IEEE EPS Heterogeneous Integration Roadmap,
Thermal Technical Working Group
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- Heterogeneous Integration has witnessed a remarkable growth of use cases in the last few years (Cloud, AI, Mobile, Autonomous Vehicles, Wearables, HEalth, IoT, Defense, Space).
- Thermal management has become a key performance enabler in this space.
- Complex configurations (stacked dies, adjacent placement, height mismatches, varying temperature requirements), rising performance requirements, and high power densities, all create opportunities for innovation at multiple length scales.
- Industry timing is ripe for aggressive exploration of integration of high performance cooling into our semiconductor manufacturing processes and supply chain.
- Power delivery and management technology plays a key role in enabling high performance HI systems in conjunction with thermal (and other) advances.
- Thermal - Power co-design will be an important theme going forward. They share several key challenges including a dramatic rise in device power and power density.
Hardware Embodiments of AI Systems
Air and Liquid Cooled

AI Design Forum at SEMICON West 2019, Cliff Young (Google Research) gave a presentation on “Codesign for Google TPUs – How can Materials Help?” Shown in Figure 18, from the left, are pictures of three generations of the Tensor Processor Unit (TPU): TPU1, TPU2 and TPU3.

Ref: 2019 Heterogenous Roadmap, Overview  
Three Generations of Google TPUs, Source: Cliff Young, Google Research
Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics. In this definition, components should be taken to mean any unit, whether individual die, MEMS device, passive component and assembled package or sub-system, that are integrated into a single package. The operating characteristics should also be taken in its broadest meaning including characteristics such as system-level performance and cost of ownership. Source: ITRS Assembly & Packaging Chapter.
IEEE EPS Heterogeneous Integration Roadmap (HIR)

All future applications will be further transformed through the power of AI, VR, and AR.

Ref: 2019 Heterogenous Roadmap, Overview (link)
Six application spaces undergirded by AI, VR, and AR, Source: ASE
IEEE HIR Thermal Chapter

Thermal TWG will consider three areas:

(a) Die level.
(b) Package integration/SIP/module Level.
(c) System Level (limited to board level).

Thermal TWG will focus on articulating the following in quantitative and qualitative terms:

(i) Canonical problems with thermal challenges;
(ii) Cooling limits for known solutions;
(iii) Advanced concepts and research.

Year 1 (2018-2019)
- Thermal effort kicked off in March 2018.
- ~30 industry & university experts
- Final Chapter completed in June 2019.
- Published on EPS Website

Year 2 (2019-2020)
- Feedback received on 2019 edition.
- Opportunistically add new content.
- Power density, HBMs

Year 3 (2020-2021)
- ~50 industry & university contributors
- Ongoing discussions to expand scope of technical content
- SEMI Silicon Microchannels initiative
Example of chip power density trends

Source: Ravi Mahajan, Weihua Tang, Intel, Materials to be published in 2020 HIR Thermal Chapter

Thermal Technologies must cover a Hotspot Density Envelope in the (2x-4x) range with an understanding of upside capability for both 2D and 3D Architectures
● Chip stacking requires heat to be removed through multiple conduction interfaces

● Memory stacks are growing with increasing demand for higher capacity

● Hot spots and proximity to high power ASICs exacerbate the thermal challenges

● Supportable power limits can limit device performance
1. 2D chip with stacked memory on a silicon/glass interposer

2. 3D stacked die with conduction interfaces

3. 3D stacked die with embedded liquid cooling

4. Optics/photonics based heterogeneous package

5. Harsh environment (military, aerospace, automobile)

6. Mobile application chipset (package on package, fan out, bridge)

7. Voltage Regulators in a heterogeneous package

Canonical Thermal Heterogeneous Integration Problems

Chapter 20, 2019 IEEE Heterogeneous Integration Roadmap (link)
1. 2D Enhanced Architecture - Thermal Challenges

Weihua Tang (Intel), Vadim Gektin (Huawei), Yogi Joshi (Georgia Tech)

- Increasing package power density;
- Increasing total package power dissipation;
- Thermal cross-talk, including the need for thermal isolation;
- Different thermal (Tj) requirements and sensitivities.
- TIM1 or TIM1.5 thermal insulance (K-mm2/W) uncertainty from increasing form factor and Si surface flatness and overall warpage impact
- Enablement of thermo-mechanical robustness (e.g. addressing temperature and CTE mismatch driven warpage)
- Interposer thermal properties (glass/Si/organic) (see Figure 3) including anisotropy.
- Interposer thermal conductivity has a strong impact on chip thermal resistance
- Glass and Si interposer performance can be made comparable, by appropriate enhancements
- Interposer heat spreading and heat removal
2. 3D Chip Stack Cooling - Conduction Interfaces

Kamal Sikka (IBM), Vadim Gektin (Huawei)
3. 3D Chip Stack Cooling - Embedded Cooling

Tim Chainer (IBM), Yogi Joshi (Georgia Tech), Vadim Gektin (Huawei)

DARPA ICECool Apps Phase 1 TDV Results
4. Thermal challenges in Photonic devices
Amr helmy (Univ. Toronto), Weihua Tang (Intel)
5. Heterogeneous Integration for Harsh Environments

Peter de Bock (GE), Sreekant Narumanchi (NREL), Craig Green (Carbice)

Notional 3D chip architecture and anticipated topology challenges

Inverter in a multi-layered board or stack-up configuration
6. Thermal challenges in Mobile platforms

Nelson and Galloway (Semitherm 2018)

Temperature contour data for the external surface of a Smartphone

Micro heat pipe in a modern smartphone
Even at 95% efficiency, a 200W VR (Voltage Regulator) will dissipate 10 Watts – mostly within the power switching devices with a small footprint inside the package.
Advanced Thermal Technologies & Research

Chapter 20, 2019 IEEE Heterogeneous Integration Roadmap (link)

[A] Thermal Interface Materials

[B] System thermal limits for HPC multi-chip modules

[C] Embedded liquid cooling of chip & chip stacks

[D] Advanced Thermal Materials for Thermal Management

[E] Thermomechanical Modeling for Heterogeneous Integration

Design Space Definition
- Geometrical description
- Material property distributions
- Interface/Boundary conditions across domains

Finite element simulation setup and data generation (Electrical, thermal and mechanical models)

Field output preparation \( \rightarrow \) Training and Test Split

DAE training using an ML library

Validation and Deployment into design/reliability simulation tools

A 3D chip stack using advanced materials in the conduction heat flow path.
SEMI Proposal: Pre-competitive Silicon Microchannels Study

- SEMI has been engaged to develop a Strategic Innovation Platform on semiconductor manufacturing assessment of silicon microchannels on the back side of high-performance ASICs.
- Motivating factor is the high cooling load created by such devices used in data centers.
- While silicon microchannels have been investigated in laboratory settings, they have not been implemented in commercial settings.
- Goal of this program is to bring together companies involved in materials and equipment (particularly lithography and etch processes), as well as manufacturers (foundry, OSAT), and system integrators (data center) to establish baseline manufacturing technologies for silicon microchannels, identify and assess solutions for cost-effective implementation, identify supply chain and manufacturing readiness, and address identified gaps/show-stoppers.
The timing for our industry is ripe for aggressive exploration of the integration of high performance cooling into our semiconductor manufacturing processes and supply chain.
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Call to Action

- The slowing down of Moore’s Law and the End of Dennard Scaling means that device powers and localized hotspot power densities have been rising and this trend is expected to continue.

- Thermal management and power delivery/management are much more intrinsically intertwined in how joint advances will move the needle for device and system performance to fulfill market and societal demands.

- Advances will take the form of device to system holistic design and multi-discipline co-design with an emphasis on structures close to the “chip”.

- Over the last 3 years, the IEEE EPS Heterogeneous Integration Roadmap Thermal Management Technical Working Group has attracted ~50 industry/university experts to contribute to this space, and offers a unique opportunity to unite a vast ecosystem, including Power Delivery expertise and thermal-power co-design.