Efficient Grid-to-Battery Power Electronics for EVs

Kraig J. Olejniczak, Ph.D., P.E.

Zach Cole, Jonathan Hayes, Dan Martin, Chad O'Neal, Ty McNutt, Jeff Casady, Dave Grider, Edward VanBrunt and John Palmour

Andrew Lemmon and M. Olimmah, University of Alabama

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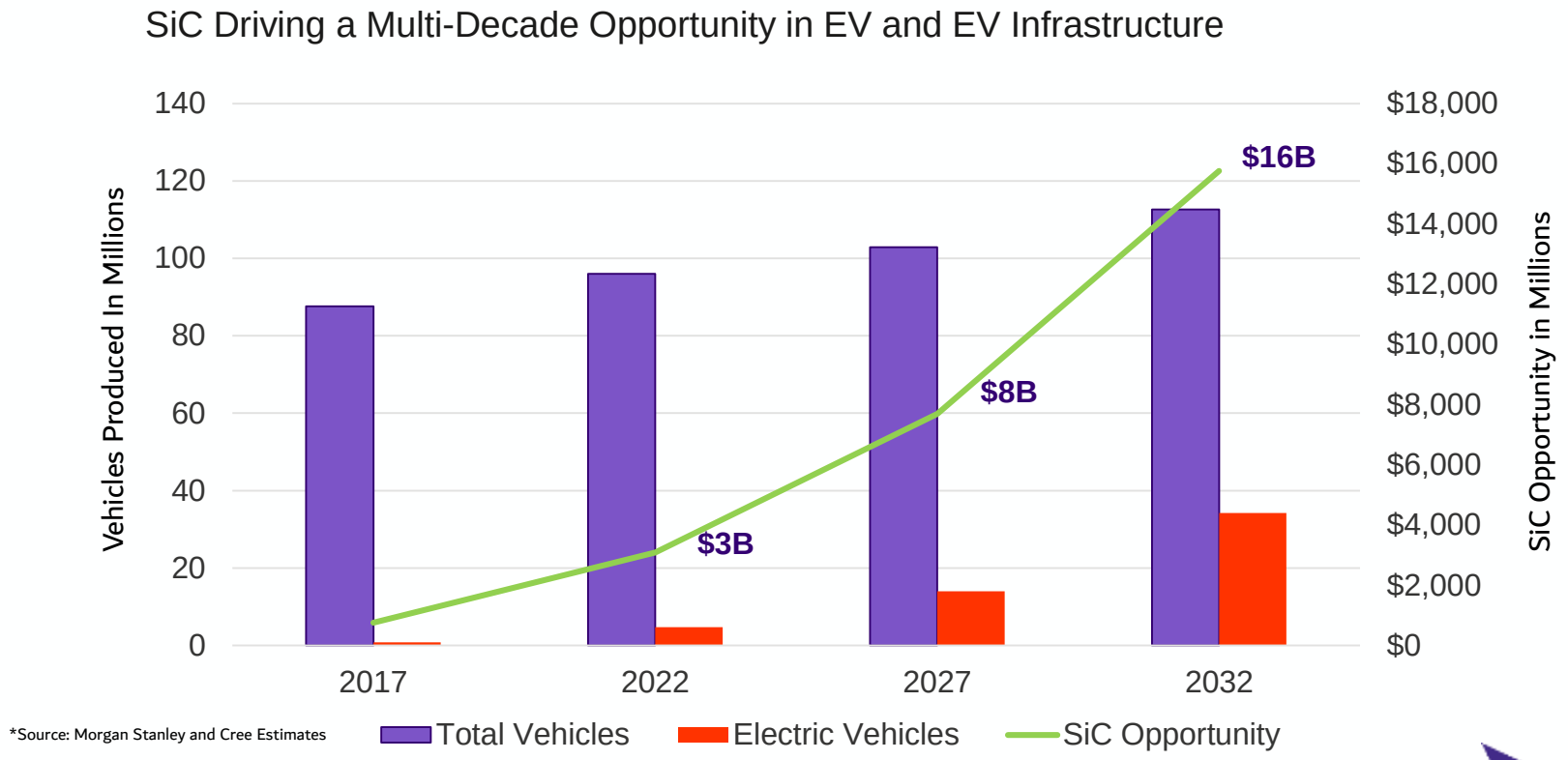
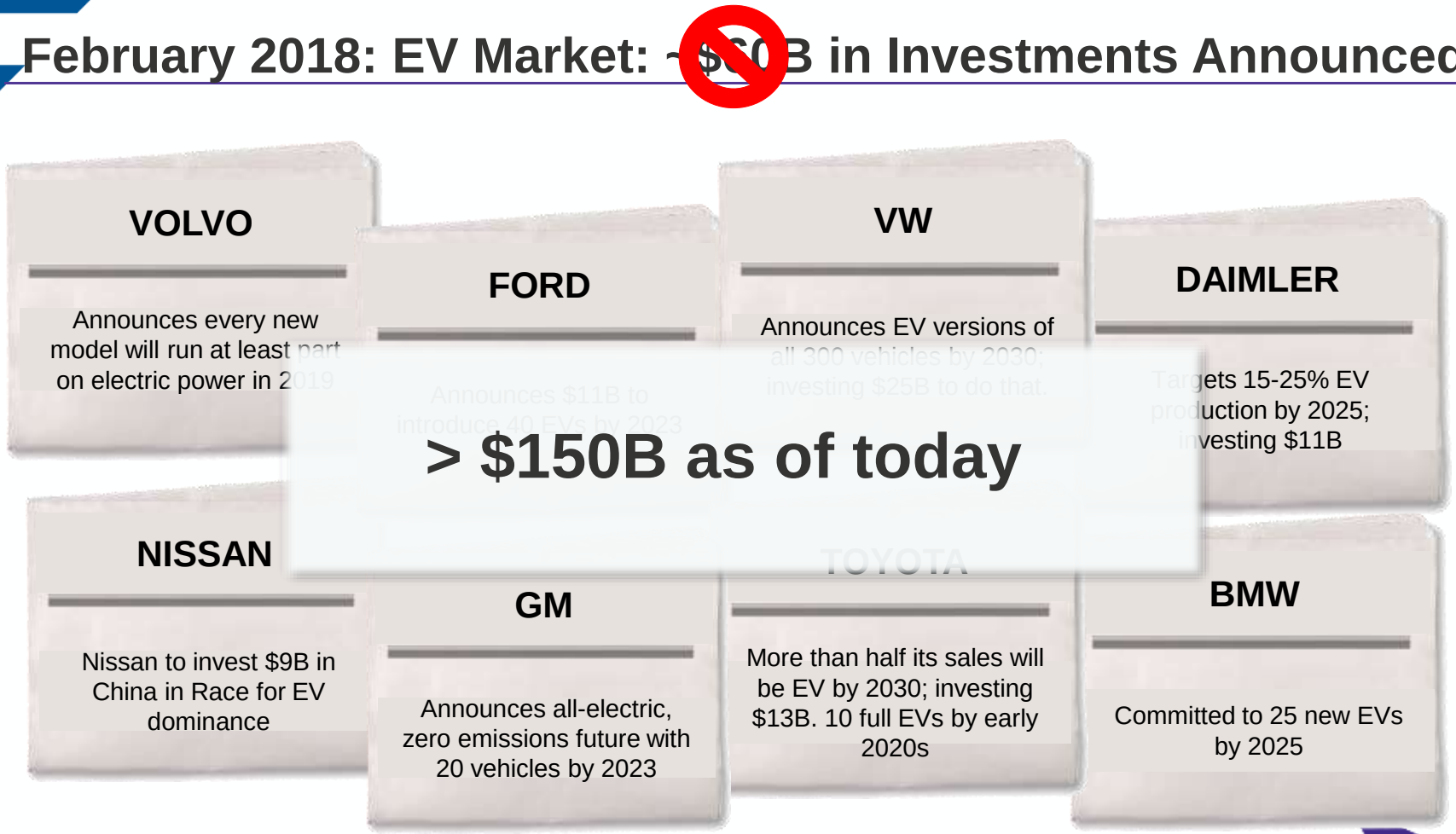
Even Modest EV Adoption Drives Significant Opportunity



February 2018: EV Market: ~$60B in Investments Announced

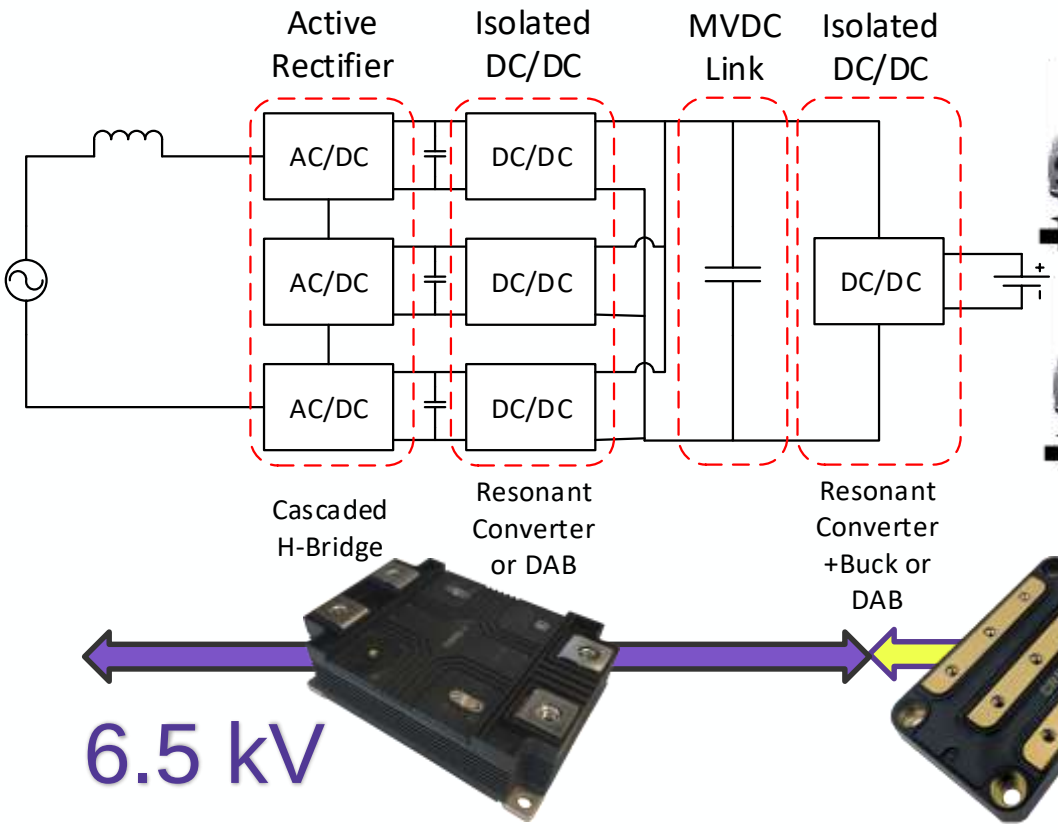


More Power, Delivered More Efficiently

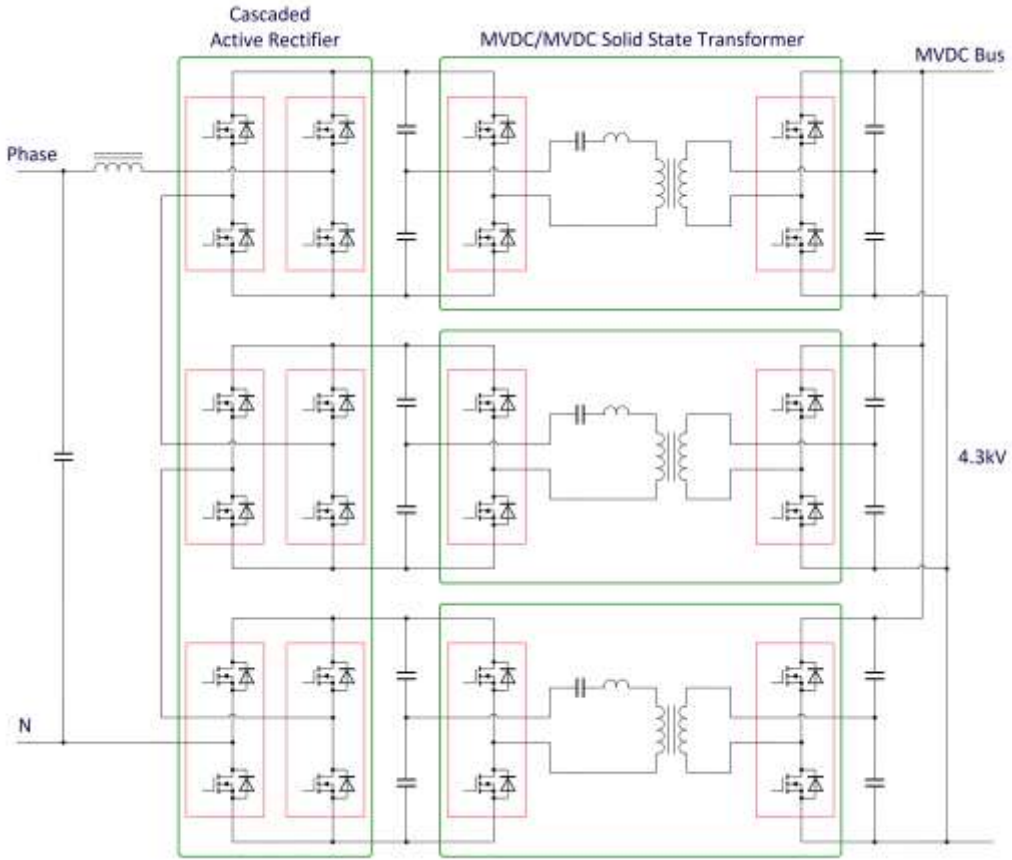
DESIGN GOAL: To develop a high-performing and standardized packaging solution for Wolfspeed's 3.3 kV and 6.5 kV SiC MOSFETs to enable transformative improvements in efficiency, reliability, and life-cycle costs in medium-voltage applications where the Si IGBT is the incumbent switch technology.

ARPA-E CIRCUITS: 1 MW Fast Charger Example

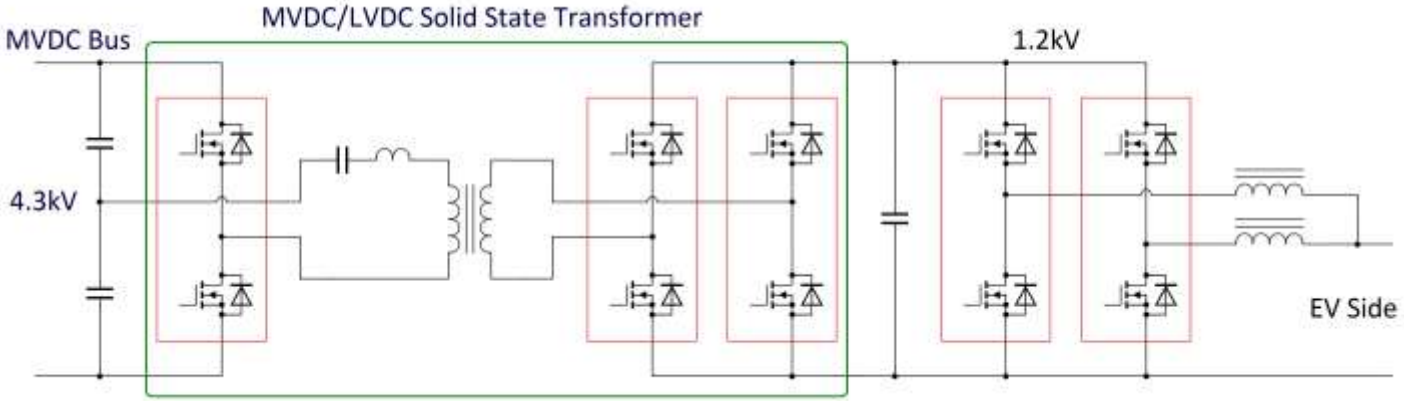
U.S. Department of Energy's ARPA-E ≡ Advanced Research Project Agency-Energy, arpa-e.energy.gov



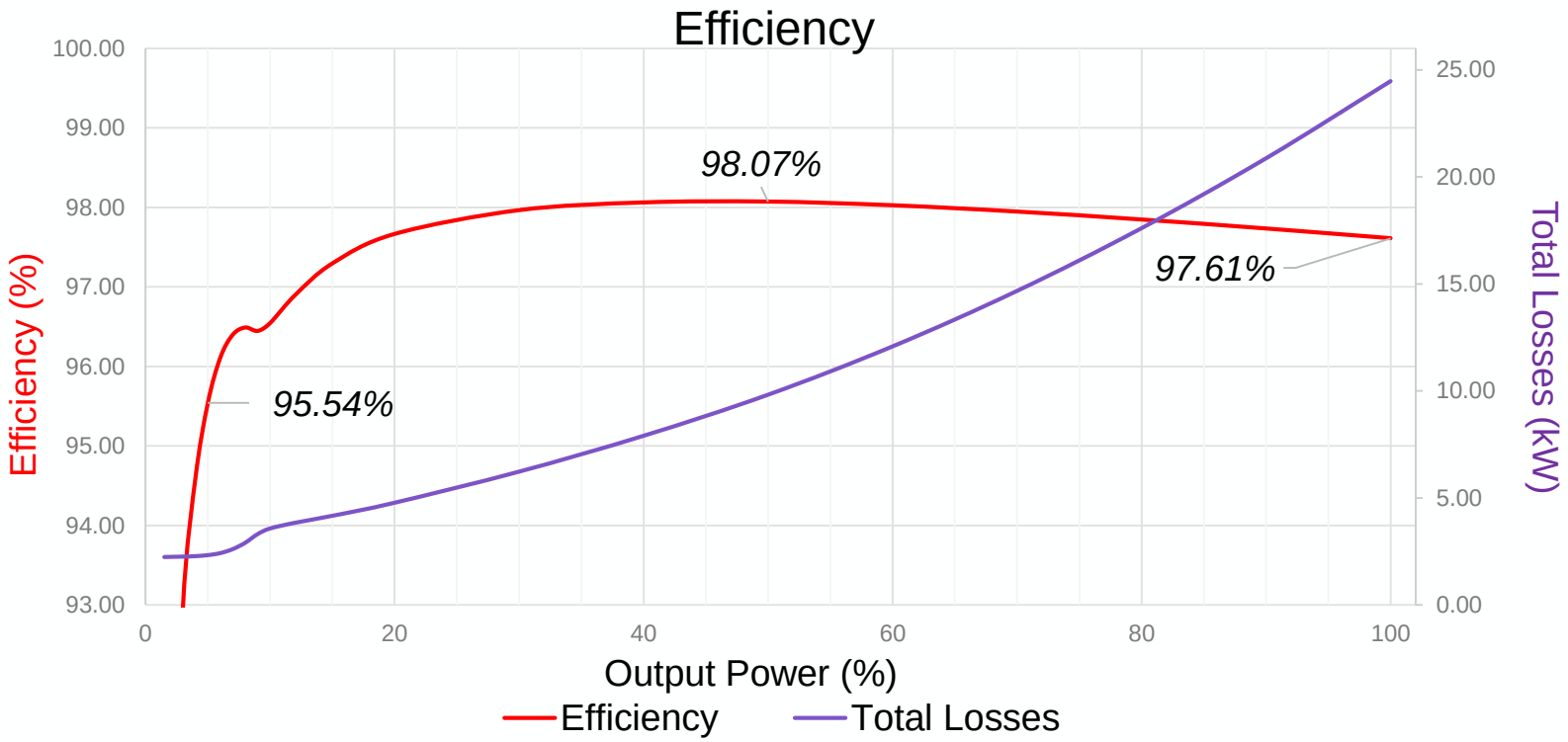
Technically-Innovative System – Grid-to-MVDC Bus



System Topology – MVDC Bus-to-EV

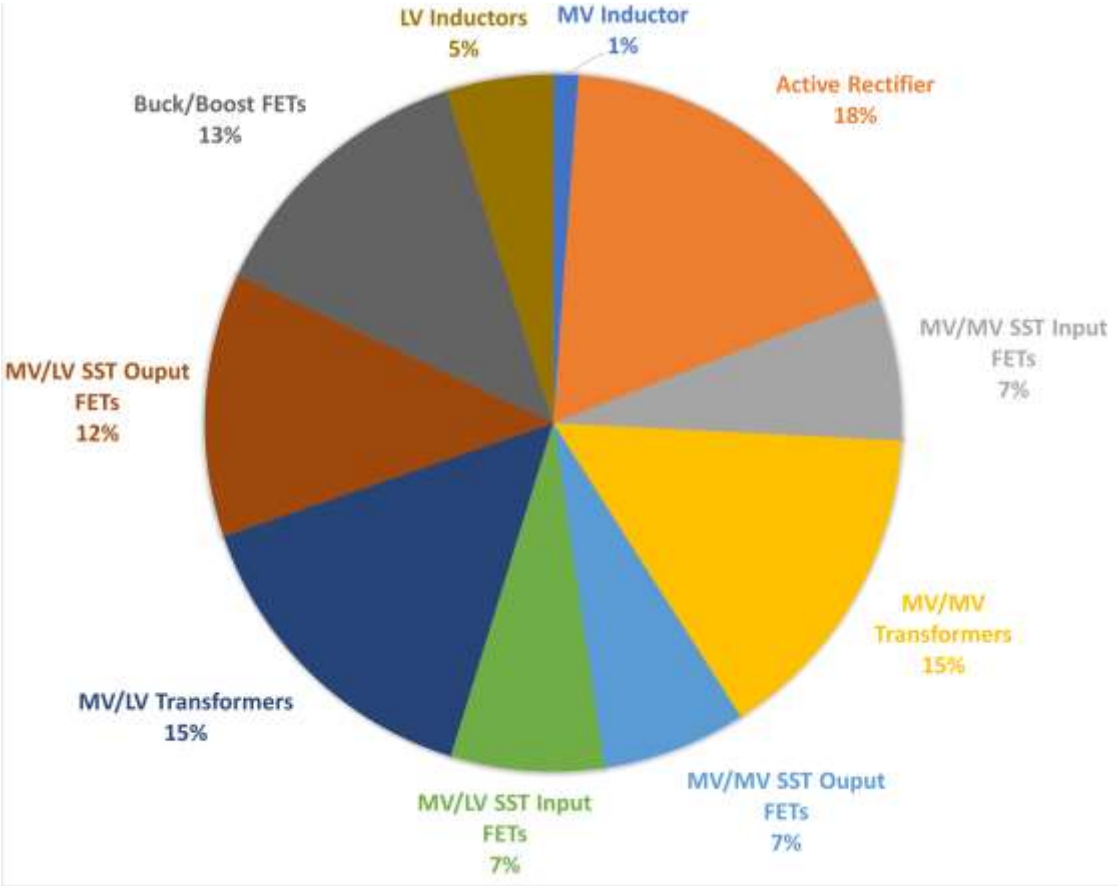


Simulated System Loss Calculation



Simulated Loss Distribution

- The active rectifier (input) and the Buck/Boost converter (output) are hard-switched and contribute to 31% of system losses
- The resonant converters present purely conduction losses and contribute 33% of system losses
- The remaining 36% of losses from the magnetics in the system
- The system losses are well balanced and don’t present any major cooling concerns



More Power, Delivered More Efficiently

Maximize the module current rating…maximize the area of the switch position…maximize # of die per SP…$f(A_{die})$…this motivates one to consider a 2D+ packaging approach

Medium Voltage SiC Power MOSFET JEDEC Qualification

- Completed on PowerAmerica-BP1 / BP2 – Fabrication & JEDEC Qualification of New Design 3.3 kV / 50 mΩ SiC MOSFETs and 10 kV / 300 mΩ SiC MOSFETs on 100 mm 4HN-SiC Wafers
  - High Temperature Reverse Bias (HTRB)
  - High Temperature Gate Bias (HTGB)
  - Time Dependent Dielectric Breakdown (TDDB)
  - Thermal Shock (TS)
  - Body Diode Operating Lifetime (BDOL)
  - Electrostatic Discharge (ESD)
  - High Humidity High Temperature Reverse Bias (H3TRB)
- Underway on PowerAmerica-BP3/4 – Fabrication & JEDEC Qualification of 6.5 kV / 100mΩ SiC MOSFETs on 150 mm 4HN-SiC Wafers
  - High Temperature Reverse Bias (HTRB)
  - High Temp Gate Bias (HTGB)
  - Time Dependent Dielectric Breakdown (TDDB)

4.9 mm × 7.7 mm

Gen3 3.3 kV / 50 mΩ SiC MOSFET

8.1 mm × 8.1 mm

Gen3 10 kV / 300 mΩ SiC MOSFET

8.1 mm × 8.1 mm

Gen3 6.5 kV / 100 mΩ SiC MOSFET

XHV-7 Module and Companion Gate Driver

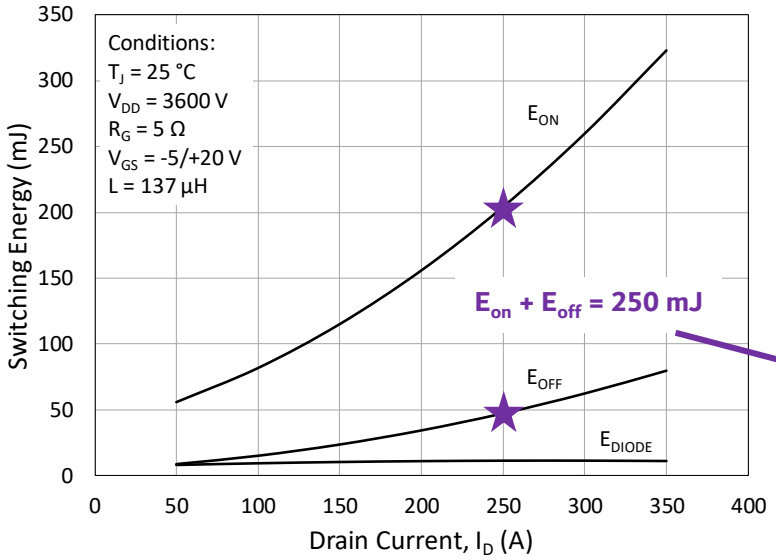
- 3.3 kV & 6.5 kV Gen 3 SiC half-bridge power module
- Industry standard XHP™ 3 package
- Designed to simplify external bussing for easy paralleling of modules
- Low 6.5 kV FET R_{jc} of 0.039 °C/W with a maximum power dissipation of 3816 W per switch position (T_C = 25 °C, $T_{J,max}$ = 175 °C)
- Direct mount, form-factor fitting half-bridge companion gate driver
- Onboard, hardware configurable protections and gate drive voltages
- High output current optimized for 6.5 kV SiC Gen 3 MOSFETs

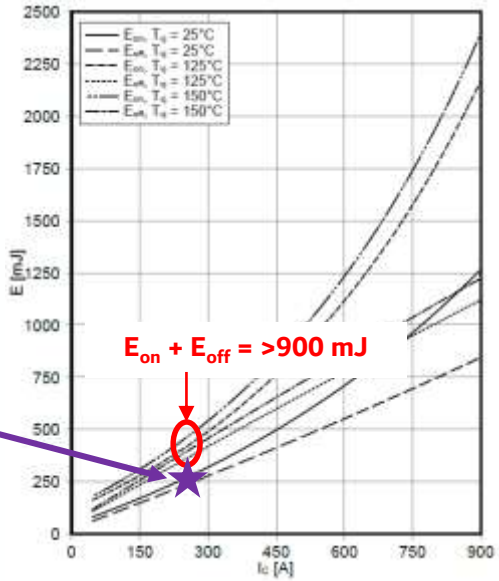
Footprint =
100 × 140 × 40 mm

Switching Energy Comparison to 3.3 kV Si IGBT

Wolfspeed 6.5 kV all-SiC XHV-7 MOSFET Loss
V_{GS} = +20 V / -5 V, R_G = 5 Ω, V_{DS} = 3600 V

Infineon 3.3 kV FF450R33T3E3 (XHP 3) – Si IGBT Loss
V_{GE} = ±15 V, R_{Gon} = 0.7 Ω, R_{Goff} = 3.3 Ω, V_{CE} = 1800 V

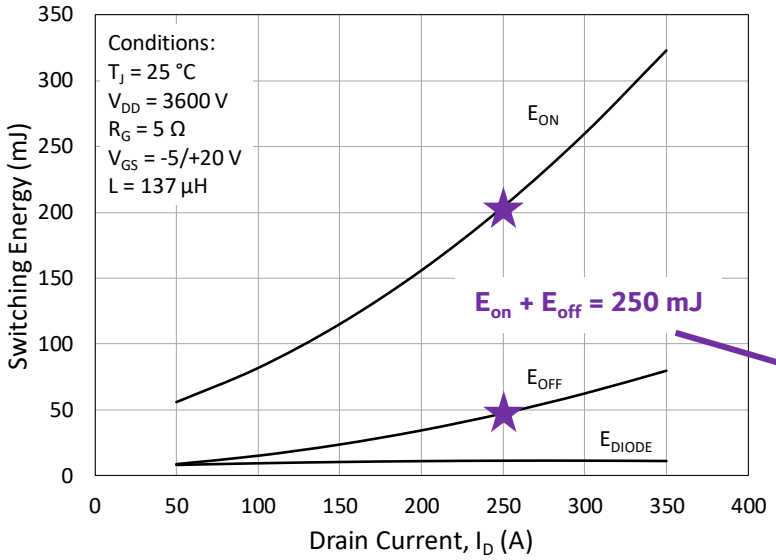




Switching Energy Comparison to 6.5 kV IGBT

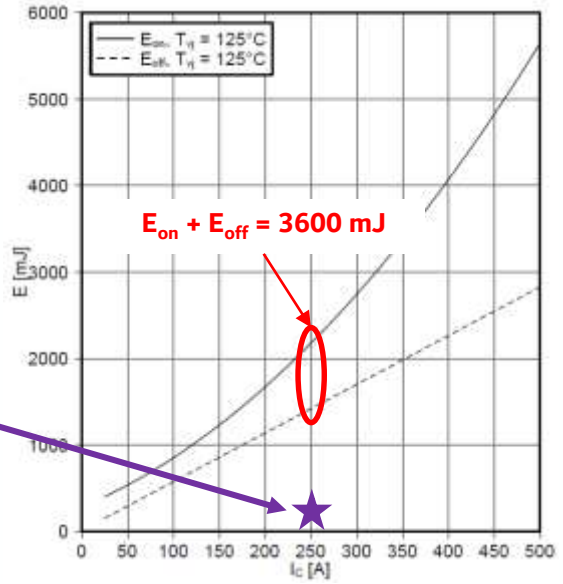
Wolfspeed 6.5 kV all-SiC XHV-7 - MOSFET Loss

V_{GS} = +20 V / -5 V, R_G = 5 Ω, V_{DD} = 3600 V



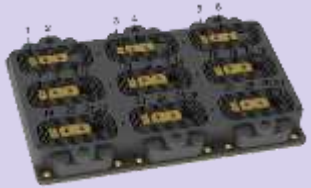
Infineon 6.5 kV FZ250R65KE3 – Si IGBT Loss

V_{GE} = ±15 V, R_{Gon} = 3 Ω, R_{Goff} = 20.4 Ω, V_{CE} = 3600 V



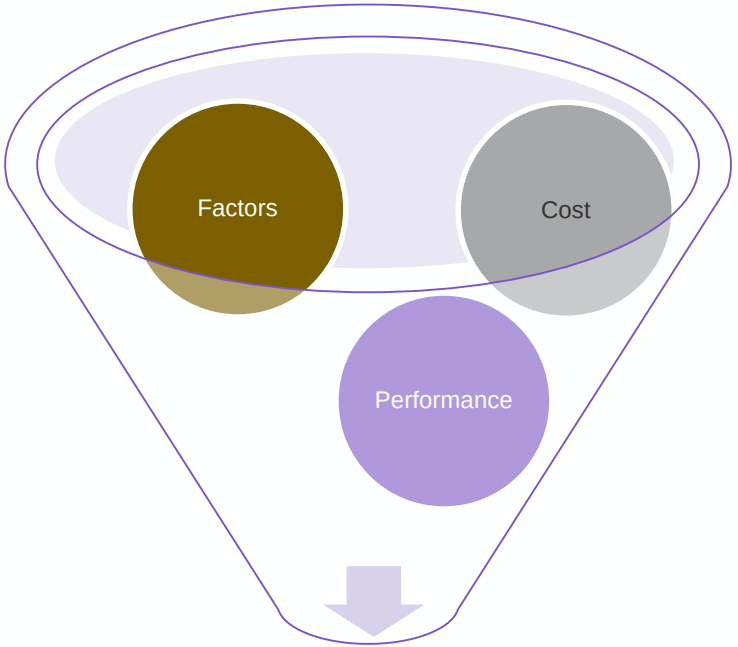
3-D Packaging Challenges for MV All-SiC Power Modules

1. Application-specific
2. Material Properties
3. Ceramic Materials for Use in Power Substrates
5. Ceramic Substrate Needs
6. Electrical Challenges
7. Thermal Challenges
8. Mechanical Challenges
9. Environmental Challenges
   – EN 45545-1, smoke and flammability

Module	Photo (NTS)	Configurations	No. Die / SP	Applications
XHV-6 125 × 195 × 24 mm		Half-bridge Common Source Common Cathode-Drain	• 10 kV: 3 – 18 • 6.5 kV: 3 - 18	• MV converters • Motor drives • High-speed motor drives • Traction drives • UPS systems • Wind • Solar • Energy storage • Smart grid, SSTs • FACTS controllers
XHV-7 100 × 140 × 40 mm		Half-bridge	• 6.5 kV: 1 – 12 • 3.3 kV: 1 - 16	
XHV-9 65 × 125 × 24 mm		Half-bridge Common Source Common Cathode-Drain	• 10 kV: 1 – 6 • 6.5 kV: 1 – 6 • 3.3 kV: 1 - 12	

Application of Interest: MV Power Modules

- Electronic packaging technology has not enjoyed anywhere near the performance advancement of power semiconductor device technology (i.e., wide bandgap) over the past 10 years
- Power electronics system performance, using wide bandgap semiconductors, has become increasingly **limited by legacy silicon (Si) packages**
- **Factors** that relate cost and performance to packaging technology
  - Manufacturing Costs
  - Manufacturability Costs
  - Size and Weight
  - Electrical Design
  - Thermal Design
  - Mechanical Design
  - (Design for) Manufacturability
  - (Design for) Testability



"Optimal" Package

Ceramics in Packaging

- Aluminum oxide (Al_2O_3)
- Aluminum nitride (AlN)
- Beryllium oxide (BeO)
- Silicon Nitride (Si_3N_4)

Ceramic	Dielectric Constant	Dissipation Factor, tan δ	Electrical Resistivity (Ω-cm)	CTE (ppm / °C)	TC (W / m-K)	Flex Strain (MPa)	Density (kg/cm^3)
Al_2O_3	4.5 - 10	0.0004 – 0.001	$> 10^{14}$	6.5 – 7.2	22 - 40	300 - 385	3.75 – 4.0
AlN	8.5 - 10	0.001	$> 10^{14}$	2.7 – 4.6	100 - 260	280 – 320	3.2
BeO	6.5 – 8.9	< 0.001	$> 10^{15}$	6.3 – 9.0	260 - 300	170 - 240	2.95
Si_3N_4	5 - 10	-	$> 10^{14}$	2.3 – 3.2	25 - 35	255 - 690	2.4 – 3.4

Characteristics

- Typically hard and brittle with low toughness and ductility
- Generally they are electrically and thermally insulating
- Ceramic materials normally have high melting temperatures
- High chemical stability
- May be amorphous, polycrystalline, or crystalline

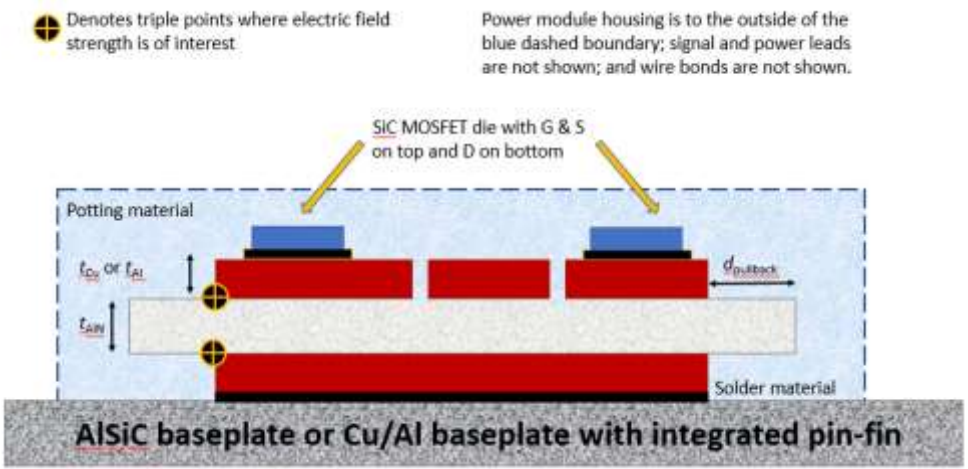
Metal	Conductivity (nΩ-m)	CTE (ppm /°C)
Al	28.2 at 20°C	21 – 24
Cu	16.8 at 20°C	16 – 16.7

Electrical Challenges

1. Insulation Coordination
   - Creepage
   - Clearance
   - External vs. internal
2. Dielectric Test / “High-Pot” Test
   – Vertical Isolation
   – Lateral Isolation
   – Need for testing beyond 50/60 Hz
   – Testing at temperature
3. Partial Discharge Test
   - PD inception voltage
   - PD extinction voltage
   - Need for testing beyond 50/60 Hz
   - Testing at temperature

$T_{ceramic} \in [20\ °C \ldots 200\ °C]$

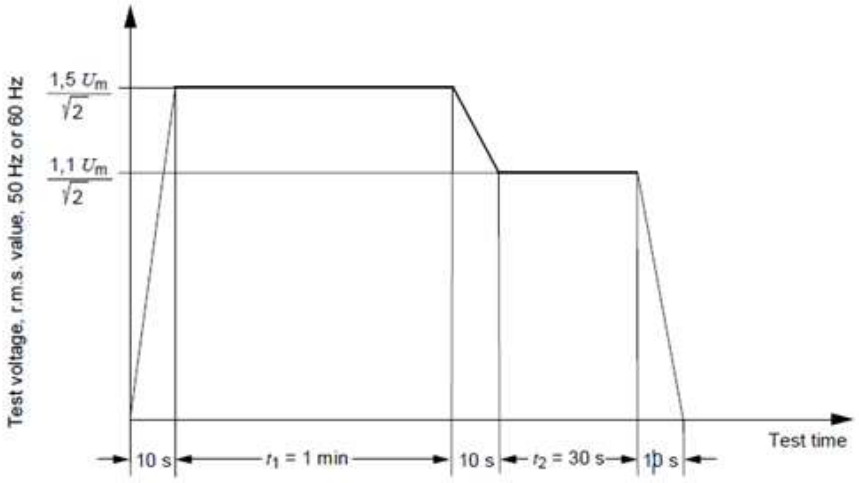
Power substrate structure within a MV power module



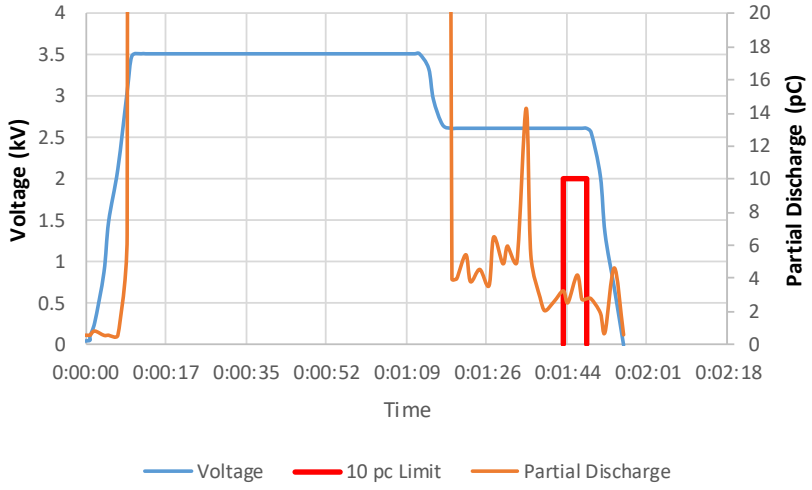
Partial Discharge Test

IEC 61287-1† states: “This test is carried out to verify the insulation of elementary components or subassemblies. It is recommended to perform this test for equipment working at 1,500 V or more, especially for new components and for semiconductor device assemblies with new insulating technology.”

† Railway applications – Power converters installed on board rolling stock – Part 1: Characteristics and test methods



Voltage test profile for the partial discharge test.



Example 3.3 kV power module test result.

Design Considerations for Partial Discharge Testing

- Application specific
  - Electro-, Thermal-,
  - Mechanical-, Chemical
- DBC vs. Cu AMB
- Need for dimpling
- Metal etching to improve PD
  - E field management
- Soldering/Brazing vs. US welding

Material	Thermal Conductivity W/mK @ 20°C	CTE ppm/K @ 20°C	Lifetime – Cycles Without Dimples★ Cu/Ceramic/Cu (mm)	Lifetime – Cycles with Dimples★	Dielectric Constant @ 1 MHz	Dielectric Constant @ 1 GHz	Dielectric Strength, ASTM D116, kV/mm (AC)	Dielectric Strength, JIS C 2141, kV/mm (AC)	Ceramic Thickness (0.635 mm)	Ceramic Thickness (1.00 mm)
Al_2O_3	24	6.8	> 65 0.3/0.32/0.3	~650	9.8	10.0	15	15	×	×
Si_3N_4	54	2.5	> 5000 0.5/0.32/0.5	~50,000	8.0	7.5	17.7	12	0.32 mm	
AlN	170	4.7	> 35 0.3/0.635/0.3	~350	9.0	7.5	15	14	×	×

Source: Curamick Ceramic Substrates, DBC technology, Design Rules, Version 12/2014.

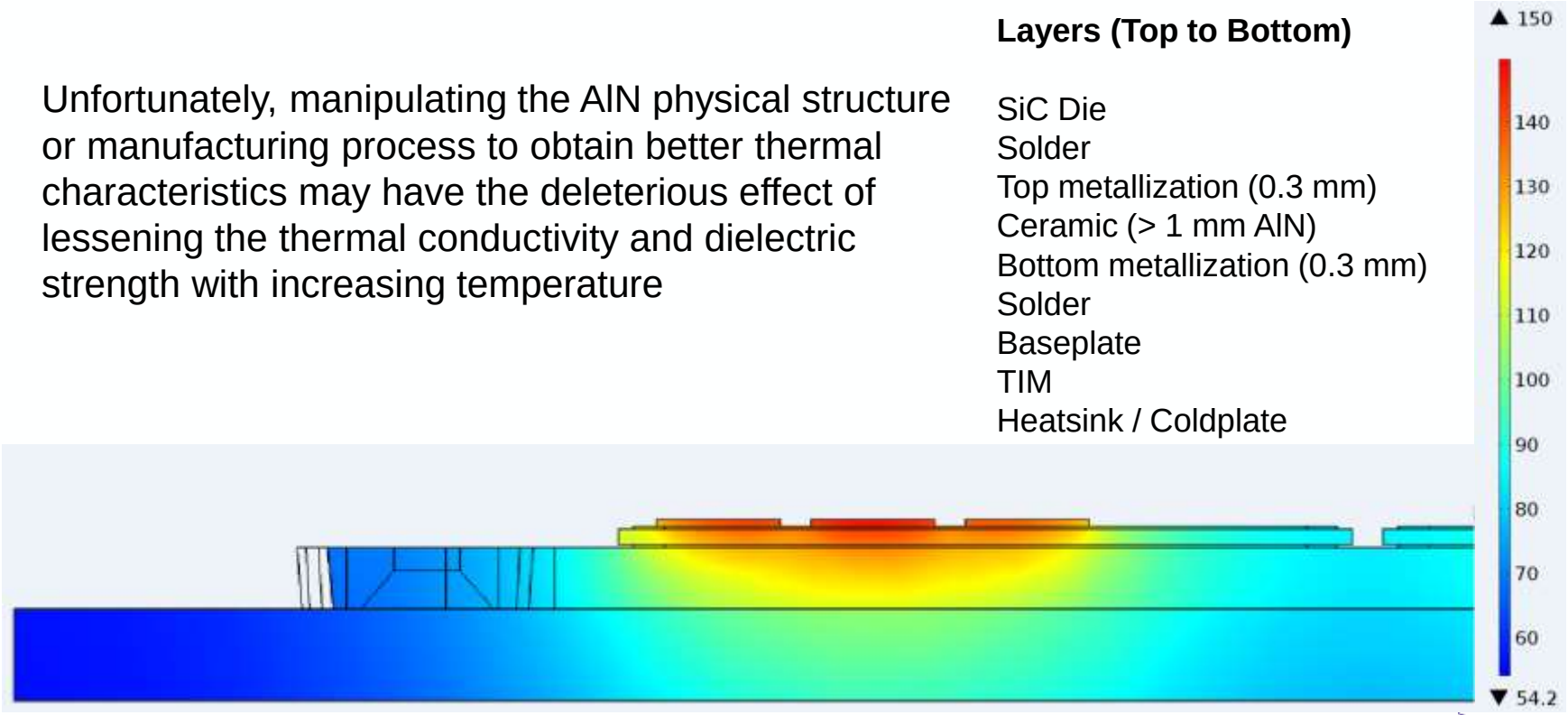
★ Lifetime measurement conditions: -55 °C to 150 °C thermal shock testing

Thermal Challenges

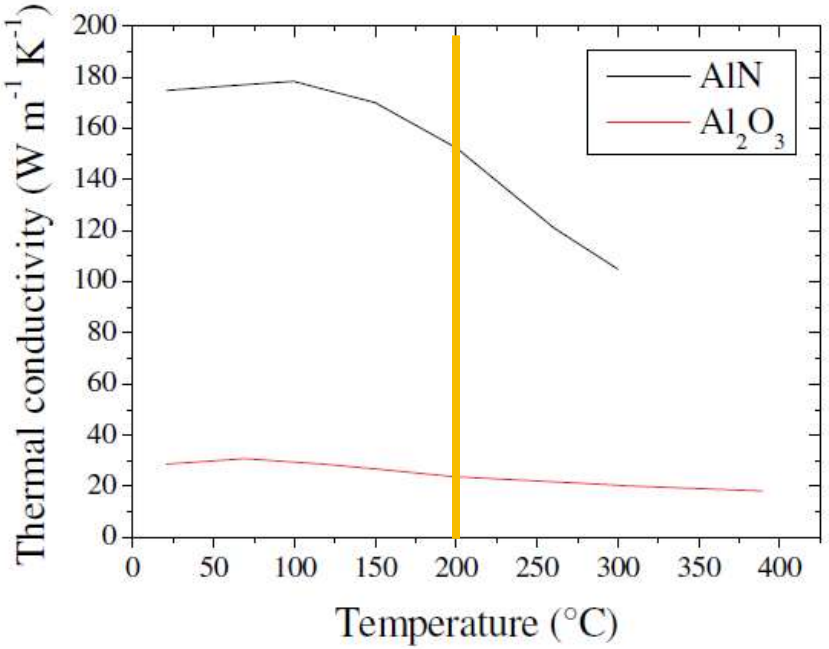
Unfortunately, manipulating the AlN physical structure or manufacturing process to obtain better thermal characteristics may have the deleterious effect of lessening the thermal conductivity and dielectric strength with increasing temperature

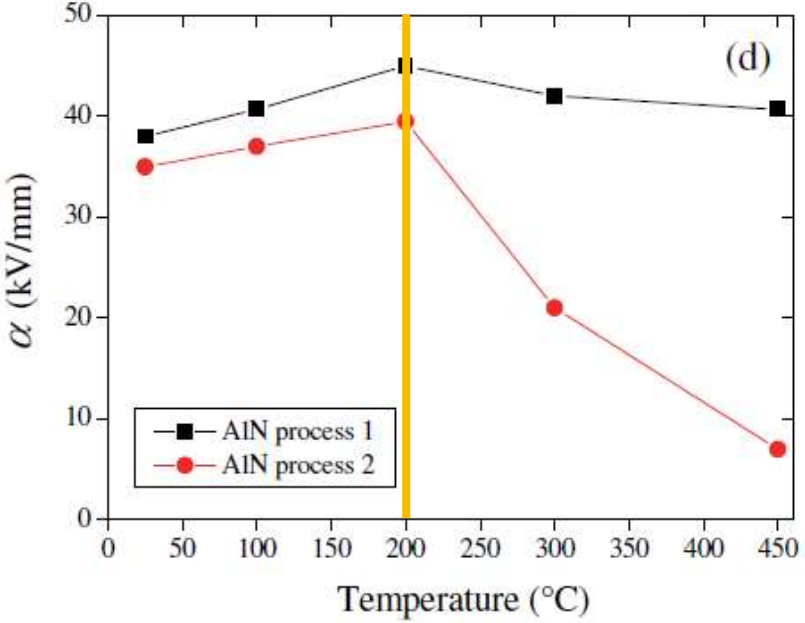
Layers (Top to Bottom)

SiC Die
Solder
Top metallization (0.3 mm)
Ceramic (> 1 mm AlN)
Bottom metallization (0.3 mm)
Solder
Baseplate
TIM
Heatsink / Coldplate



Thermal Challenges, cont.





Sombel Diaham, Marie-Laure Locatelli and Zarel Valdez-Nava (2011). Dielectrics for High Temperature SiC Device Insulation: Review of New Polymeric and Ceramic Materials, Silicon Carbide – Materials, Processing and Applications in Electronic Devices, Dr. Moumita Mukherjee (Ed.), ISBN: 978-953-307-968-4, InTech.

Mechanical Challenges

Highly Accelerated Life Testing (HALT)

- Thermal cycling between -55 °C to 200 °C with > 15 Grms random, six-axis vibration
- No PASS / FAIL; seek to identify failure mechanisms and fortify through design iterations

Thermal cycling

- CTE mismatch
- Delamination at the metal-ceramic interface
- Ceramic failures (e.g., microcracks, delamination at the A-B interface, etc.)
- Solder delamination between power substrate and baseplate

Processes – Mechanical attaches (e.g., substrate-baseplate, USW of power leads)

Summary

- The design of a MV power module is non-trivial; it is an electro-, thermal-, mechanical-, chemical system; multi-domain optimization problem
- In general, ideally, one would work “inside out” – optimizing from the SiC MOSFET die outward toward the terminal-bussing interfaces
- This is not possible when using a common power module specification like that found in the European Roll2Rail Program (New Dependable Rolling Stock for a More Sustainable, Intelligent and Comfortable Rail Transport in Europe, D1.2, New generation power semiconductor – Common specification for traction and market analysis, technology roadmap, and value cost prediction, R2R-T1.1-D-BTS-030-07, pp. 37-52, 25/10/2016)
- This is also true when licensing an industry-standard module footprint
- In order to maximize gravimetric and volumetric power densities, one must consider moving from a planar/2-D approach to a 3-D approach
- The specifics for how this is done is proprietary