

10A DC-DC Point-Of-Load Power Modules with Integrated Inductors and Capacitors less than 1.0mm Height for Mobile Platforms



Outline

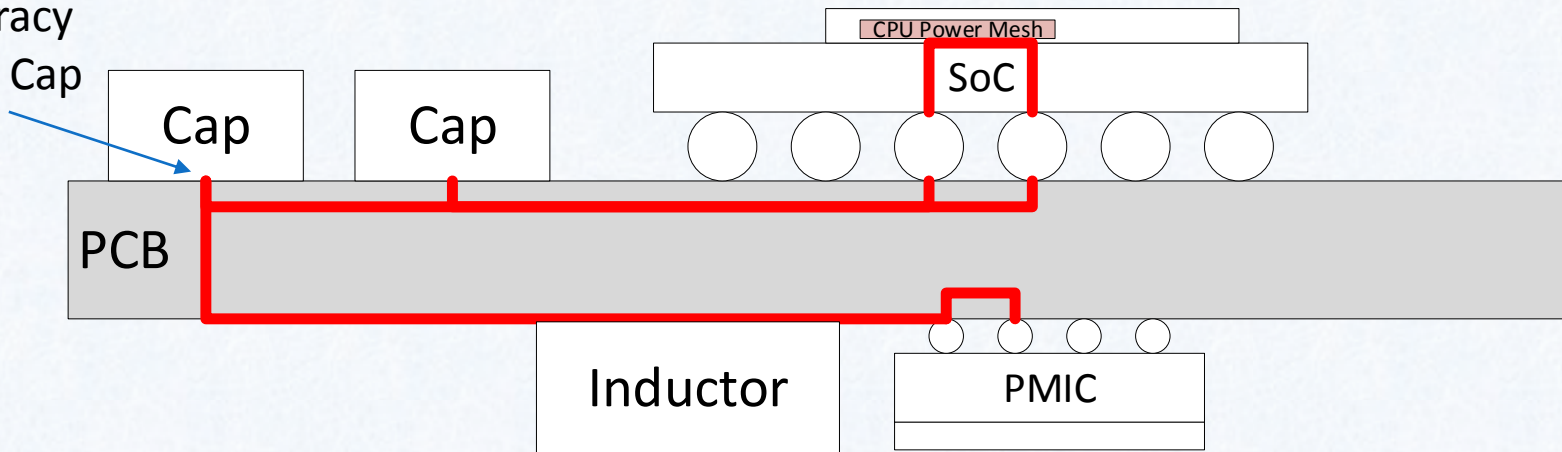
- **Motivation**
 - Platform level challenges: space constraints and PDN bottlenecks
 - Power, Performance, and Area benefits of distributed power solutions
- **System Level Considerations**
 - Optimization for distributed, more granular power domains
 - Packaging Technology Solution
- **Measurements**
 - SiP and Power Module Evaluation
- **Conclusions**

Motivation

- Distributed Ultra-Compact Power Solutions
 - 5A-10A solutions, up to 10W sustained power and 3V-5V input
- Space Constraints and PCB routing challenges
- PDN Challenges – Platform Level Validation
 - Co-design and optimization of power delivery
 - Co-design and droop mitigation for CPU/GPU power domains
- PDN Challenges – Droop Mitigation
 - 1-10ns load transient challenge
 - 100ns load transient challenge

Space Constraints and PCB Routing Challenges

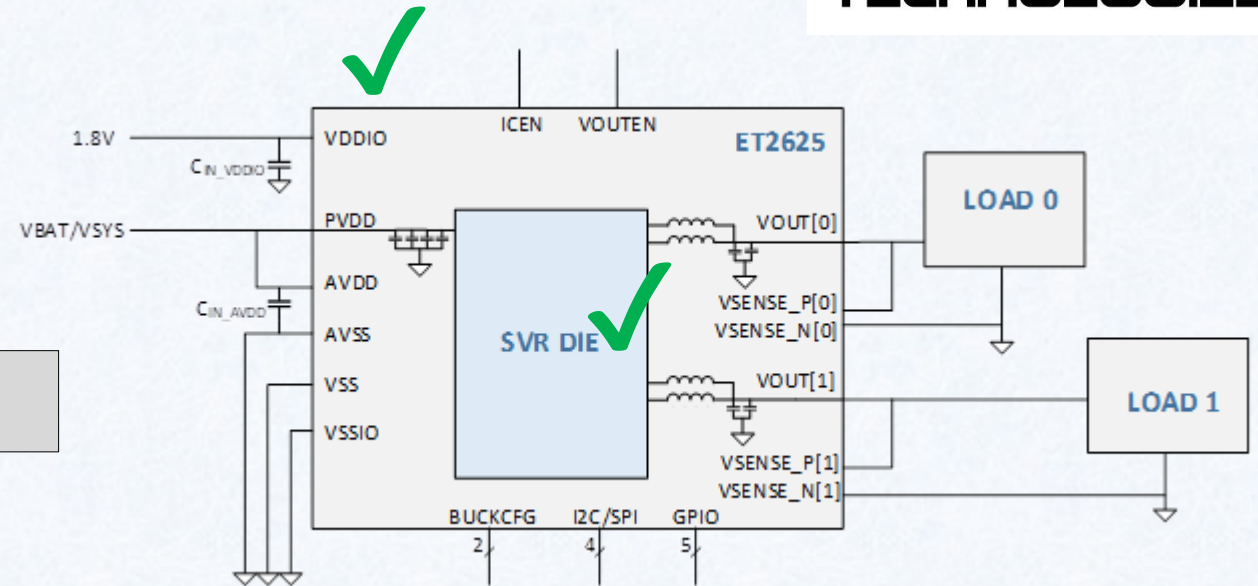
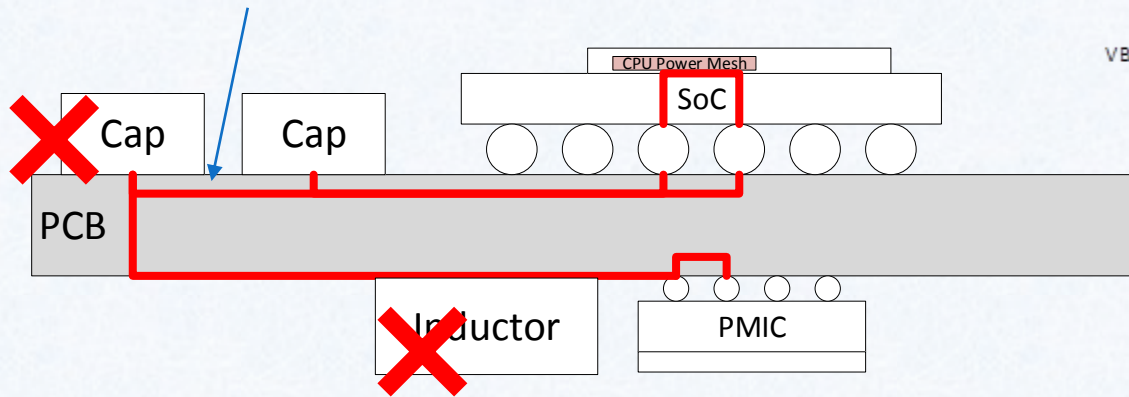
Regulation Accuracy
specified at bulk Cap



- Conventional DC-DC solutions with $<5\text{MHz}$ switching frequencies require large inductors and array of low-ESL capacitors
- PCB routing losses need to be included in the overall efficiency calculations
- Fully integrated, POL modules or in-package integration needed to address these challenges

PDN Challenges – Platform Level Validation

Regulation Accuracy
specified at bulk Cap



- PMIC evaluation performed with oversized components on “ideal” PCB. Final product validation performed without components.
- Regulation accuracy needs to be specified at the CPU power mesh
- Fully integrated module validation includes all components and critical routing

PDN Challenges – Droop Mitigation

- **$L \cdot di/dt$ voltage drop across the parasitic inductance**
 - Current solutions rely on low-ESL capacitor array for fast load transients which is limited by the number of capacitors that can be placed in parallel next to SoC
- **$R \cdot I$ voltage drop across the parasitic resistance**
 - Remote sense technique is useful only for partial compensation of IR drop and only if fast load transients supported. It does not help in worst case of 0- \rightarrow I_{max} transition.
- **On-chip design solutions required to address PDN challenges**
 - 1ns-10ns load transients best handled by on-chip droop mitigation solutions
 - Droop mitigation solution such as Endura eTC™ can be extended up to 50ns
 - Voltage regulation need to seamlessly overlap the response of droop mitigation

Technical Approach

- **Active Transient Control – Integrated within CPU/GPU**
 - Gen2 eTC 10nm FF [presented at ISSCC 2017]
 - Gen3 10nm FF integrated into product
 - Gen4 eTC 12nm/7nm [to be published]
- **SiP solutions - Embedded Voltage Regulator (eVR)**
 - [presented at 3D-PEIM, 2018]
- **Ultra-Compact module solutions – Fully integrated modules**
 - Mobile Platforms (Area=18mm², Thickness= 0.9mm)
 - Server/Industrial Platforms (Area=25mm², Thickness=1.2mm)

DROOP
MITIGATION
<10ns Load
Transients

FAST DVFS
~100ns Load
Transient

COMPACT
DISTRIBUTED
MODULES
Point of Load

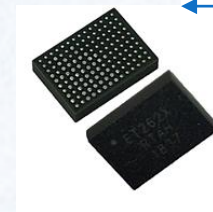
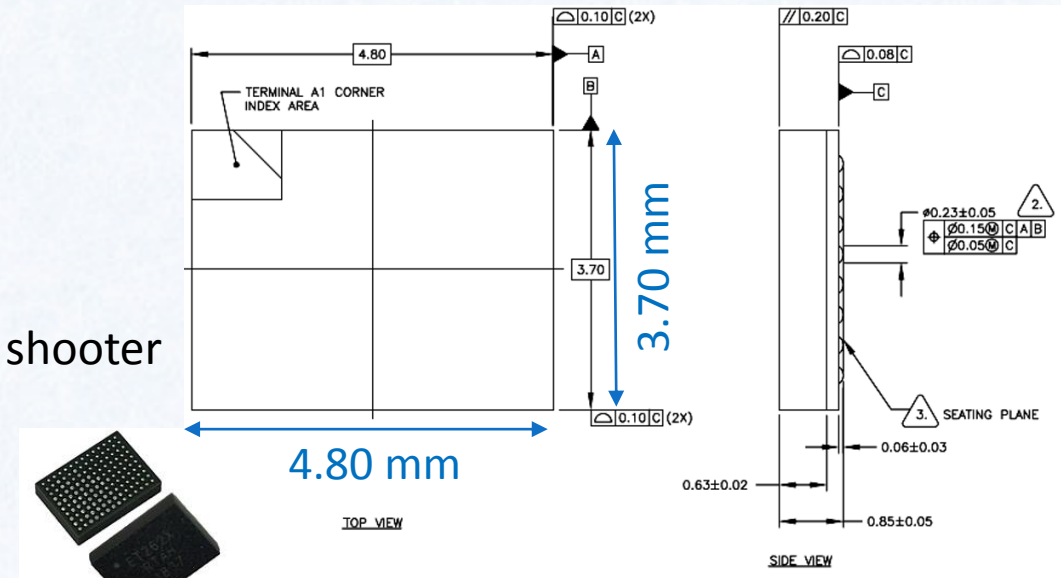
Power Module Package Solution

➤ Package information

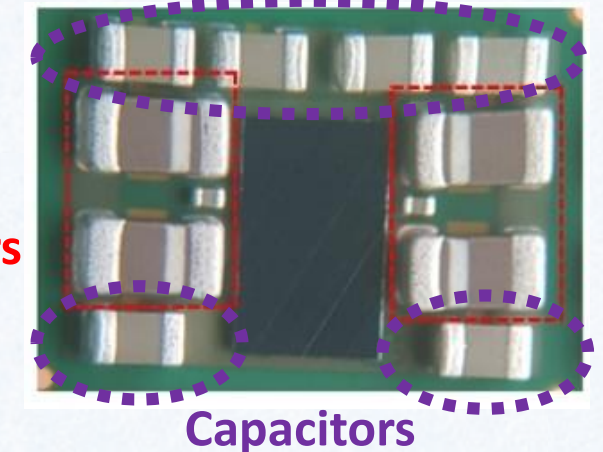
- ET262x Size: 6.0x4.3x1.15; 0.4mm pitch Micro-BGA
- ET261x Size: 4.8x3.7x0.85; 0.4mm pitch Micro-BGA
- Assembly: one flip chip die and 12 passives using chip shooter

➤ Summary of Packaging Solution Requirements

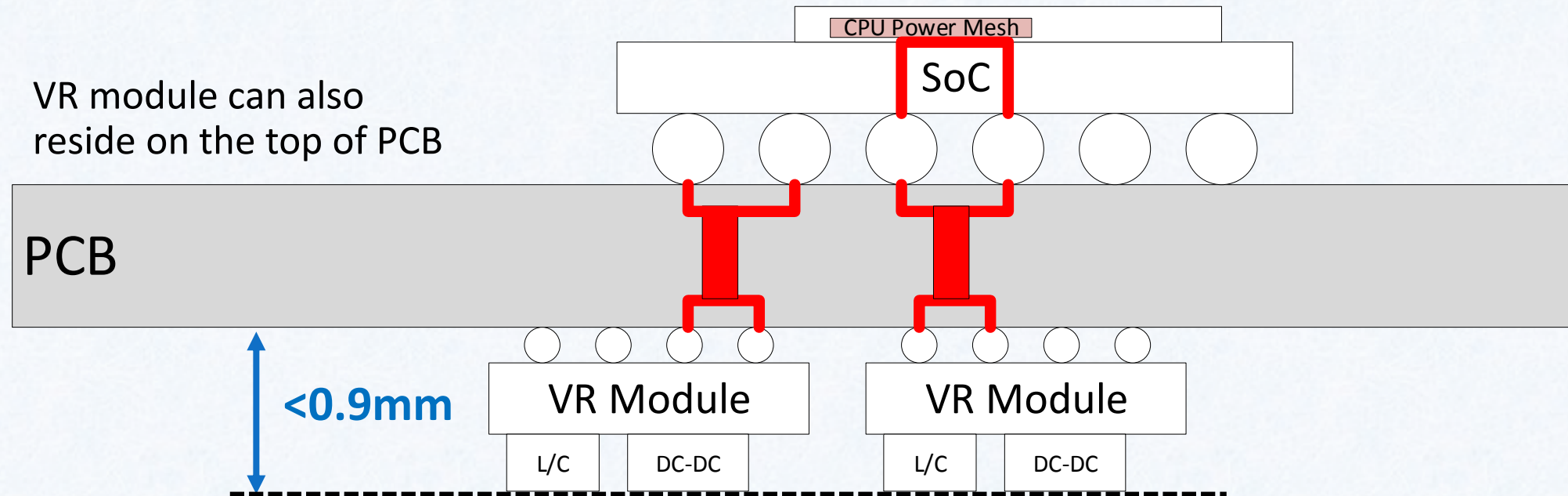
- Thin substrate (0.16mm coreless) vs thicker mold cap (0.63mm and 0.93mm for ET261x and ET262x)
- High density SMT component population on thin substrate:
- Micro-BGA ball attachment (0.15mm BGA ball): 60um height



Inductors

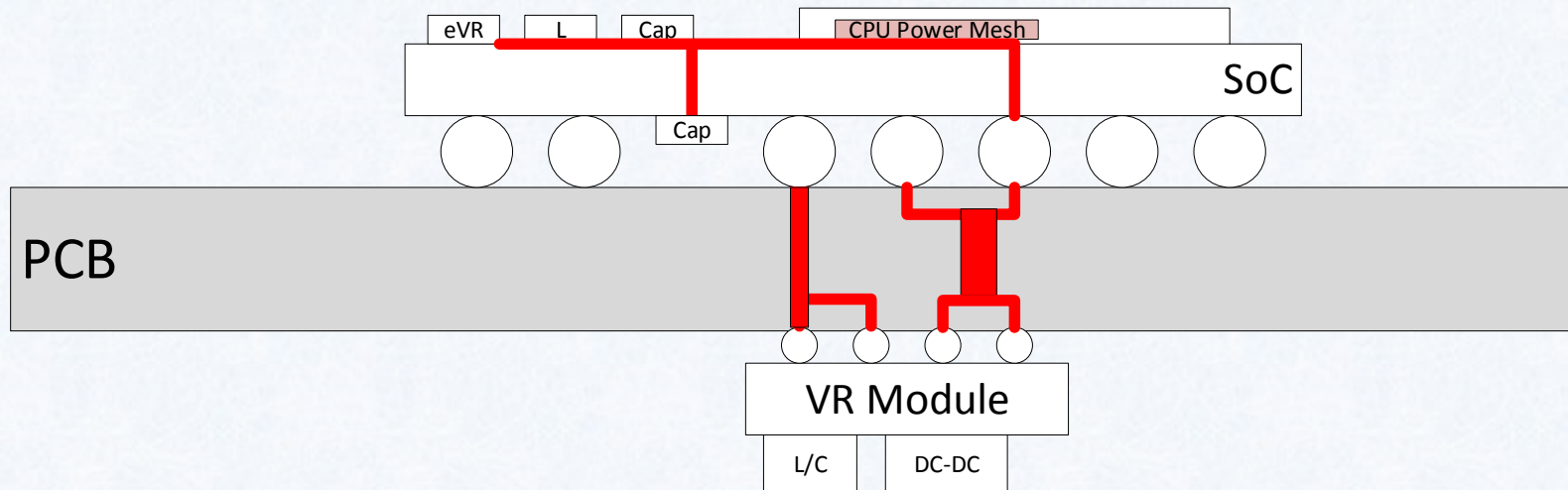


Ultra-Compact Power Module Solutions



- Fully integrated compact module with less than 0.9mm height
 - Provides easy adoption and faster TTM without SoC package re-design
 - Significant PCB area reduction with integrated inductors and capacitors
 - PCB routing minimized with significant reduction of losses

SiP integration in SoC Package

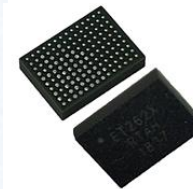


- 130MHz, 6A, 3-phase 1.8V input voltage DC-DC implemented in 1mm³
- Programmable internal clock from 13MHz – 130MHz
- Inductor and capacitor determined based on transient response and total regulation accuracy including ripple at power mesh

Measurements: SiP and Power Module

- Measurement configurations and evaluation board
- 130MHz SiP Solution Advantages
 - Fast start-up
 - Fast Dynamic Voltage Control (DVC)
 - Fast load transient
 - Switching frequency vs Inductor values
- Extending the solution to Power module with Li Ion battery input
 - Efficiency: SiP solution and Power Module
 - Thermal performance: 10A, 10W, 10MHz Power Module
 - Benefits of Load Line regulation

Evaluation Board and Configurations

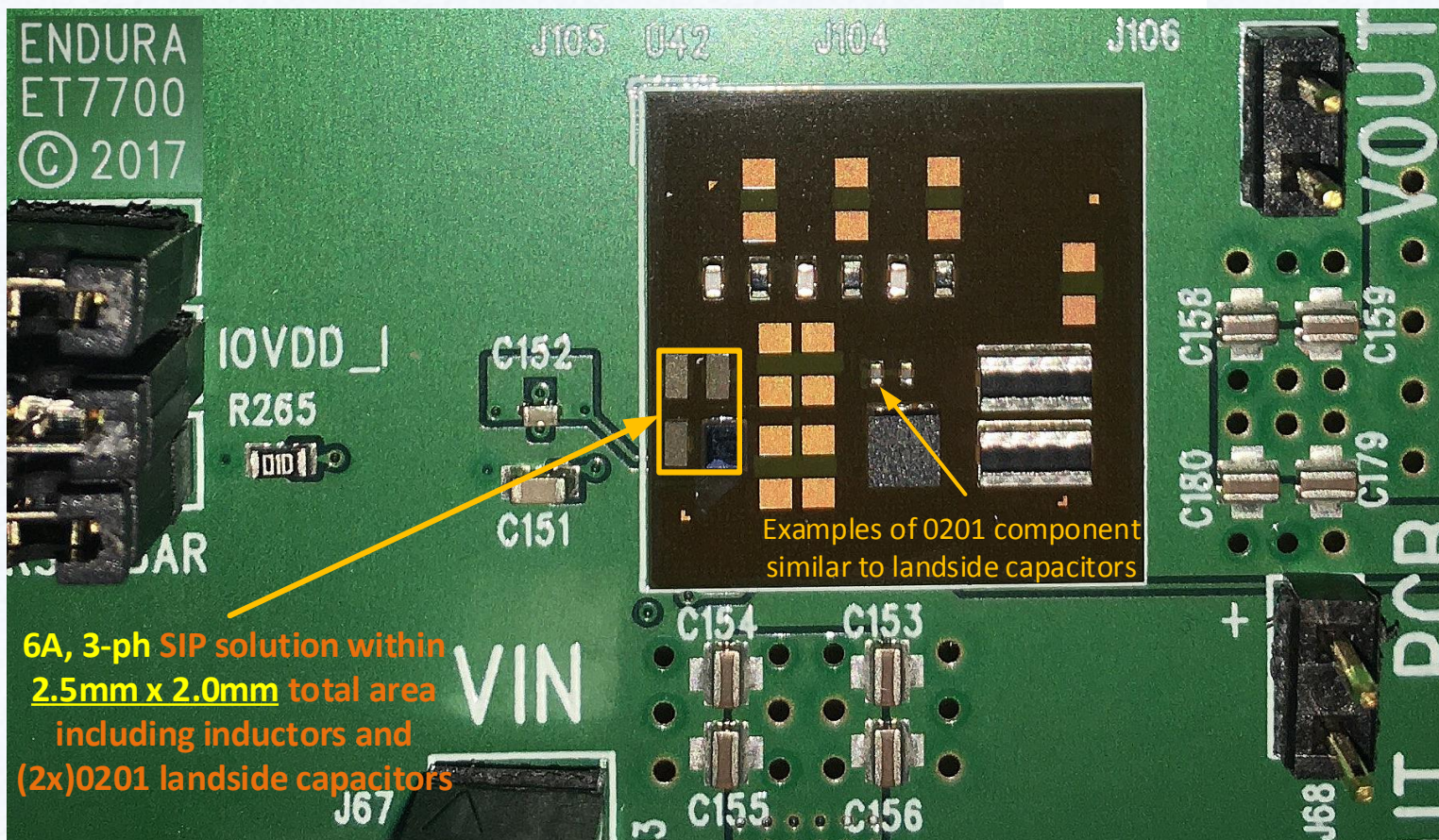


Fully Integrated Power Module for distributed power on PCB

- V_{in} : 3.0V – 5.5V, F_{sw} : 10MHz
- I_{max} : 10A, Max. Power: 10W

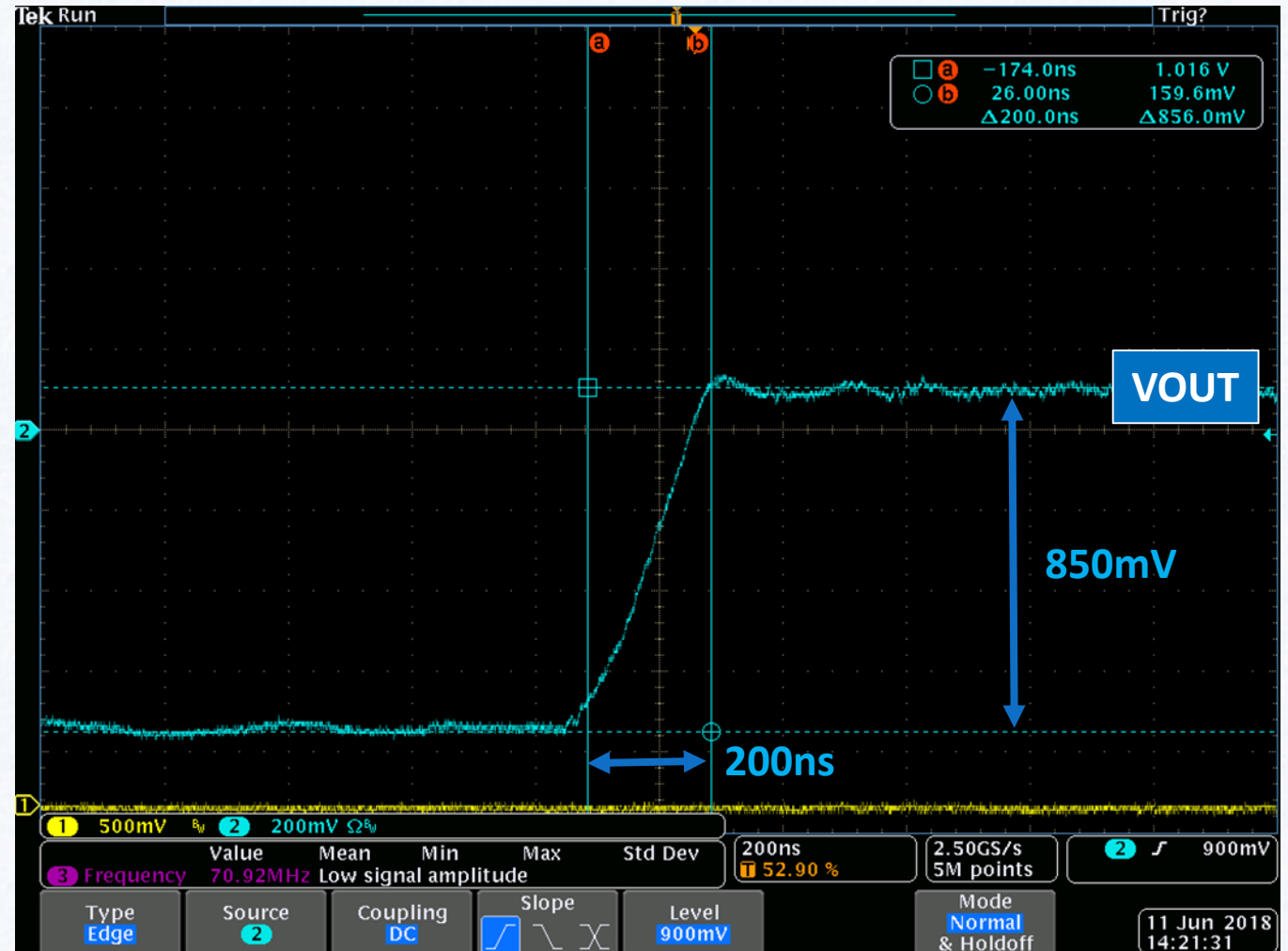
SiP prototype suitable for PoP integration

- (2.5mm x 2.0mm, $T < 0.2$ mm)
- V_{in} : 1.6V to 2.0V
- F_{sw} : 13MHz to 130MHz
- I_{max} : 6A



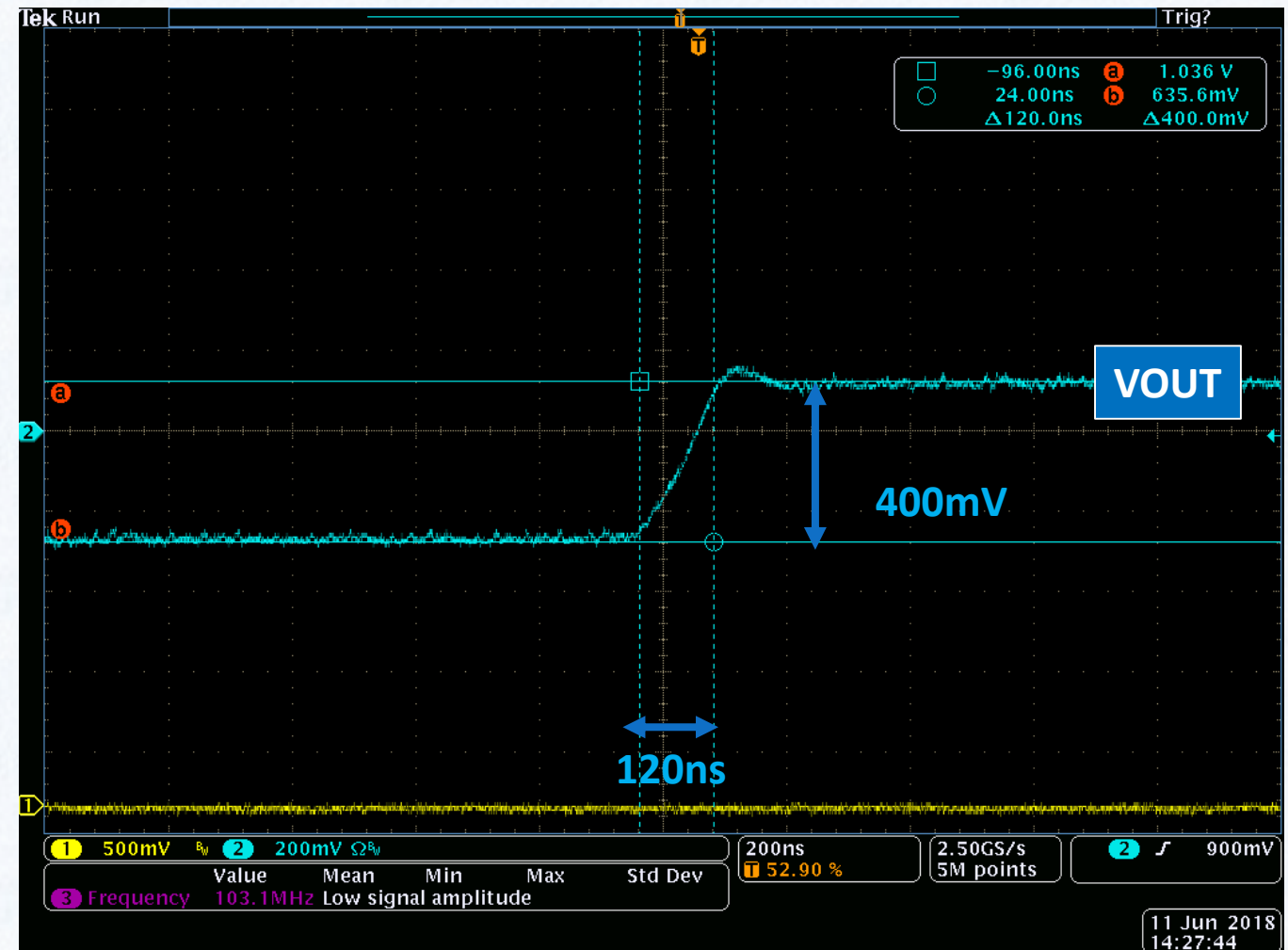
Fast Start-Up

- Dormant to regulation in 200ns
- Ability to provide regulation for the entire load range at 200ns



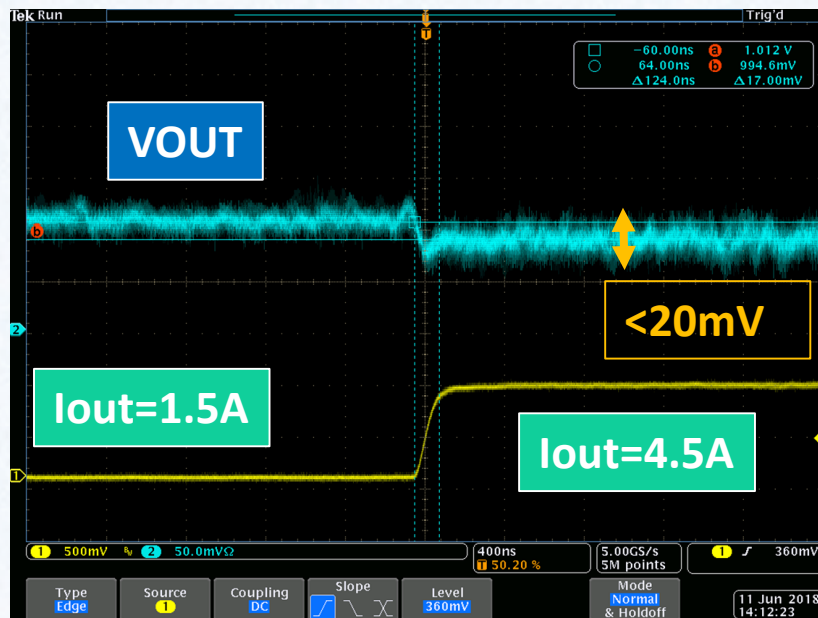
Fast Dynamic Voltage Control (DVC)

- Fast DVC : 400mV / 120ns
- Suitable for High Definition Dynamic Voltage and Frequency Scaling (DVFS) control of SoC power domains



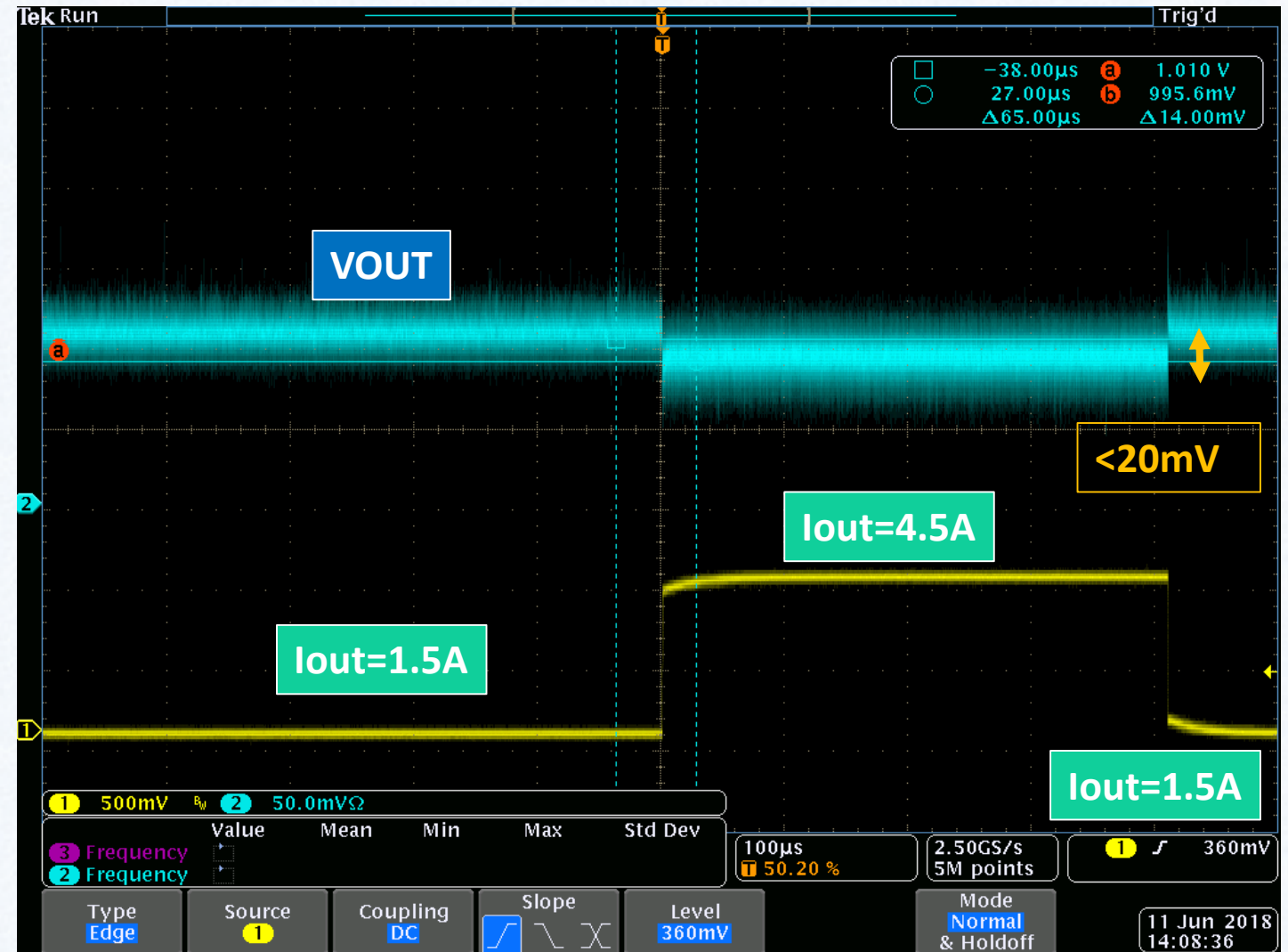
Fast Load Transient

- Load Transient:
 - 1.5A \rightarrow 4.5A in 100ns
 - 4.5A \rightarrow 1.5A in 100ns



Zoomed in showing light load to high load transient

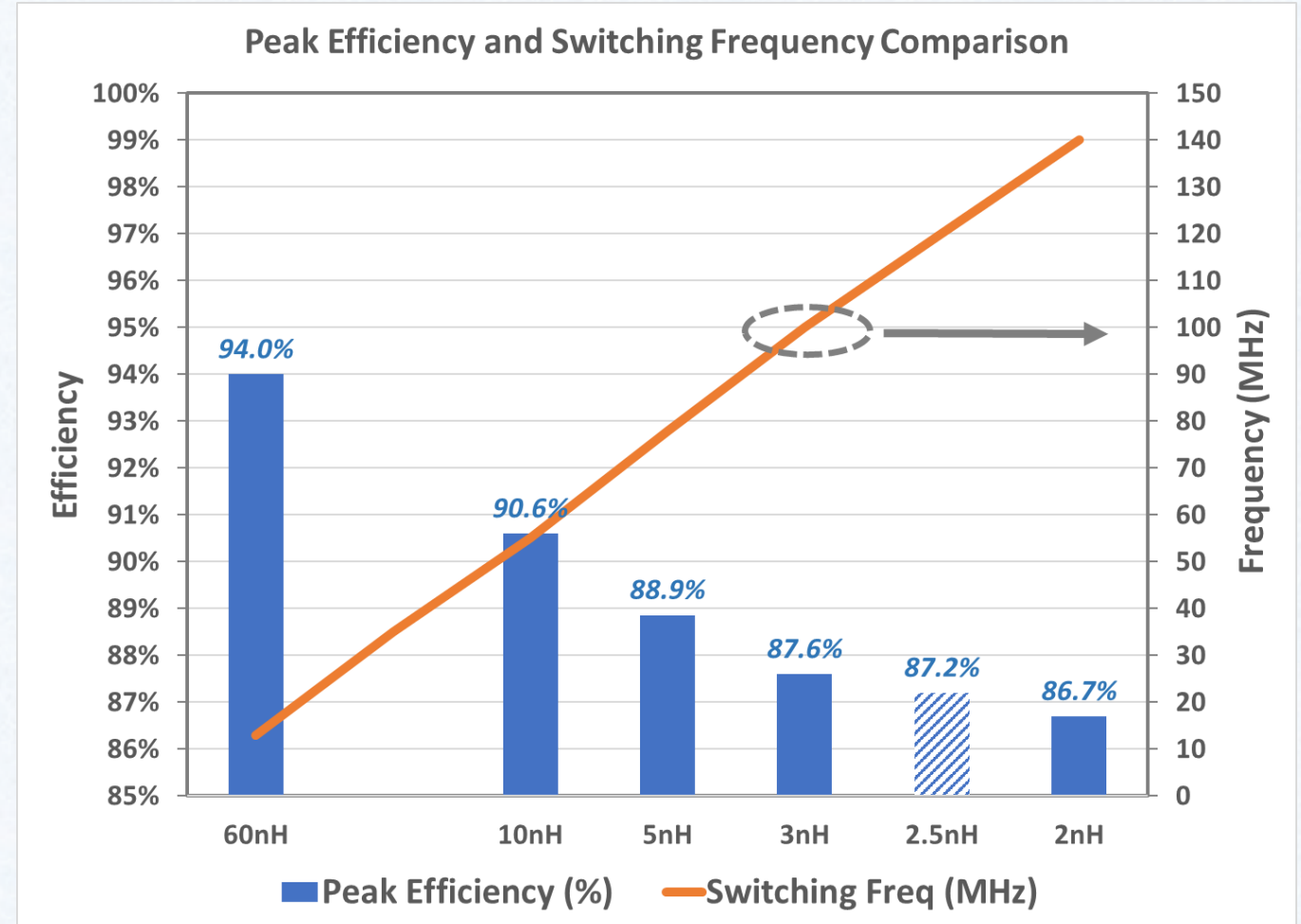
March 20, 2019



APEC 2019, Endura Technologies, Dosluoglu et. al.

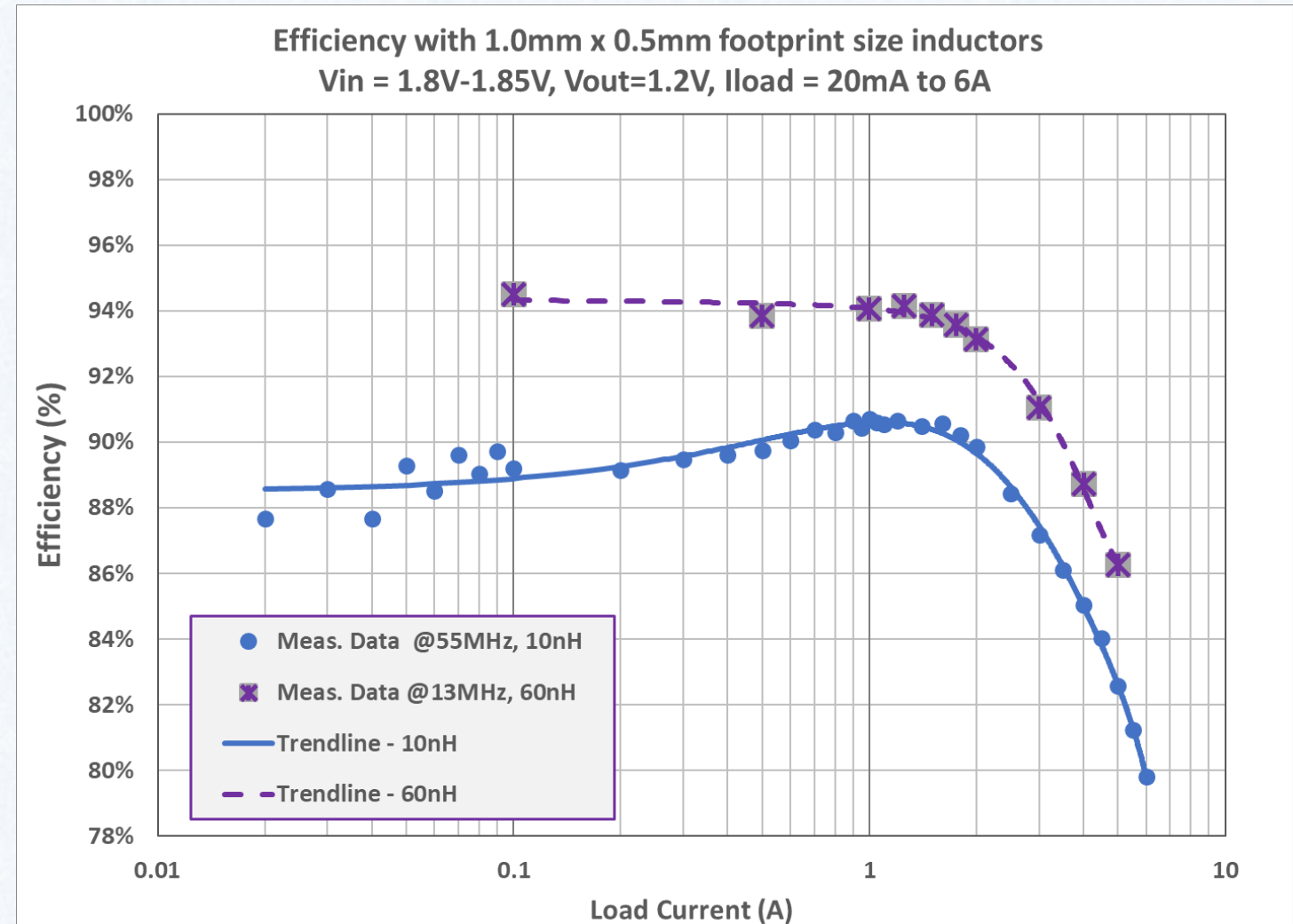
Switching Frequency vs Inductors

- Optimum switching frequency for maximum efficiency
 - SiP solution: $L = 2\text{nH} - 10\text{nH}$
 - Power Module: $L = 60\text{nH}$
- Switching loss vs R_{DSon} optimized to achieve $>85\%$ efficiency for the entire load range
 - SiP solution: I_{max} up to 6A
 - Power Module: I_{max} up to 10A



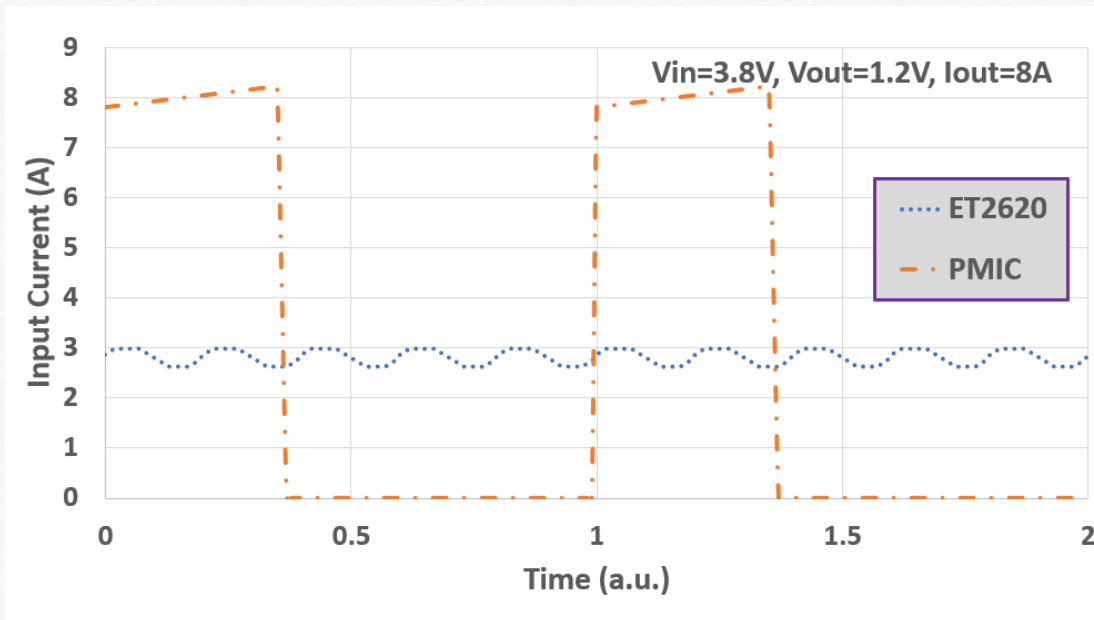
ET7730 Efficiency Measurements

- 3-phase, up to 2A/phase
- Single mode operation for the current load range 20mA to 6A
 - Seamless DCM/PFM to CCM/PWM transition
 - Seamless phase-shedding
- >88% efficiency up to 2.5A (SiP) with 10nH inductors
- 94% efficiency with 0.5mm thick 1.0mm x 0.5mm footprint 60nH inductors (module)

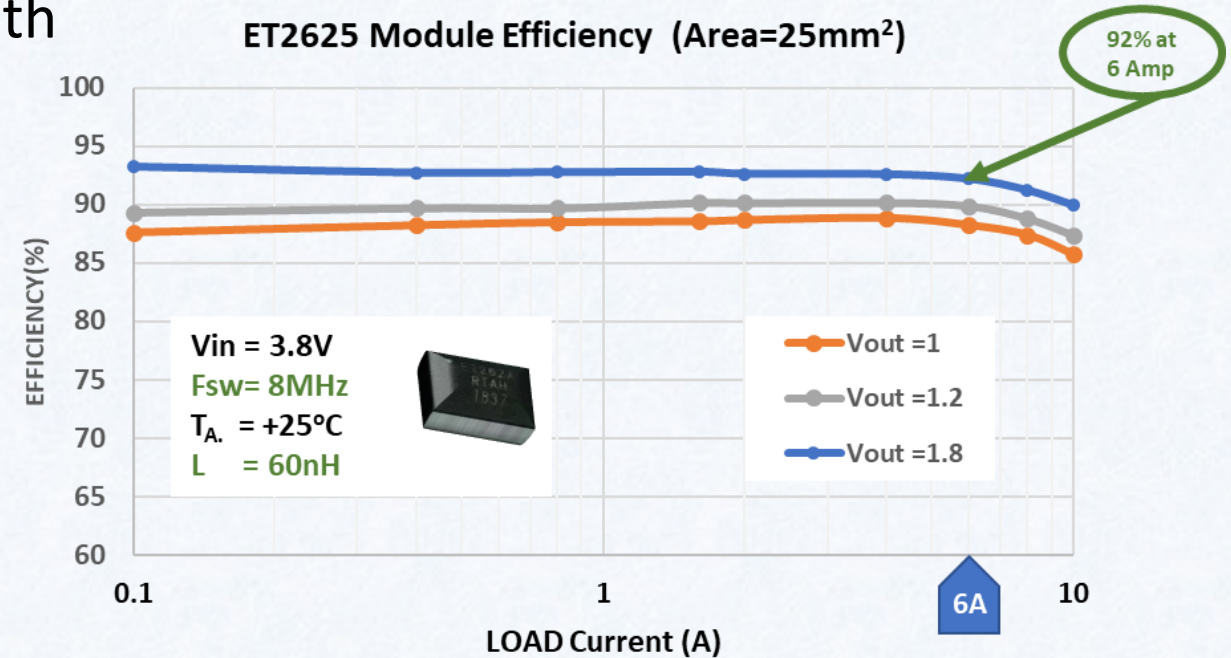


Fully Integrated Module Efficiency

- Single or Dual output configurations with Li Ion battery input ($V_{in} = 3.0V \rightarrow 5.5V$)
 - 4-phase 10A
 - 2x2-phase 2x5A



High input peak current with additional rms losses

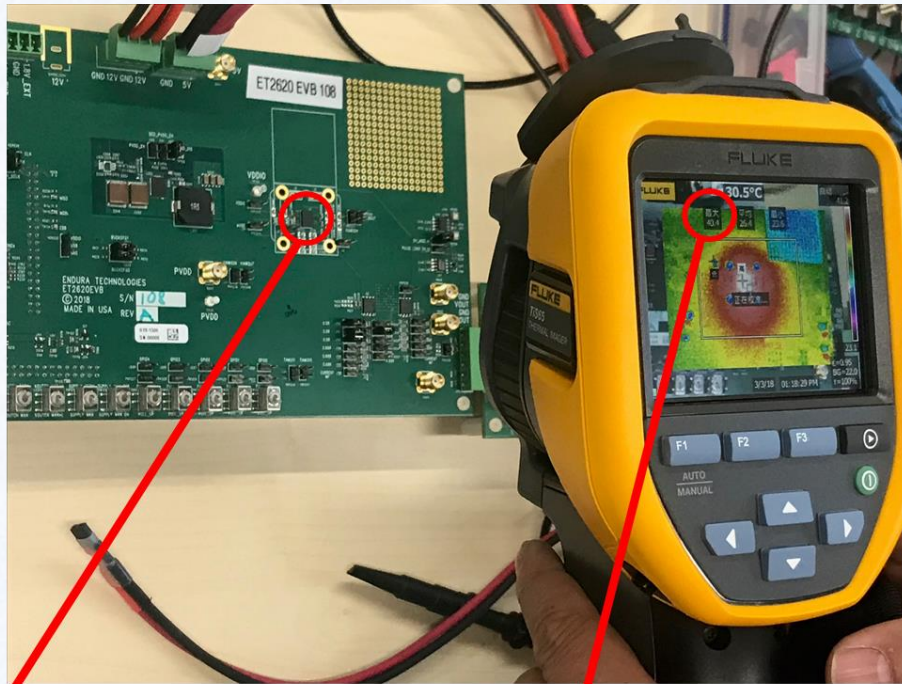


Multi-phase with integrated input capacitor

- No additional peak current losses at the input
- High current single phase PMIC has additional 3%-4% loss in platform

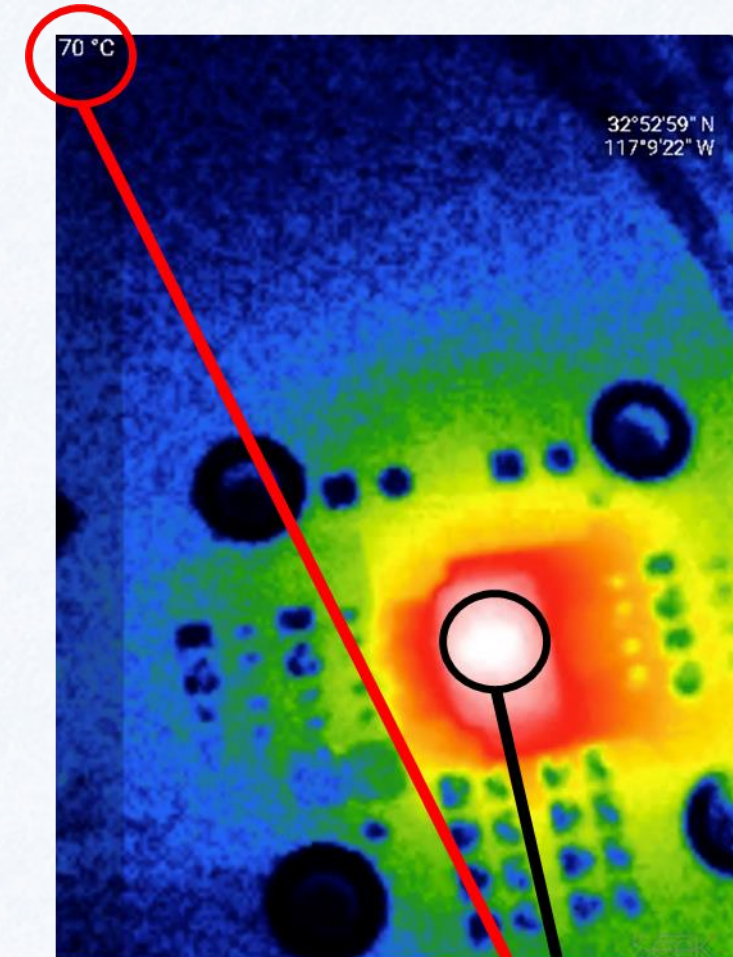
Thermal Measurements

- 10A, 10W, 10MHz Fully Integrated Power Module
 - Sustained 5W delivery at 40C (20C above ambient)
 - Sustained 10W delivery at 70C (50C above ambient)



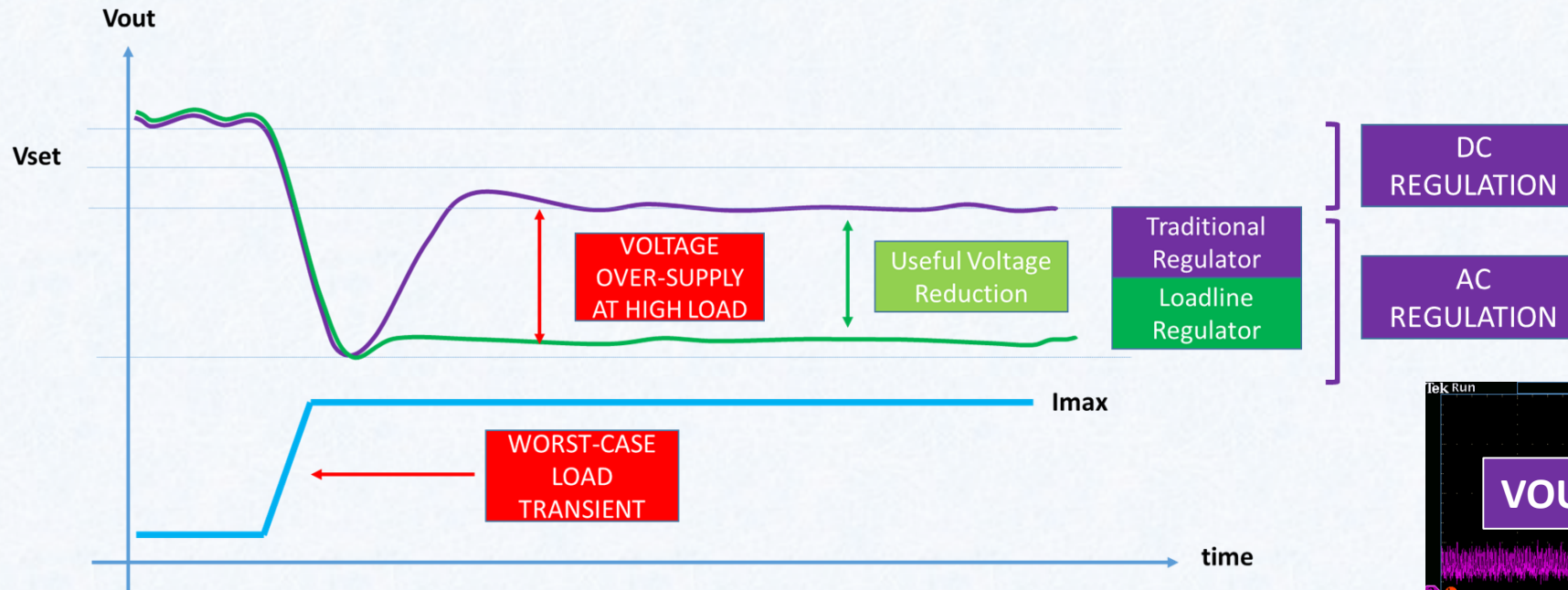
ET2620 Module

$I_{out} = 5\text{Amps}$, 40 Degree C

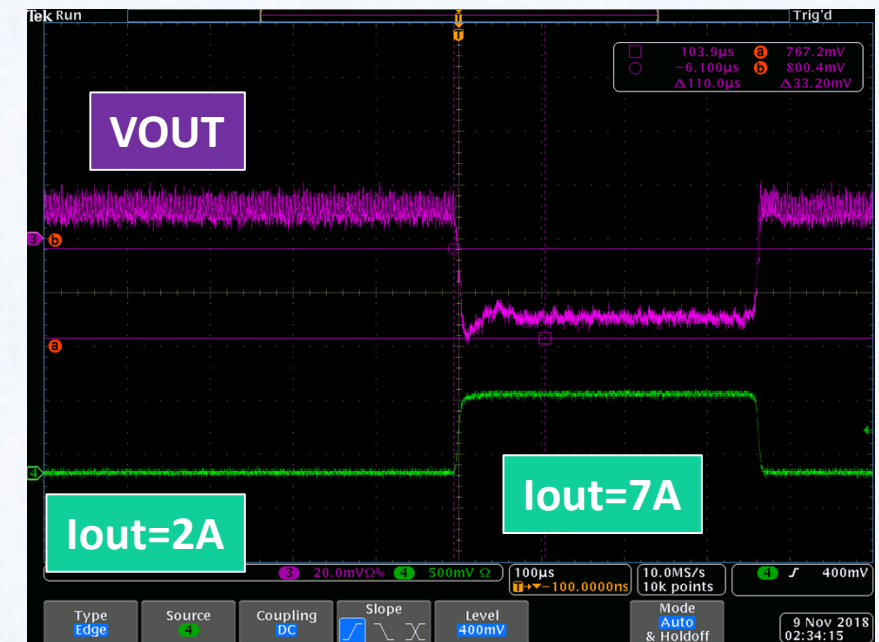


$I_{out} = 10\text{Amps}$, 70 Degree C

Demonstration of Load Line Regulation



- ET2620 load line with 5A load step transient
- Step response with DC regulation optimized to match AC regulation in fully integrated module



Distributed Power Solutions

- System level optimization require compact flexible solutions
 - Fast DVFS require fast switching frequencies and smaller output capacitors
 - Fast switching regulators implemented at point of load may require lower input voltage
 - Fully integrated module solutions allow full control of components and minimize routing of high frequency switching nodes
 - Best optimization achieved by integrating the power delivery solution in the packaged product or power modules with integrated components
- Co-design power solution from battery to CPU/GPU power mesh with SoC Team
 - Active Transient Control – Integrated within CPU/GPU
 - SiP solutions - Embedded Voltage Regulator (eVR)
 - Compact module solutions – Fully integrated modules

Conclusions

- Power Management and SoC Requirements
 - Defining regulation on PCB capacitor is inadequate
 - Need to define V_{min} at SoC power mesh at max clock frequency target and worst case load transient
 - Regulation requirements need to be reconsidered based on V_{min} (power saving with load line)
 - Power savings of up to 20% can be achieved with granular power and fast dynamic voltage control
- Distributed Power Solutions
 - Embedded Voltage Regulator (eVR) for SiP integration
 - Fast start-up in 200ns for power savings in frequent burst mode operations and power cycling
 - Fast Dynamic Voltage Control for high definition DVFS with ramp rate $>3V/\mu s$
 - Fast switching frequency for up to 1A/30ns load transients
 - Fast switching frequency for up to 30mV DVFS set point in 10ns
 - Fully Integrated Compact Power Modules
 - Can be placed very close to power domains without additional routing to/from components
 - Validation and testing include actual inductor and capacitor components

THANK YOU!