Thermal Modeling Challenges for Multilayer Ceramic Capacitors(MLCCs) in High Power Density Assemblies

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Background

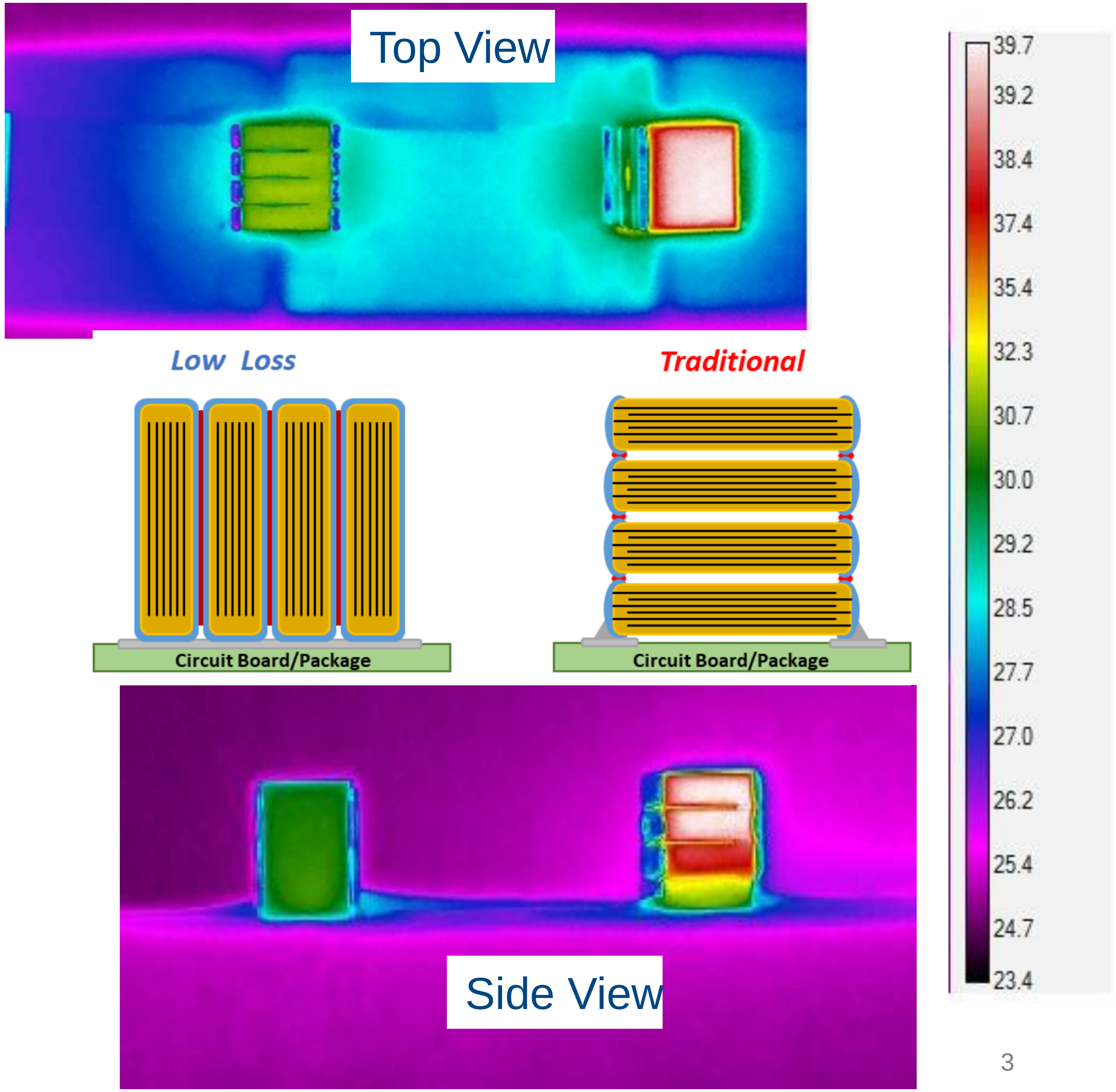
- KEMET developed Class 1 Ni BME MLCC (KC-LINK™) for use at higher frequencies and temperatures with WBG semiconductors.[1]
- Higher capacitance surface mountable leadless stacks (KEMET KONNEKT™) have lower heat dissipation when mounted with inner electrodes perpendicular to the printed circuit board (pcb).
- To better understand its thermal properties, a 3640 0.22µF rated MLCC was modeled and measured to obtain thermal resistance and capacitance.
- Thermal models and measurements have been made for 3640 Leadless Stack (KEMET KONNEKT™) packages to understand their performance in power supplies.

- ***1. 'An Evaluation of BME C0G Multilayer Ceramic Capacitors as Building Blocks for DC-Link Capacitors in 3-D Power Electronics', J. Bultitude et al, 3D PEIM 2016, Raleigh, NC, USA***

Presentation Outline

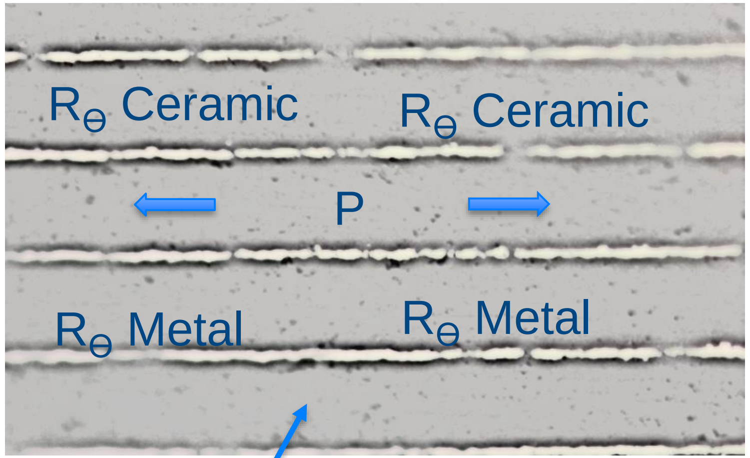
- Thermal Resistance of MLCC materials
- MLCC Finite Element Model (FEM)
- MLCC Experimental Results
- Revised MLCC Orientation Model
- Leadless Stack Models
- Leadless Stack Experimental Results
- Thermal Impedance Network
- Conclusions

The max temperature of an MLCC in a 4 component leadless stack varies based on how the component is mounted to the substrate was reported at APEC 2017 [2]



2. ‘Developing Capacitors for Wide-Bandgap Applications’, John Bultitude APEC 2017

Thermal Resistance Path to Each Termination



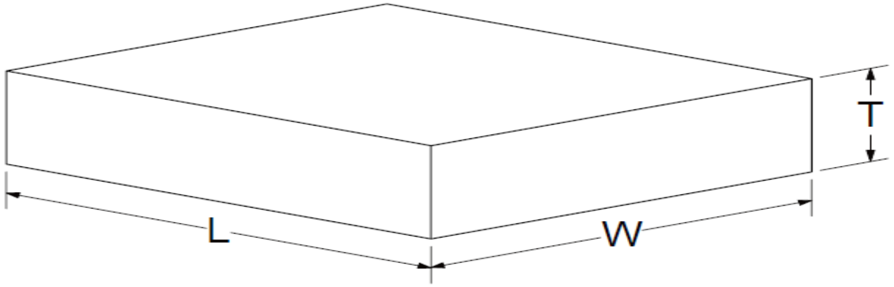
Active (parallel plate dielectric layer)

R_Θ = L/(K*A)

K = thermal conductivity

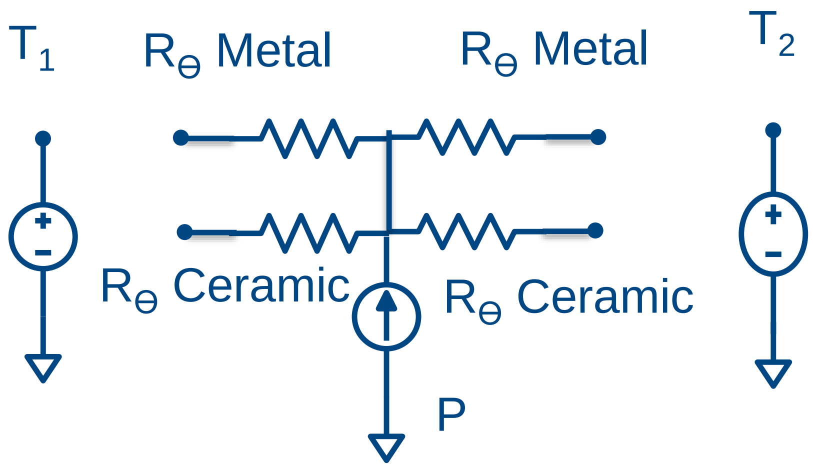
A = cross sectional area W * T

When L=W
R_Θ per square is 1/(K*T)



An effective K was computed for active region from the parallel combination of R_Θ per square of Nickel and $CaZrO_3$ for the number of electrodes and actives in MLCC

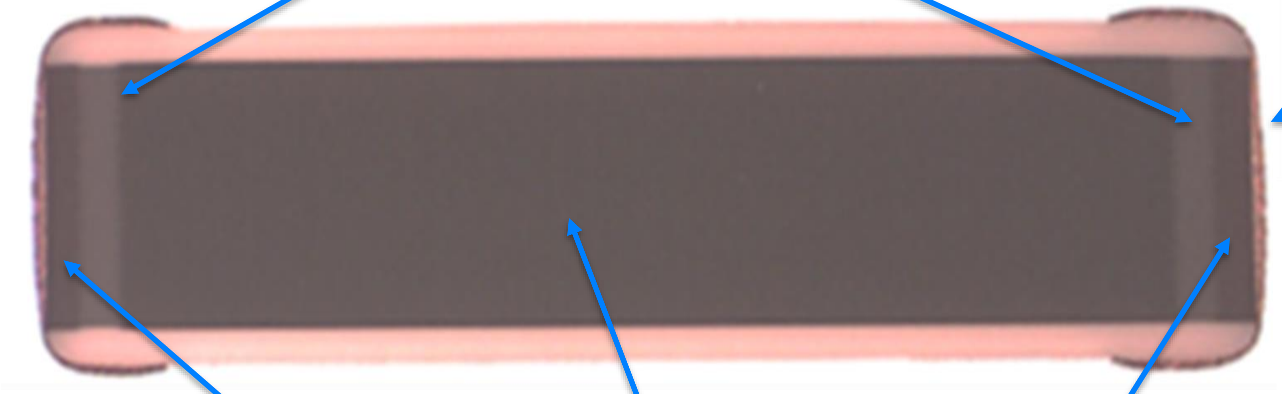
P is Dissipated Power (Heat)



	K(Watts/(°C*m)	T (m)	R_Θ per square (°C/Watt)
Nickel	90	1.2e-6	9.26E+03
$CaZrO_3$	3.0	1.27e-5	2.62E+03

Thermal Conductivity Regions

Region C alternating electrodes 1 per active

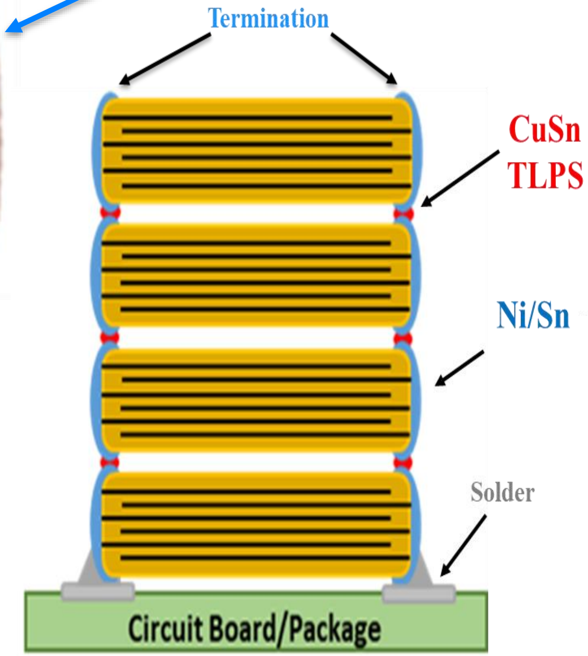


Region A and B 2 electrodes per active

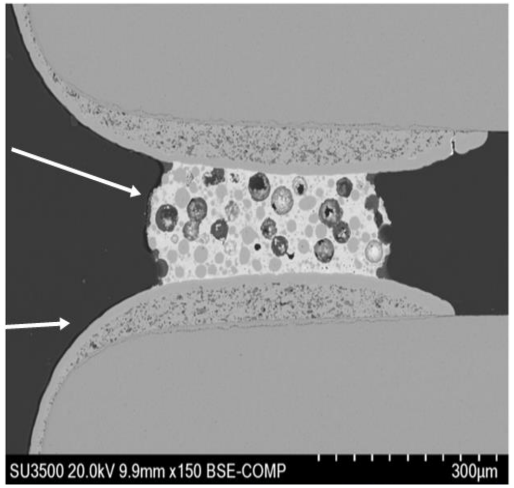
Region D Ceramic top, bottom and side margins

Transient Liquid Phase Sintered (TLPS) bond in stack

Region E Terminations

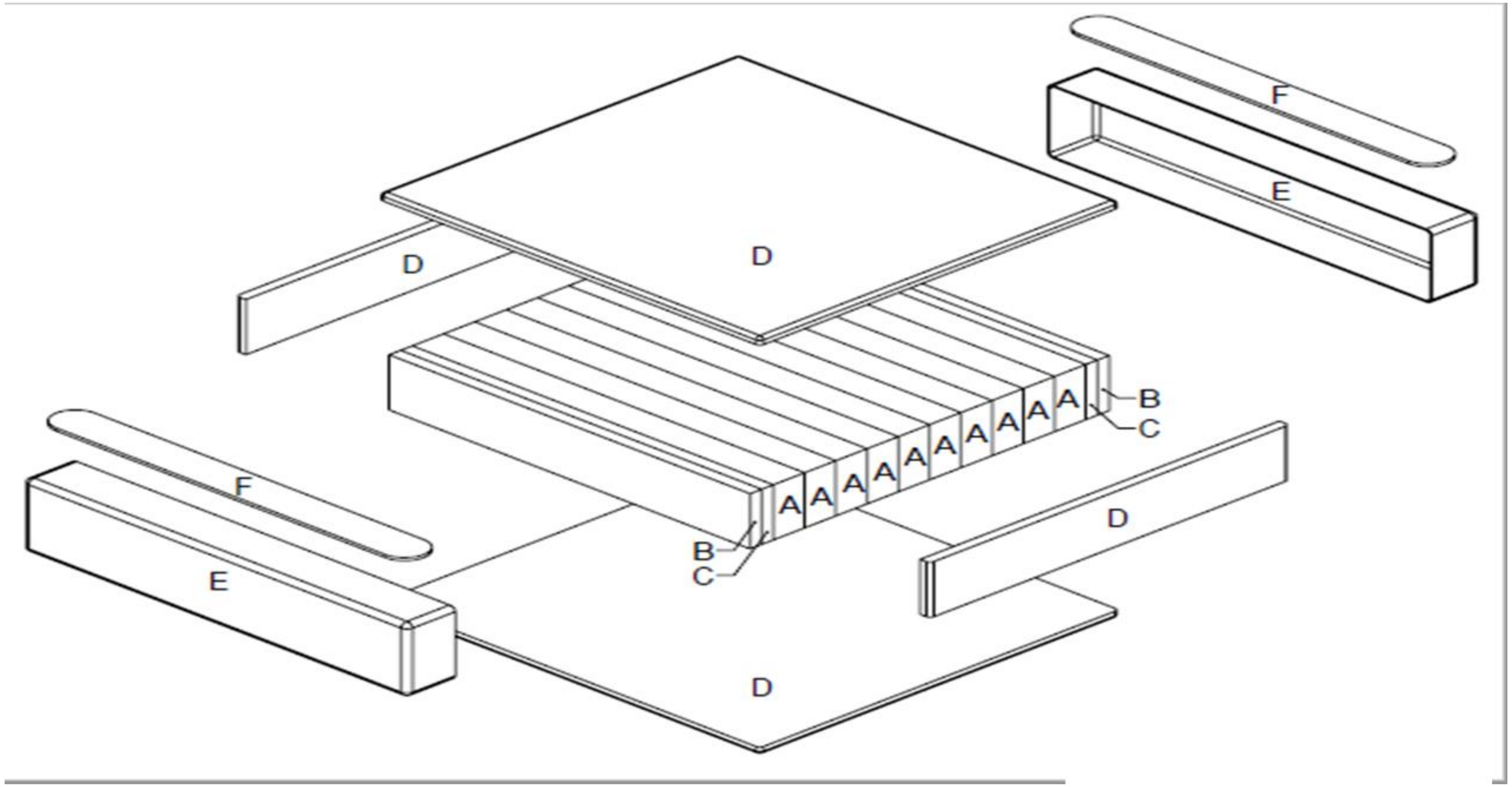


Region F TLPS



Solid Works FEM Model

The model was excited with 10 distributed 0.1 Watt heat sources in Region A based on method presented at 3D PEIM. [3]

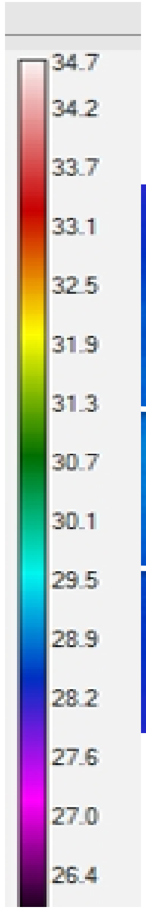


Region	Effective Thermal Conductivity K (Watts/°C*m)
A	10
B	10
C	7
D	3
E	47
F	26.8

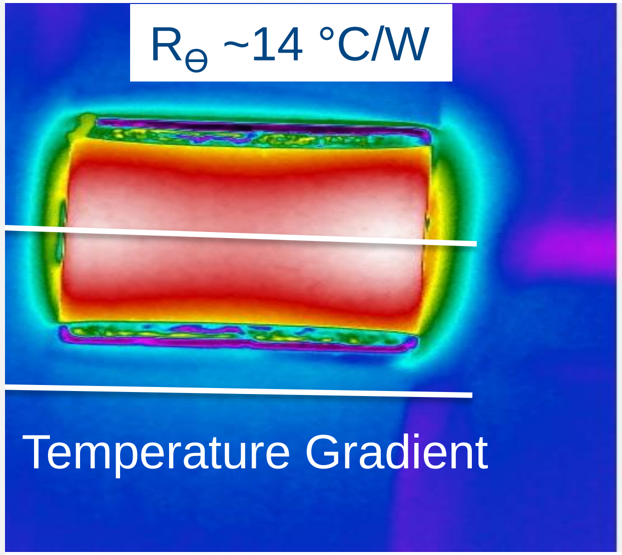
3. ‘Thermal Models of Multilayer Ceramic Capacitors for 3D Power Electronics’, Allen Templeton 3D-PEIM 2018

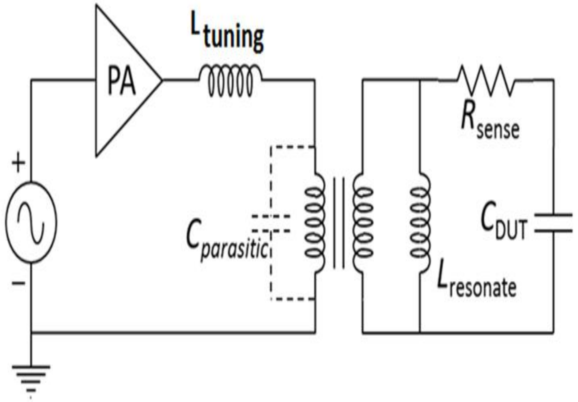
FEM Model of MLCC in Still Air

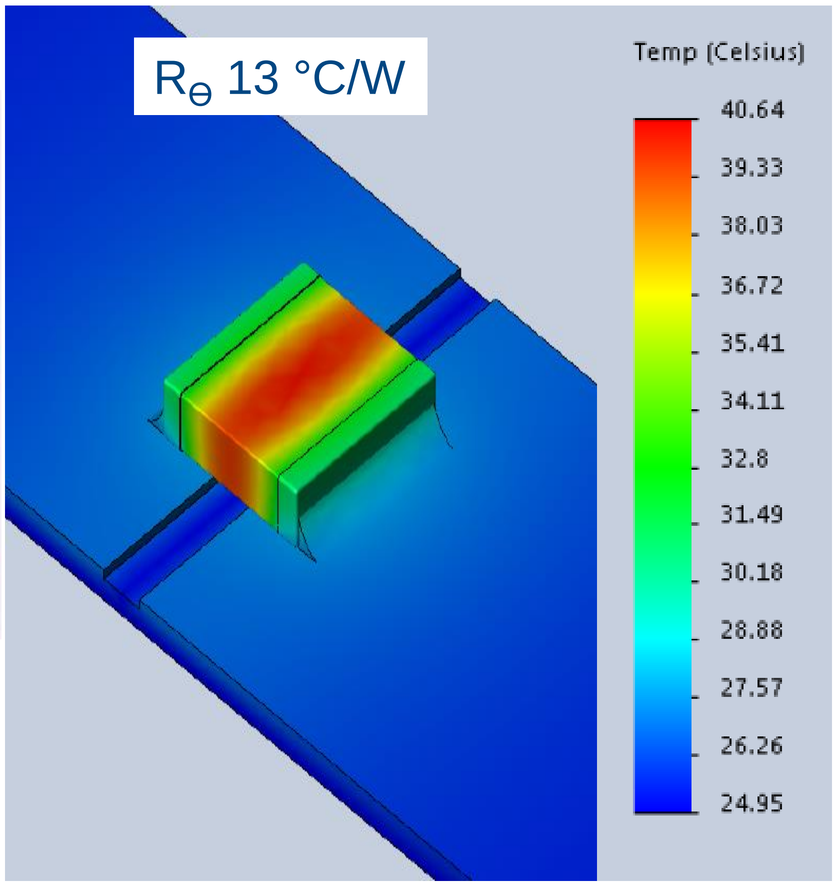
The traditional MLCC model R_{Θ} matches previous measurements the low loss R_{Θ} result is much higher

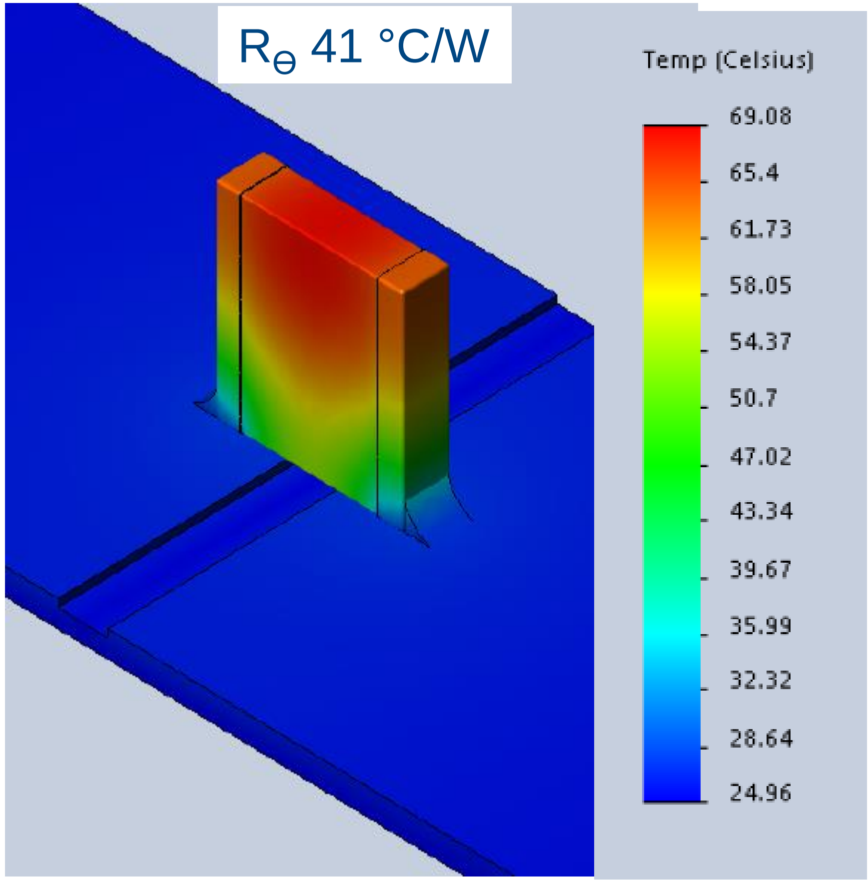


Previous Measurements



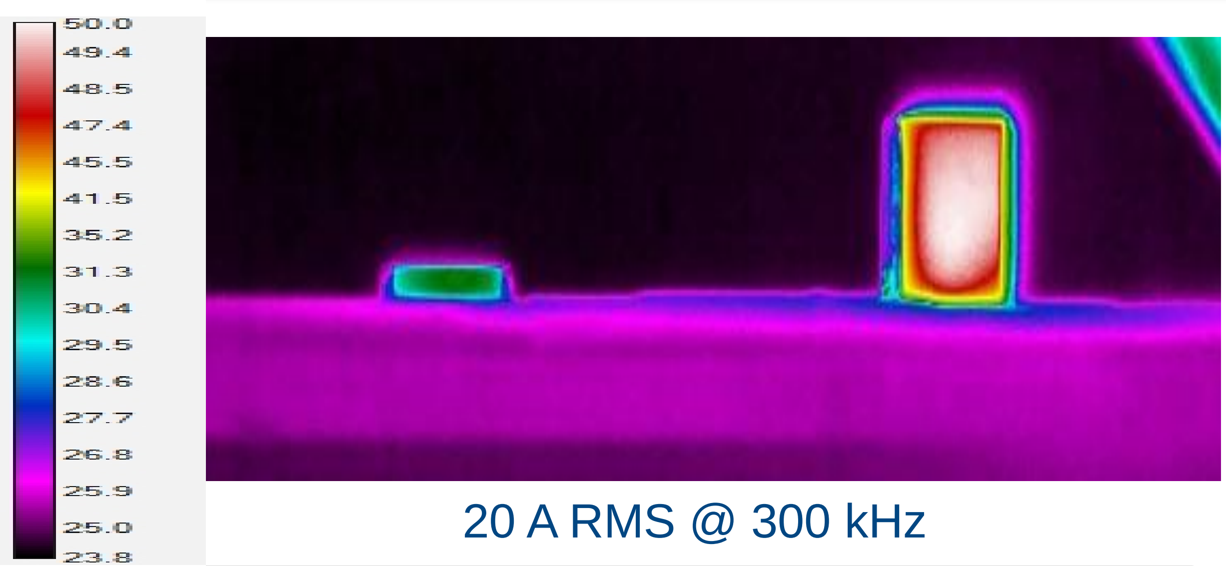




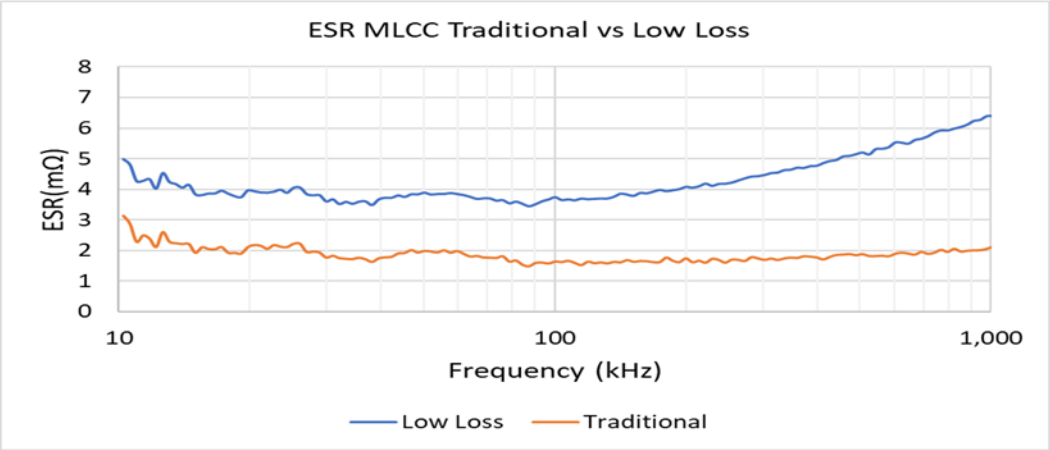


MLCCs modeled on 5 oz copper FR4 with low R_{Θ} heat sink like measurements

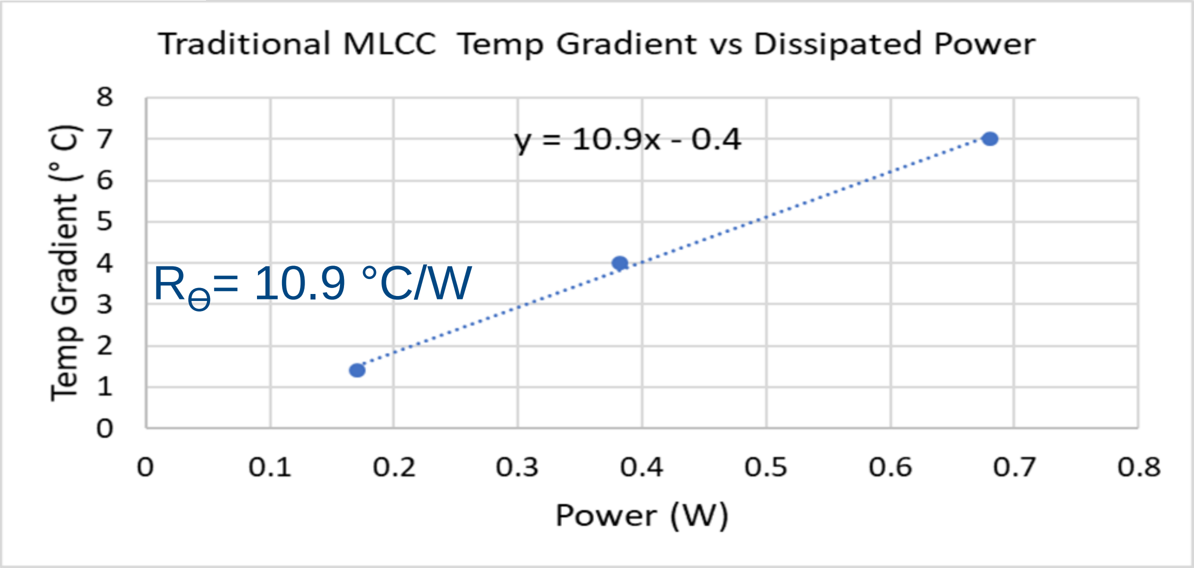
ESR and R_θ for MLCC

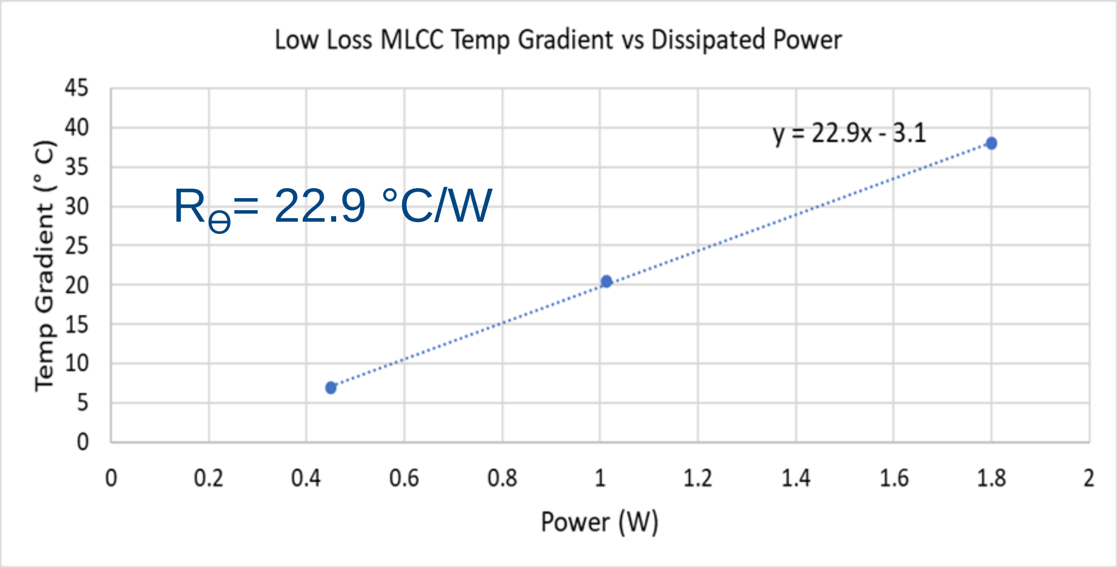


20 A RMS @ 300 kHz



Dissipated Power = I^2 x ESR(mΩ)/1000

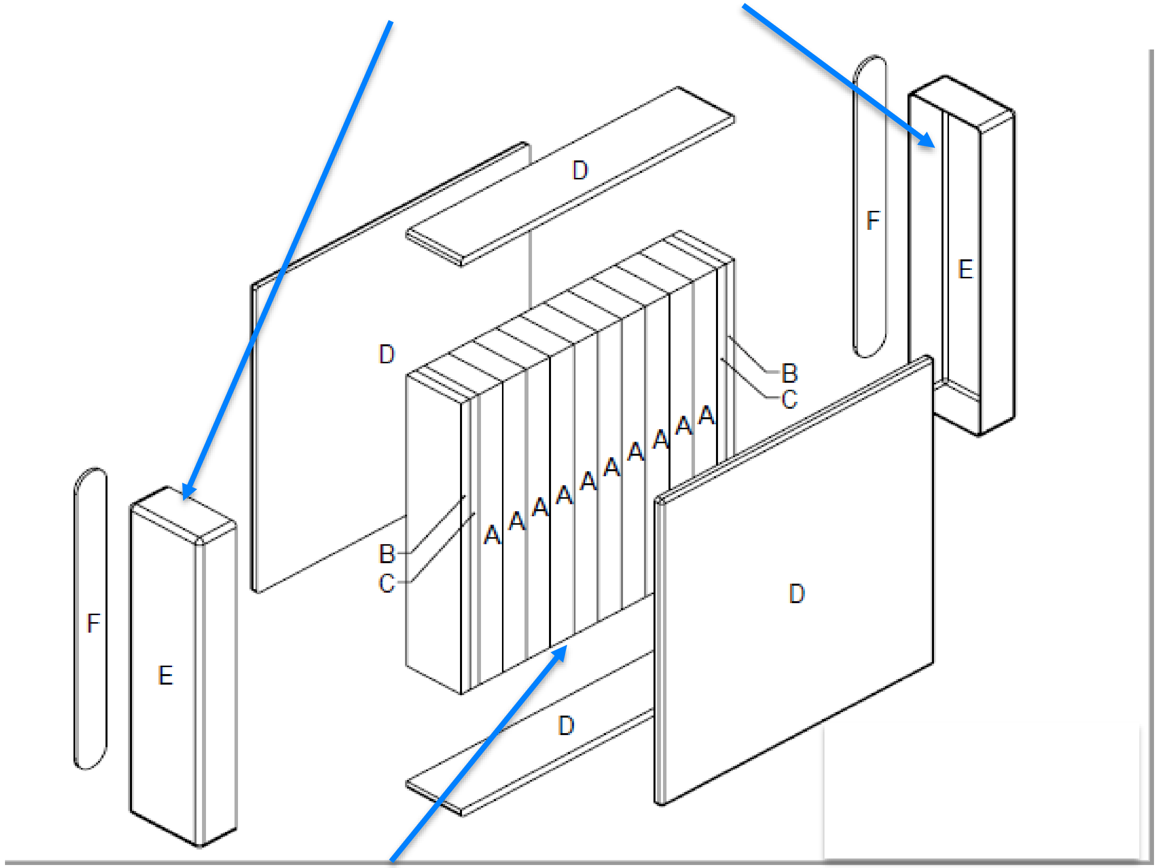




New Low Loss Model has 50 % of Heat generated in termination and 50 % inside MLCC to match measured ESR increase.

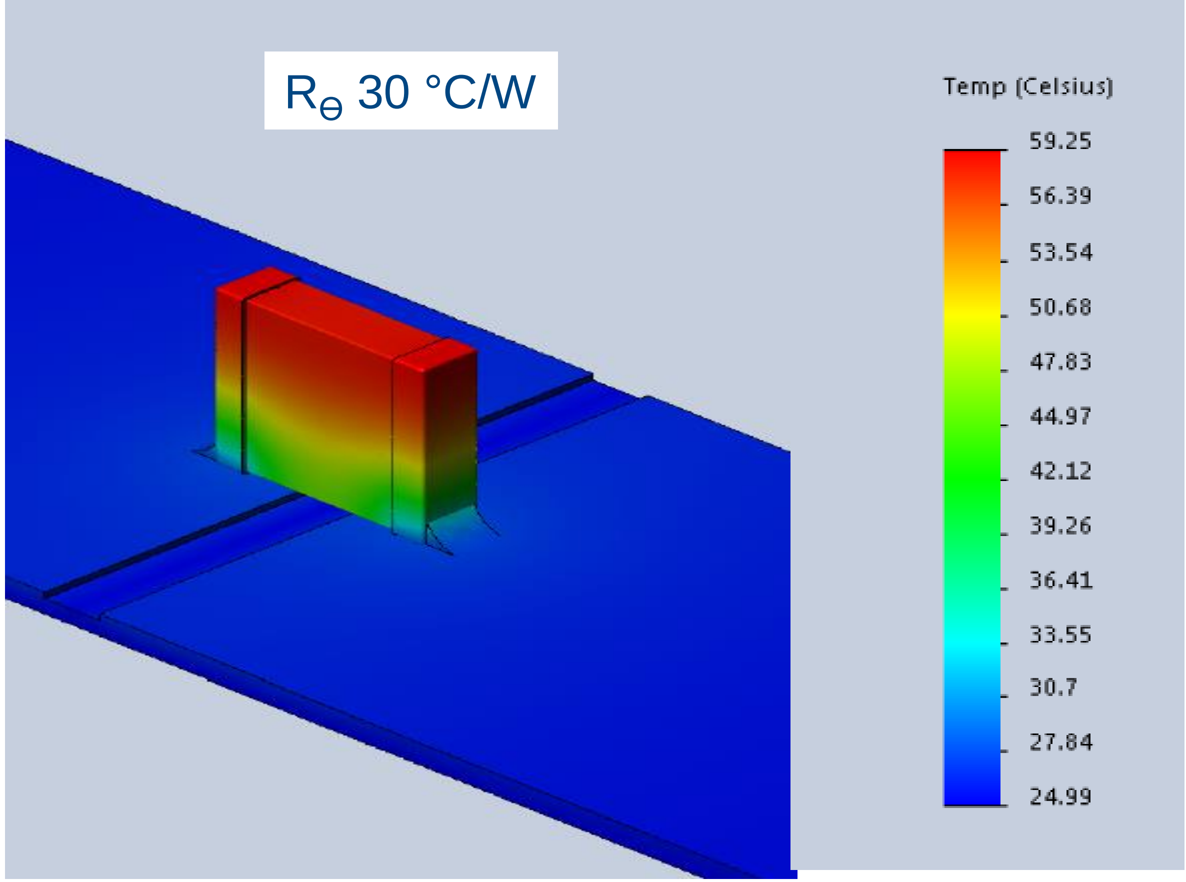
Electronic Components KEMET CHARGED®

0.25 W distributed heat source in each termination

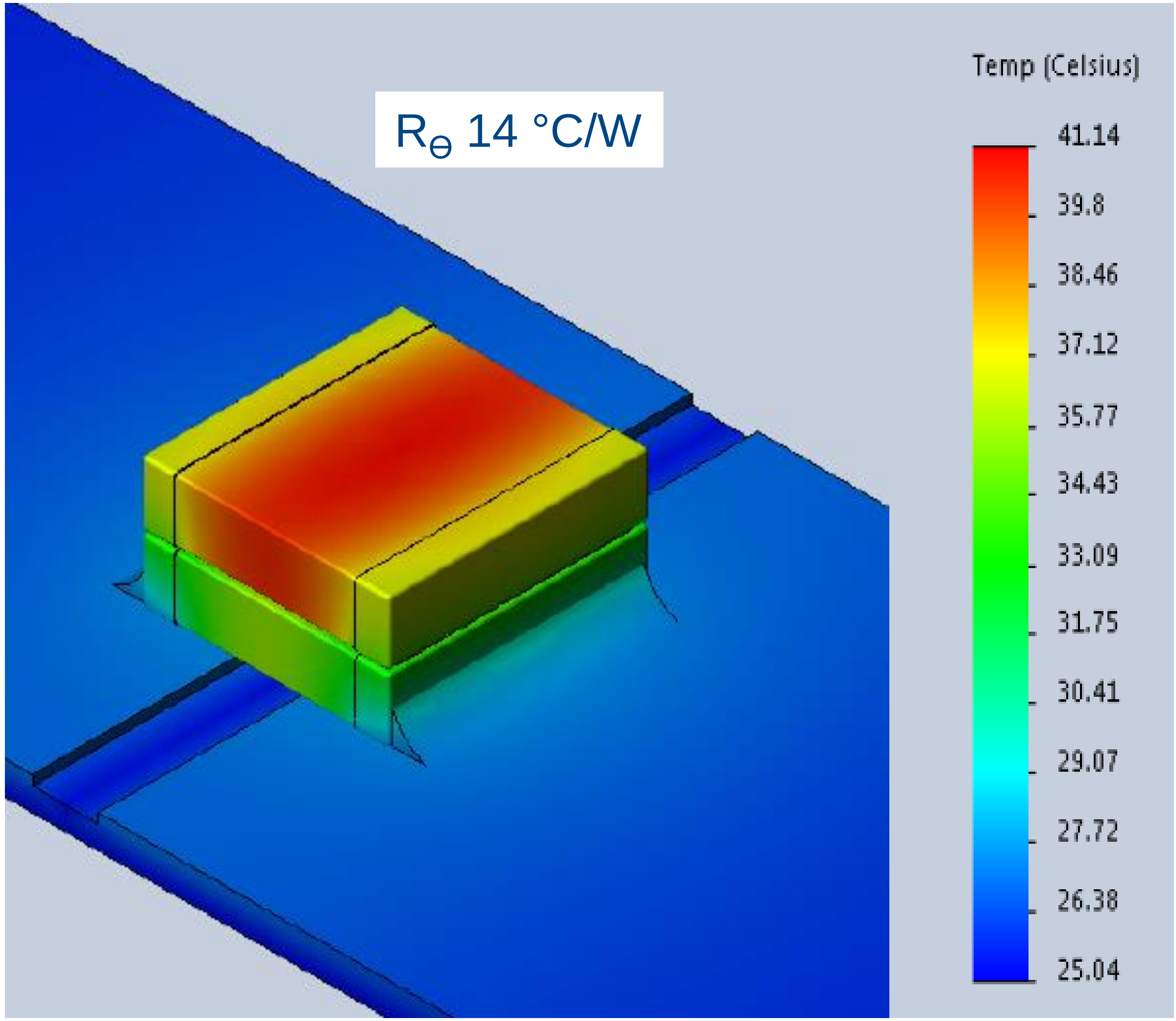


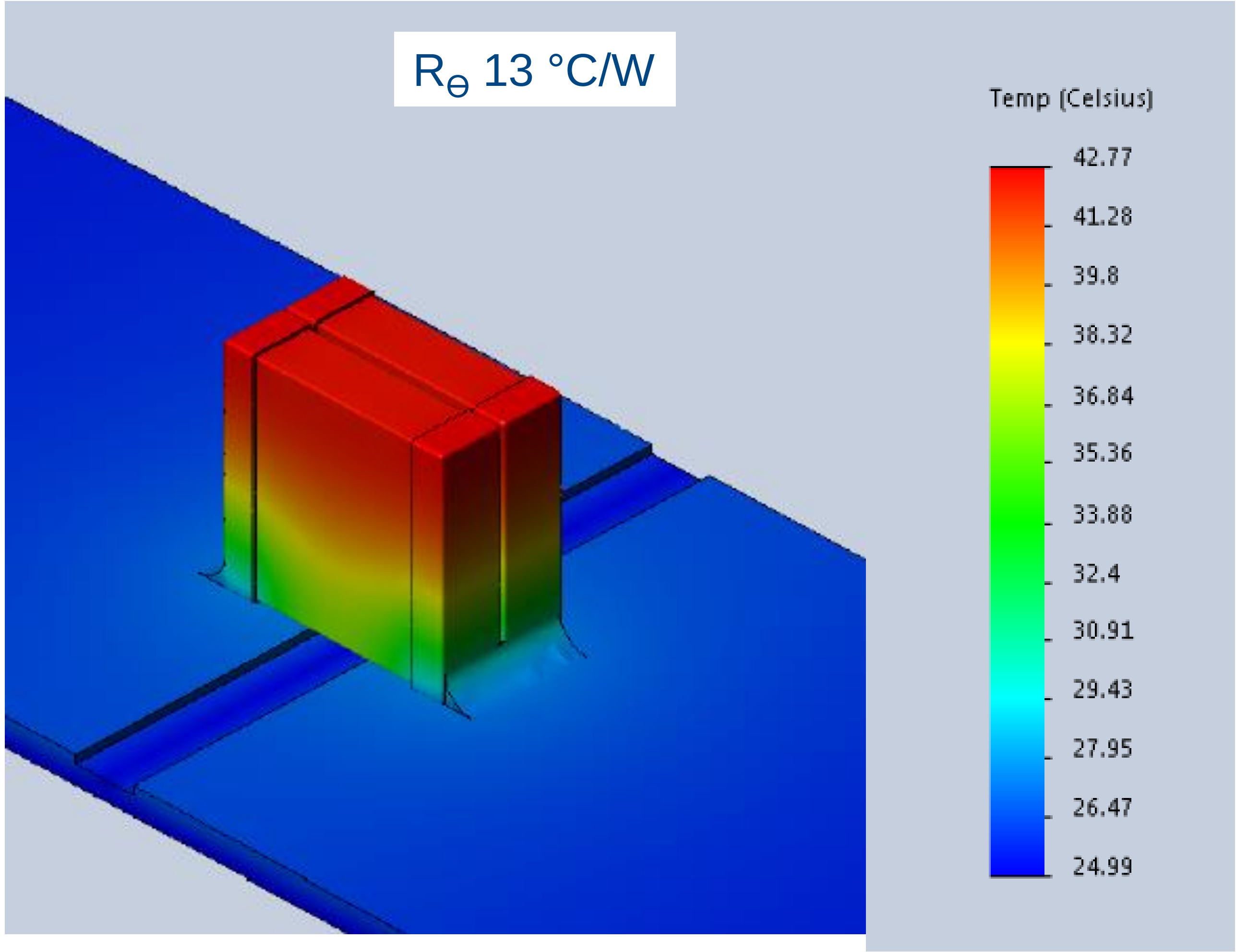
The model now has 10 distributed 0.05W heat sources for a total of 0.5 W inside MLCC

Max Temperature gradient is reduced by 11 °C

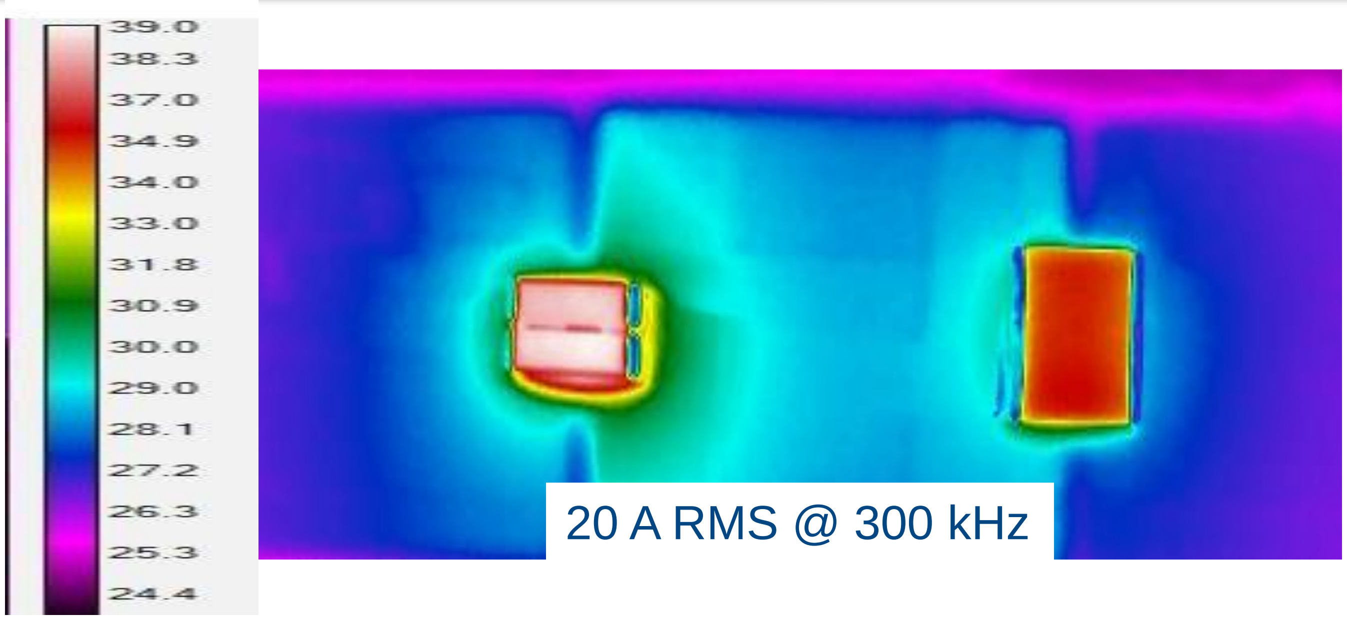


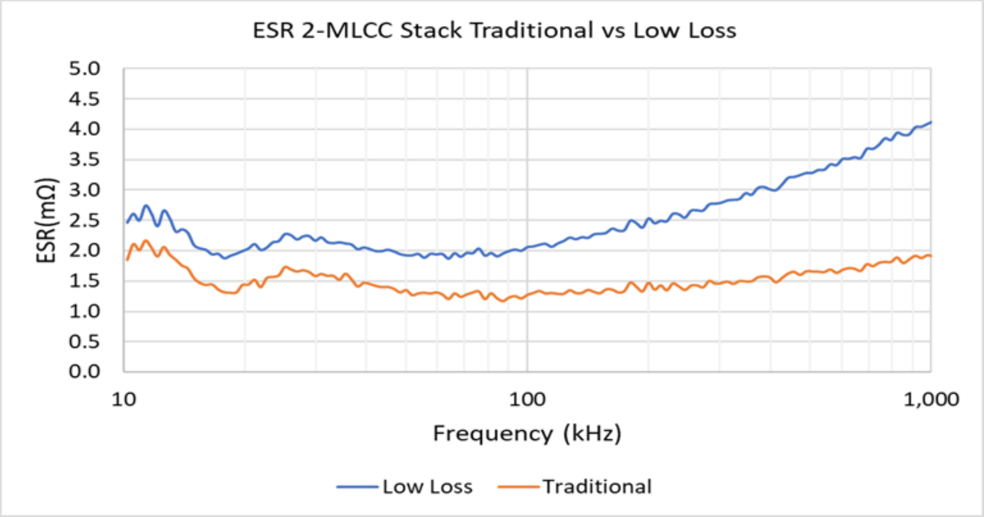
2-MLCC Stack Traditional and Low Loss Orientations

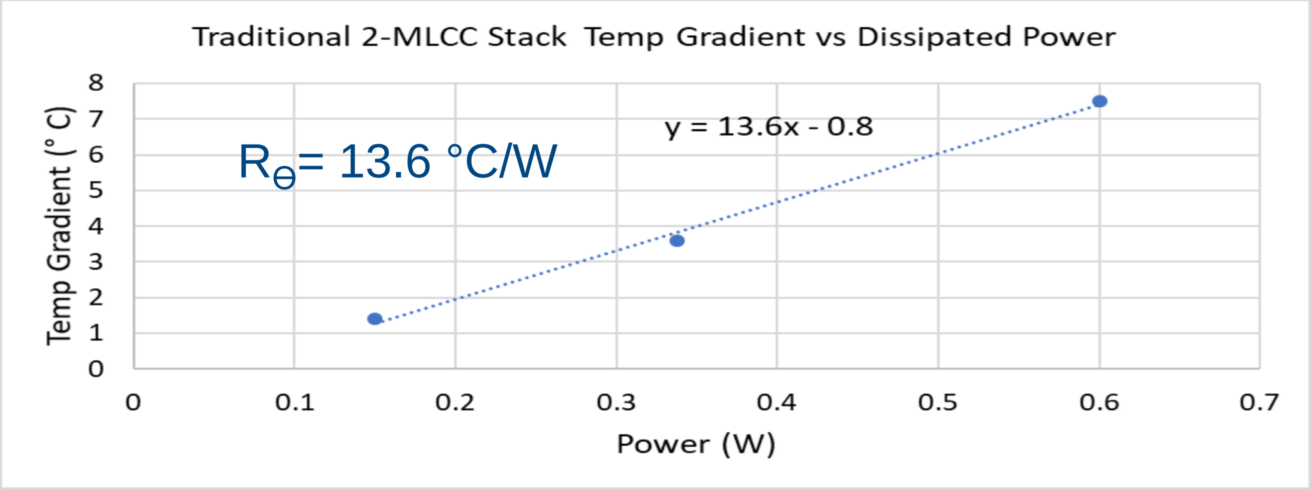


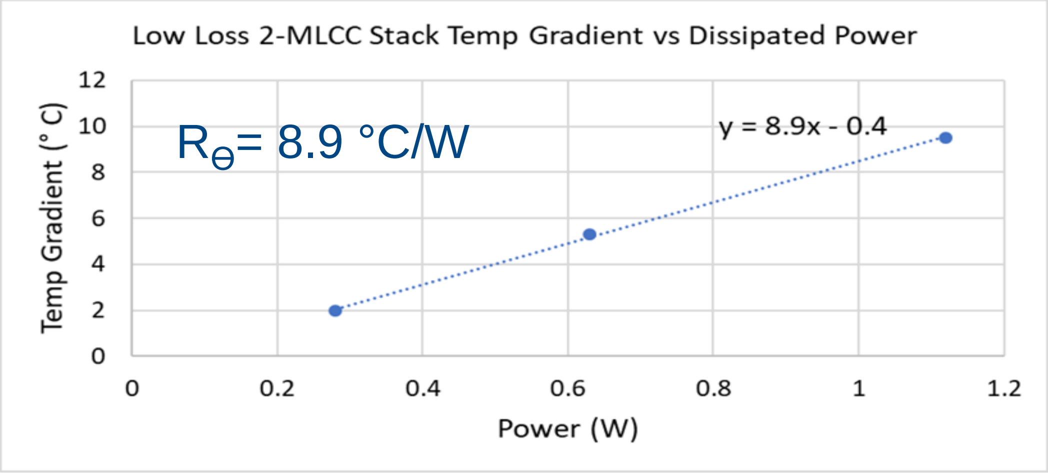


2-MLCC Stack Experimental Results

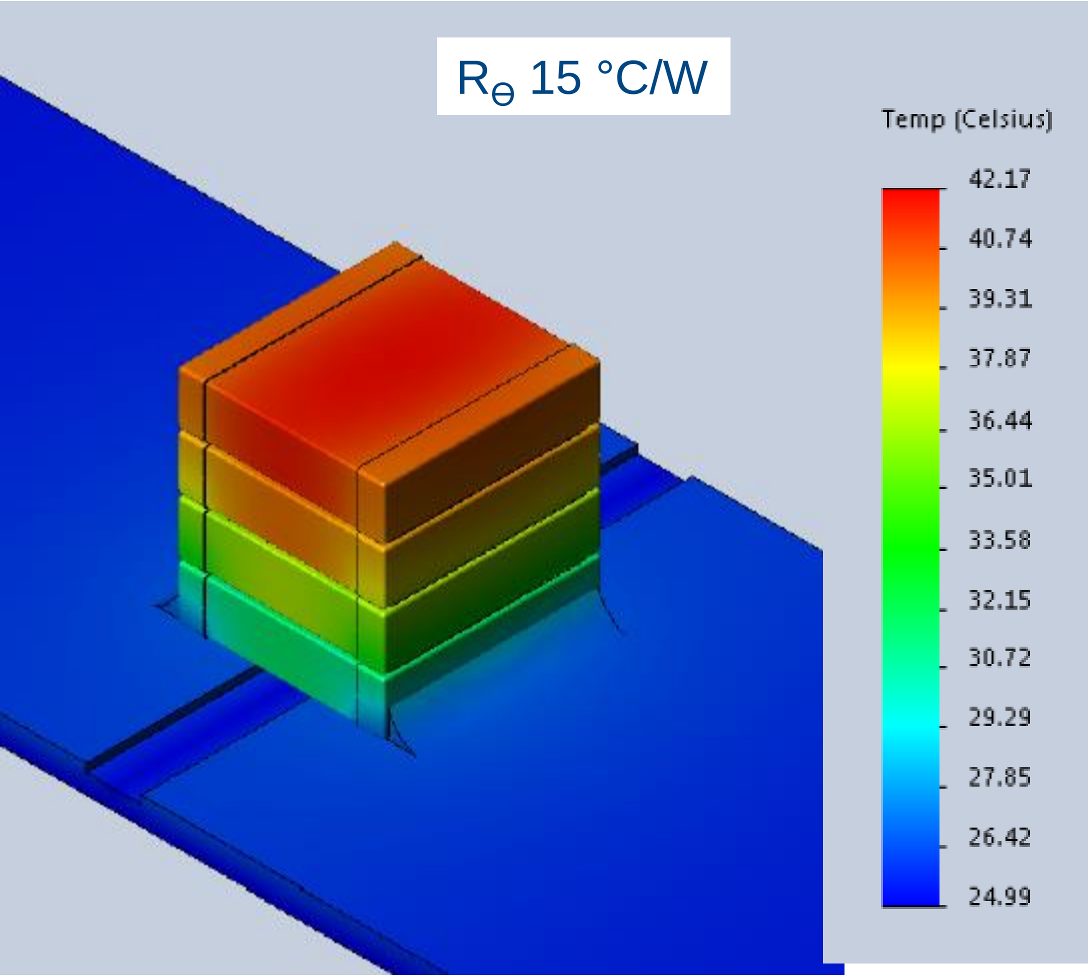


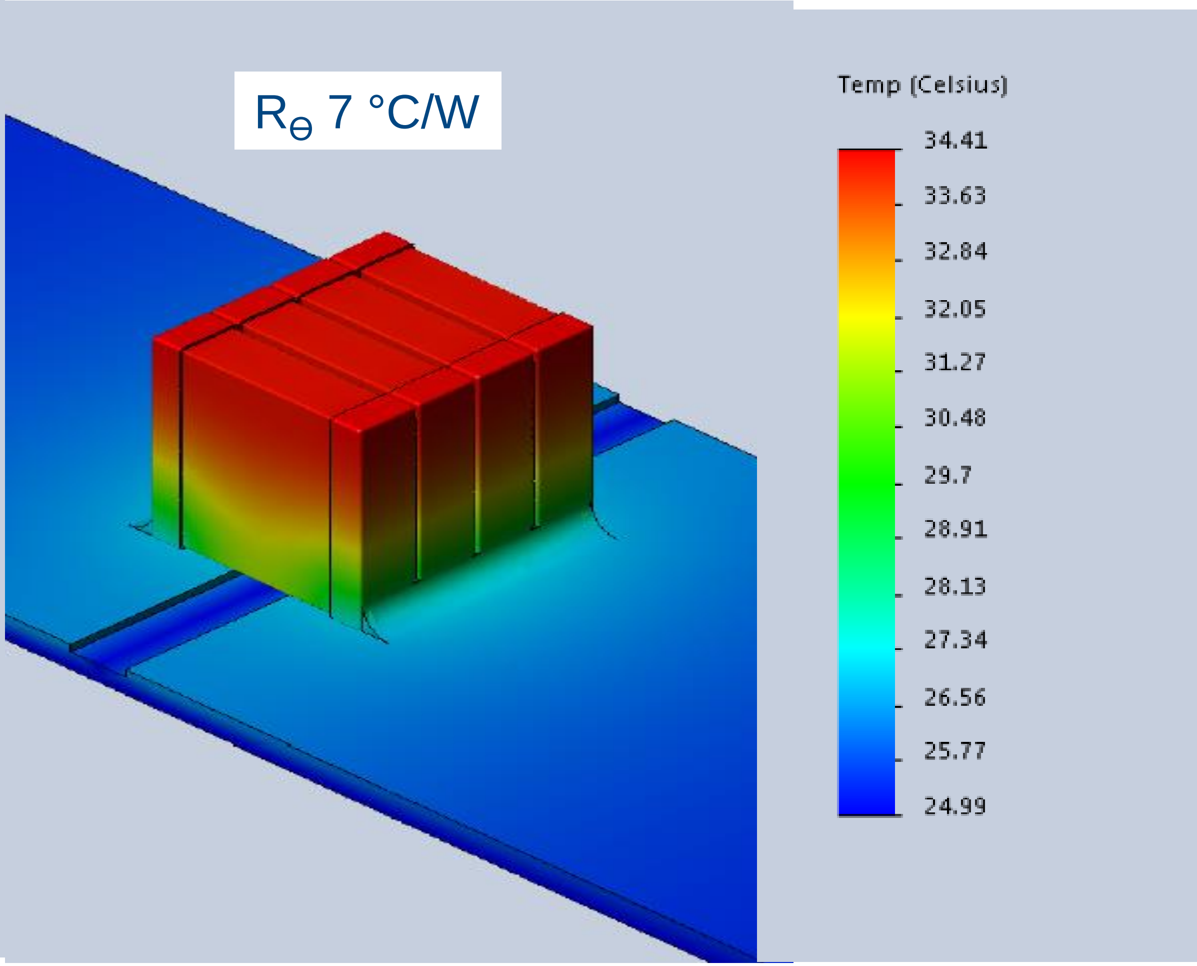




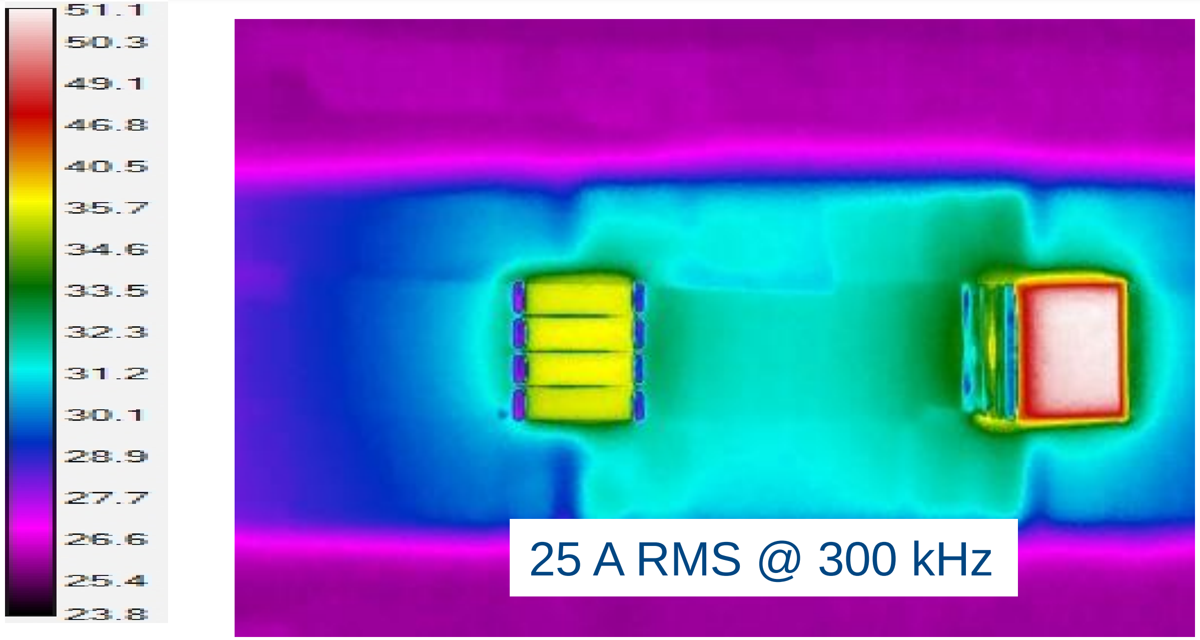


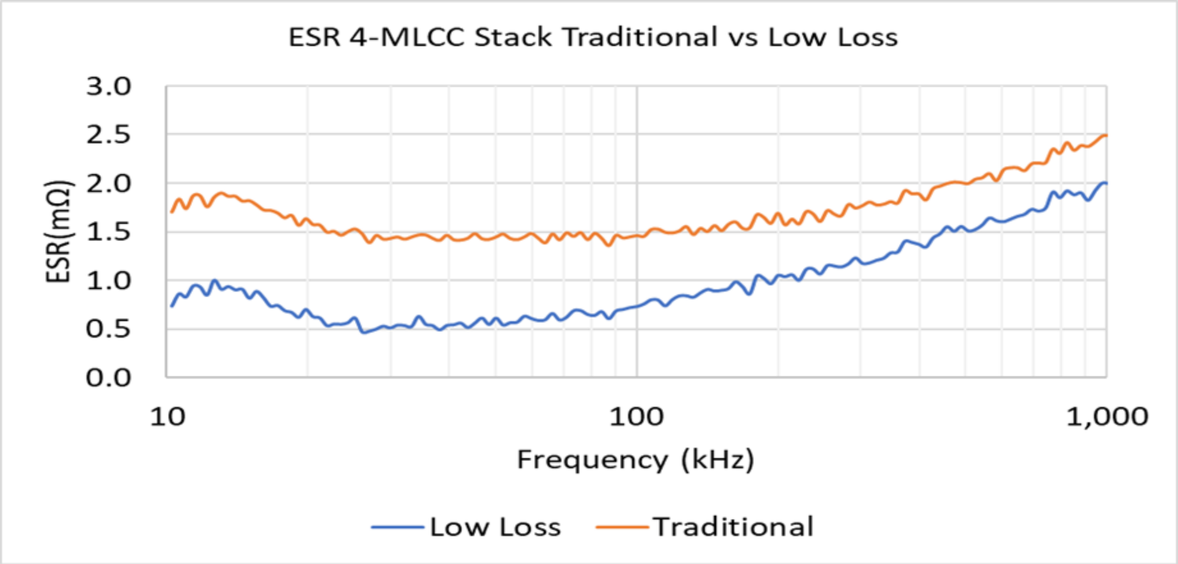
4-MLCC Stack Traditional and Low Loss Orientations

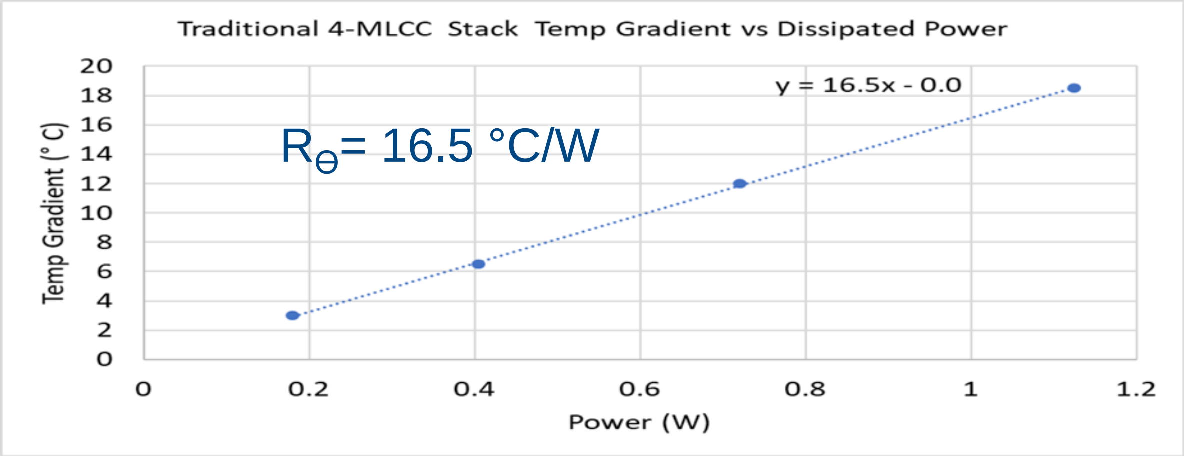


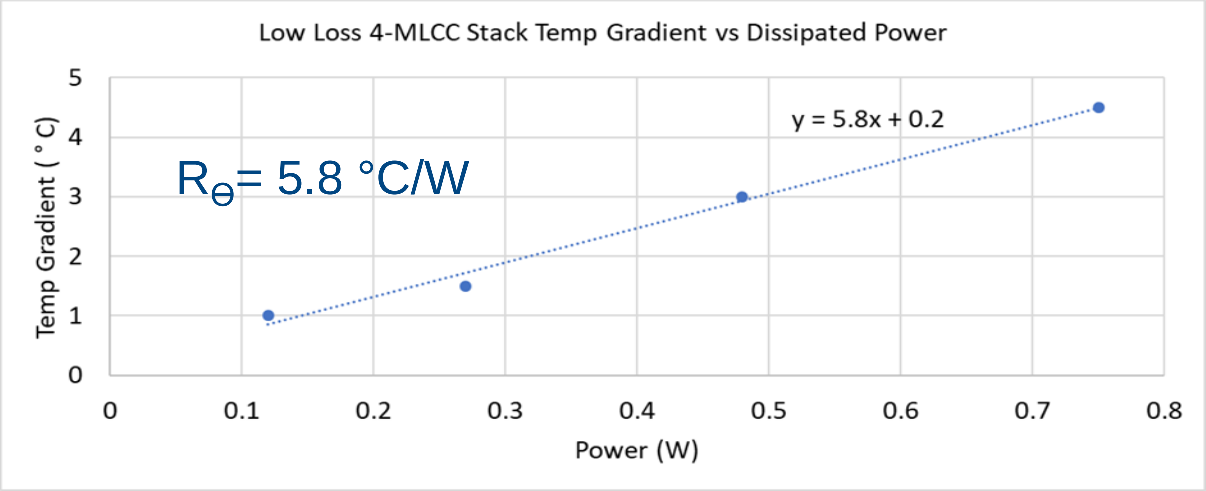


4-MLCC Stack Experimental Results





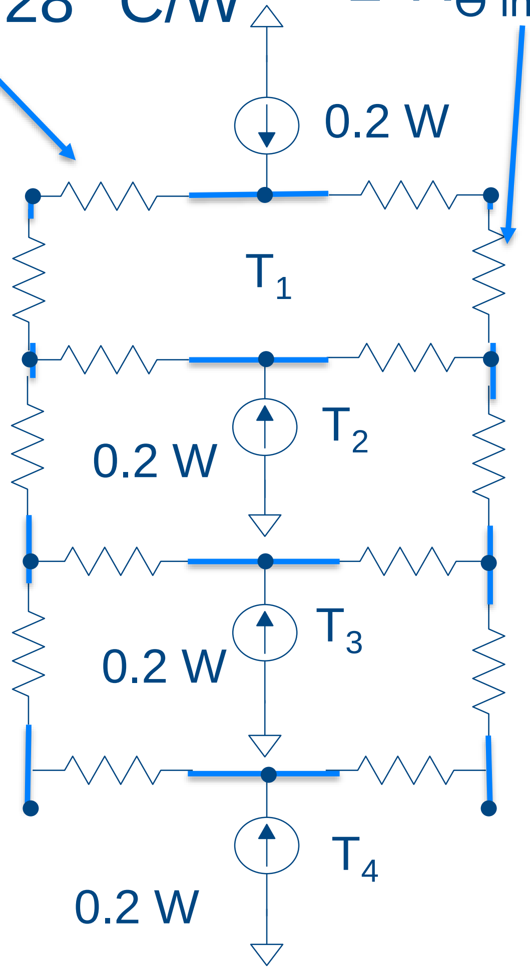




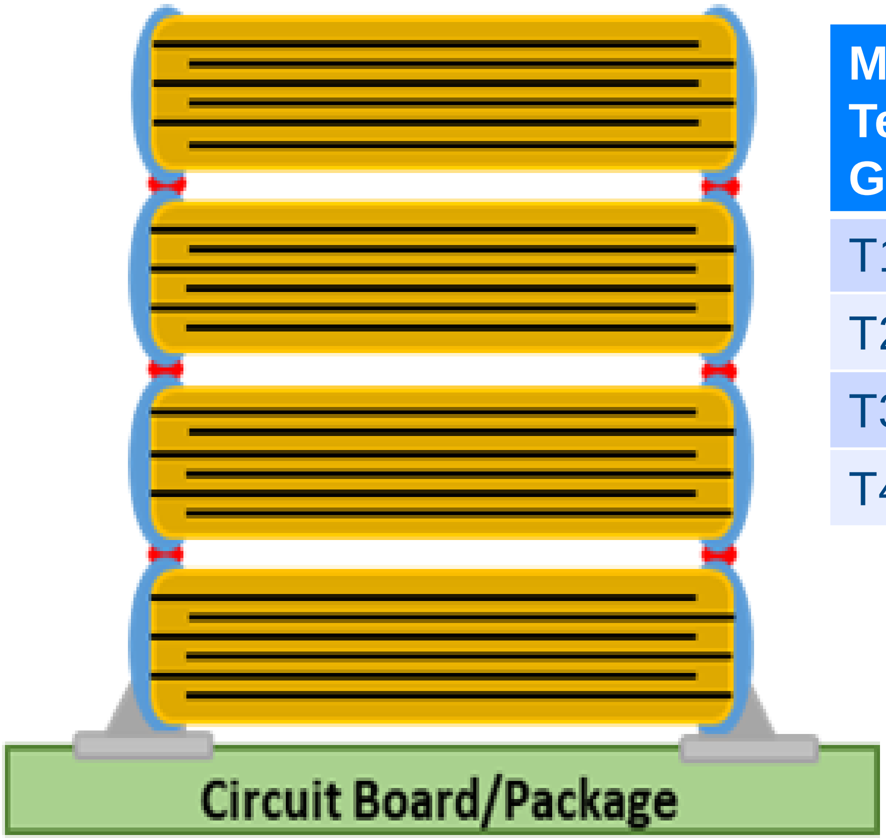
Thermal Network 4-MLCC Stack Traditional Orientation.

$R_{\Theta\ interconnect}$ was estimated from LTspice parameter sweep to match MLCC Temperatures T_1 to T_4

$2^*R_{\Theta\ mlcc}$ ~ 28 °C/W $2^*R_{\Theta\ interconnect}$ ~14 °C/W



@ 20 A RMS Total Dissipated Power was 0.8 W ~ 0.2 W per MLCC



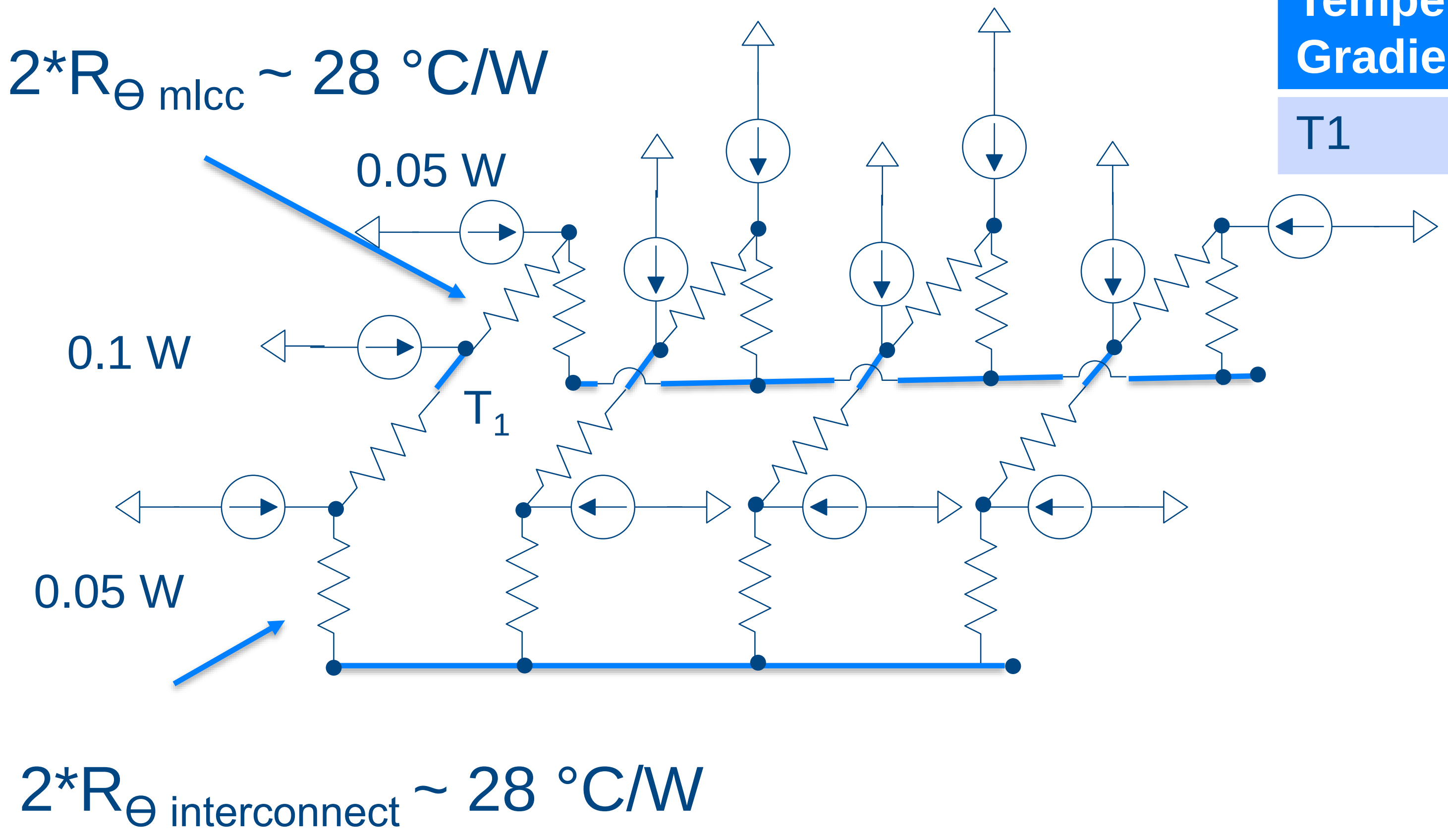
MLCC Temperature Gradient	Spice °C	Measured °C
T1	11.2	10
T2	9.8	10
T3	7	8
T4	3	3

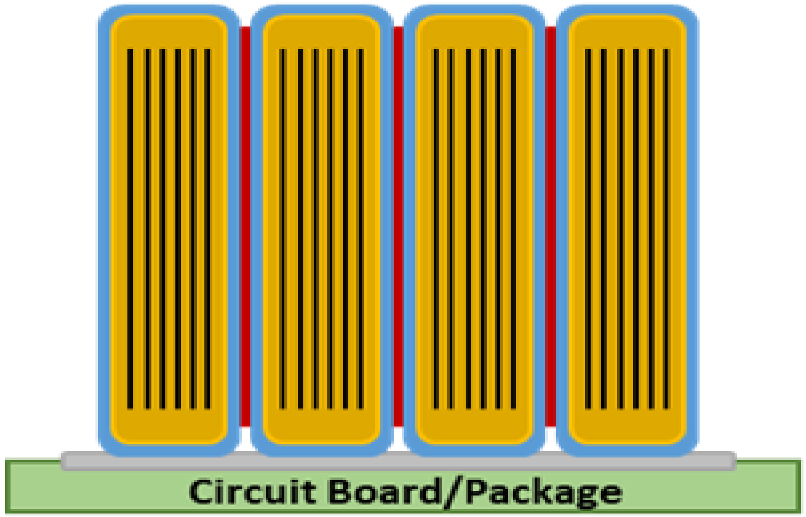
Thermal Network 4-MLCC Stack Low Loss orientation

$R_{\Theta\ interconnect}$ was estimated from LTspice parameter sweep to match MLCC Temperature T_1

@ 25 A RMS Total Dissipated Power was 0.8 W ~ 0.2 W per MLCC

MLCC Temperature Gradient	Spice °C	Measured °C
T1	4.3	4.5





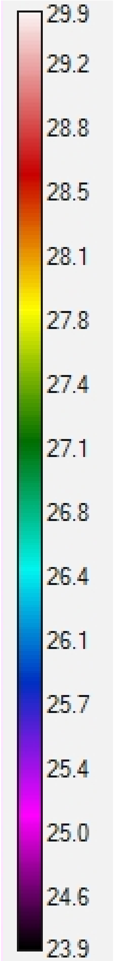
Conclusions

- Adding MLCCs in the Low Loss orientation stack reduces the electrical and thermal resistance.
- The interconnect increases the thermal and electrical resistance in traditional orientated stacks as more MLCCs are added.
- This modeling approach for MLCCs and leadless stacks will be used to optimize the thermal performance of other case size MLCC leadless stacks.
- The more complex thermal networks developed for leadless MLCC stacks will be used to study how the stacks perform in high density power supply designs.

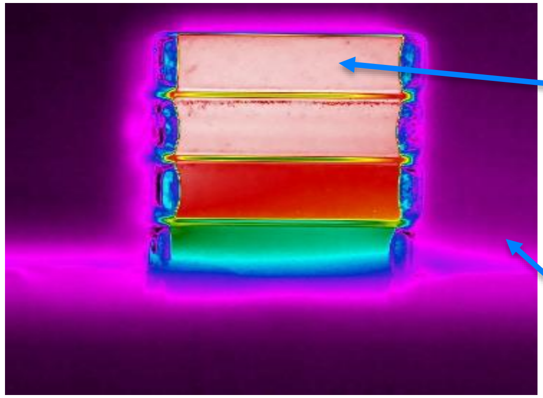
Low Loss Orientation	ESR Measured (mΩ) 300 kHz	R_{Θ} Modeled/ Measured (°C/W)
MLCC	4.5	30/22.9
2-MLCC	2.8	13/8.9
4-MLCC	1.2	7/5.8

Traditional Orientation	ESR Measured (mΩ) 300 kHz	R_{Θ} Modeled/ Measured (°C/W)
MLCC	1.7	13/10.9
2-MLCC	1.5	14/13.6
4-MLCC	1.8	15/16.5

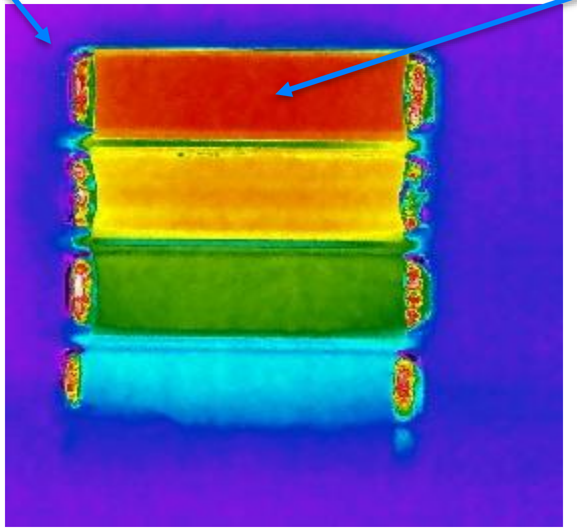
Future Work

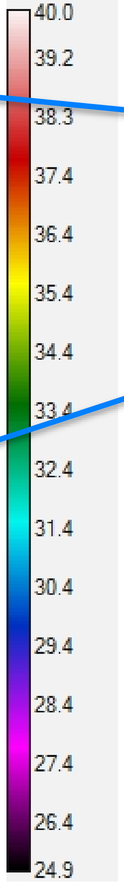


Time = 0

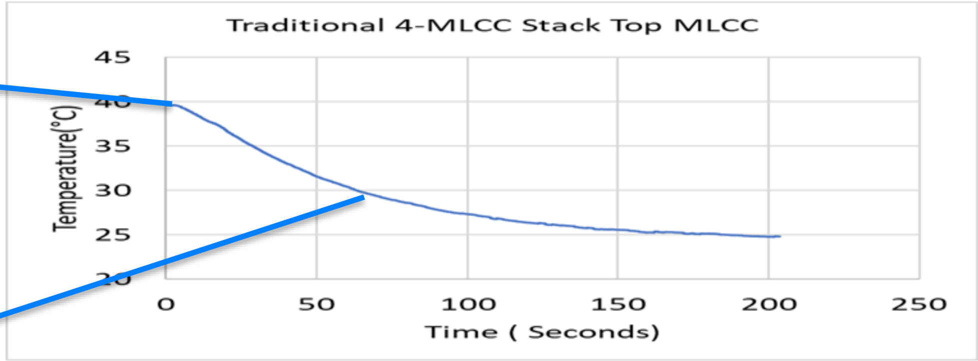


Time ~ 60 seconds





Measured Thermal Decay of Top MLCC in 4-MLCC Traditional Stack



- Compare FEM transient thermal response of leadless stacks to measurements.
- Model current flow in interconnect to better define heat source in termination.
- Study thermal resistance with other boundary conditions
  - Forced air cooling or dielectric fluids
  - Embedded in package

Thank You!

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