ADVANCED MATERIALS, DESIGNS AND 3D PACKAGE ARCHITECTURES FOR NEXT-GEN HIGH-POWER PACKAGING

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3D SYSTEMS PACKAGING RESEARCH CENTER

CREATING THE NEXT®

Outline

- Why 3D for Next-Gen SiC Packaging?
- Innovations in Package Design & Materials
- Summary

3D Systems Packaging Research Center at Georgia Tech

- Comprehensive global Industry Consortium in System Scaling to enable supply-chain manufacturing to end-user needs
- Industry culture and R&D infrastructure (300mm clean room facility)

Plating Facility

Substrate Cleanroom

Assembly Facility

Environmental Testing

Shared User Labs

Strategic Need: Packaging Solutions *FOR* WBG

- Electrical power needs are increasing across the transportation field

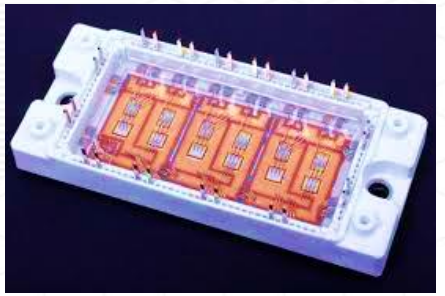
- Shift from Si to SiC with higher voltage/power ratings, switching speeds, max. junction temperatures in smaller footprint

Power ↑ + Size ↓
=
Temperature ↑

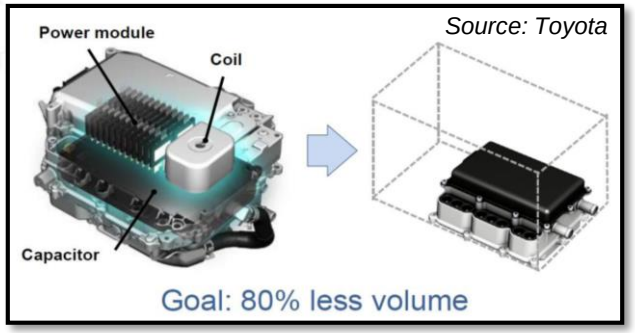
… but power packaging is slow to change and is now limiting the performance of power electronics

We need power electronics packaging AND cooling to catch up to the devices capability

Current SiC power module

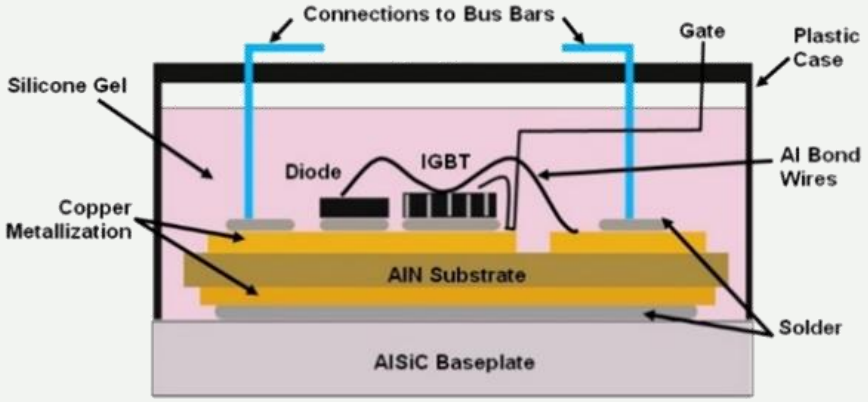


↑ capacity, ↑ efficiency, ↓ cost



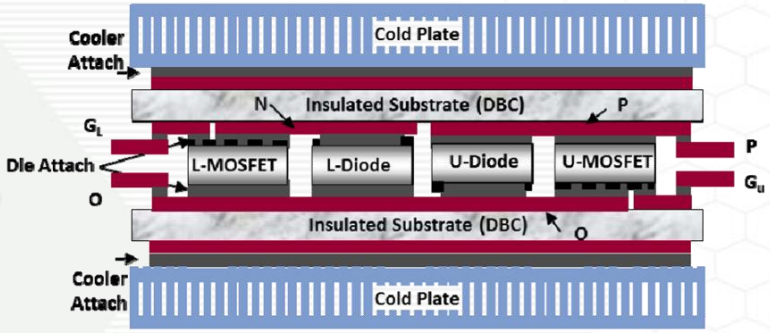
Evolution of Power Packaging Technologies

Conventional Power Module



Wire bonds, Single-side cooling, Separate power / control / drive integration

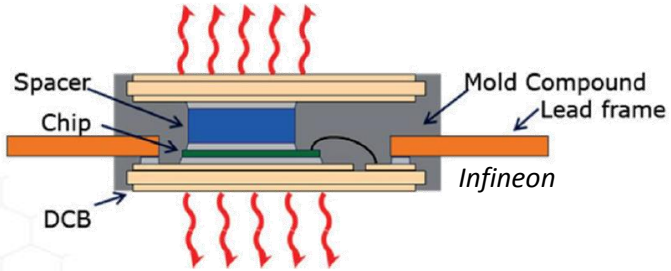
3D Power Package



Oakridge Nat. Lab.

Elimination of bond wires, Double-sided cooling, Scalability in power

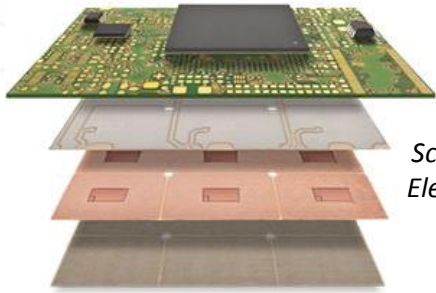
Molded Power Cards



Leadframe-based, Cu clip package, Low-cost

Modularity vs. Integration

Power Embedding



Schweizer Electronics

Heterogeneous integration, PCB-based processing

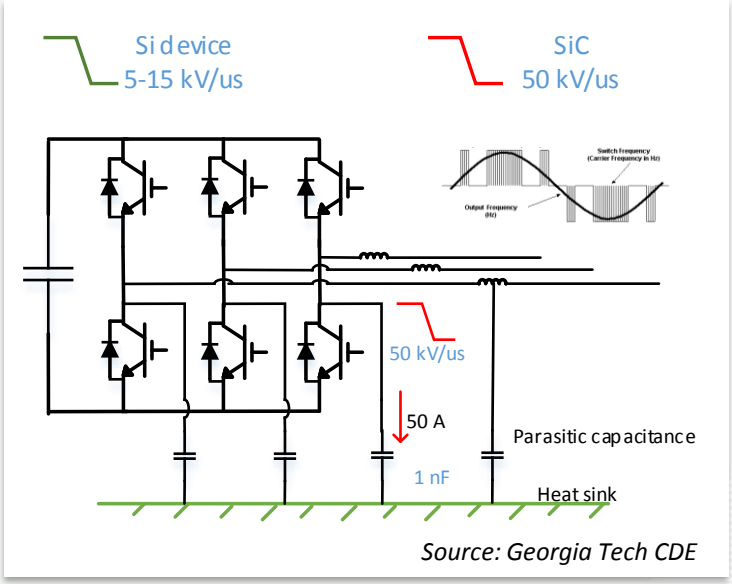
Packaging Trends:

- ↓parasitic L, ↑reliability, ↑thermal behavior
- Leverage more standardized manufacturing

New solutions required to fully benefit from performance improvements of SiC

Transition from Si to SiC… the “dv/dt” challenge

- Fast rise and fall times of SiC devices result in high dv/dt
  - Common mode currents
  - EMI
  - Complex gate driver

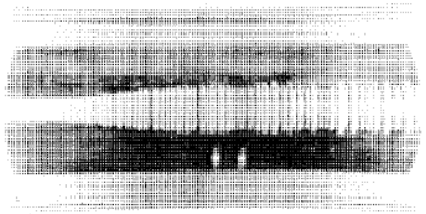


Source: Georgia Tech CDE

Package parasitic capacitance plays a critical role in dv/dt capability

- Common mode currents can lead to electrical discharge machining (EDM) on ball bearings, will be worse with SiC

Image of ball bearings in motor with voltage source converter

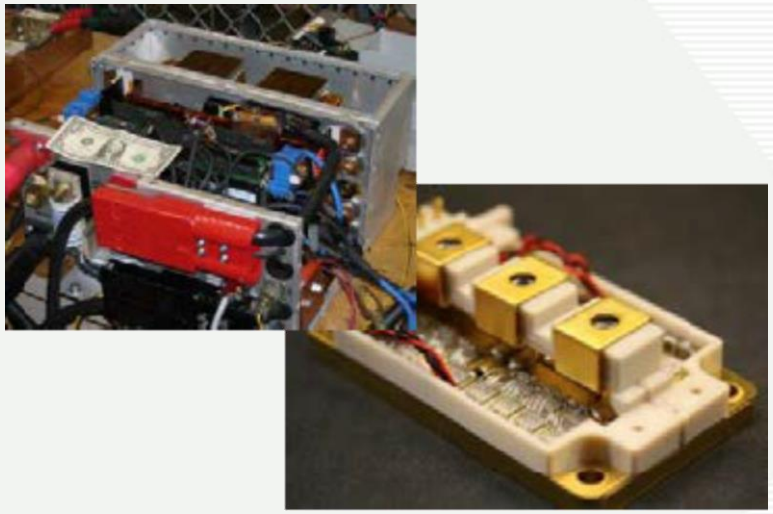


*Doyle Busse, Jay Erdman, Russel J. Kerkman, Dave Schlegel, and Gary Skibinski, “Bearing Currents and Their Relationship to PWM Drives “ IEEE IECON, 1995

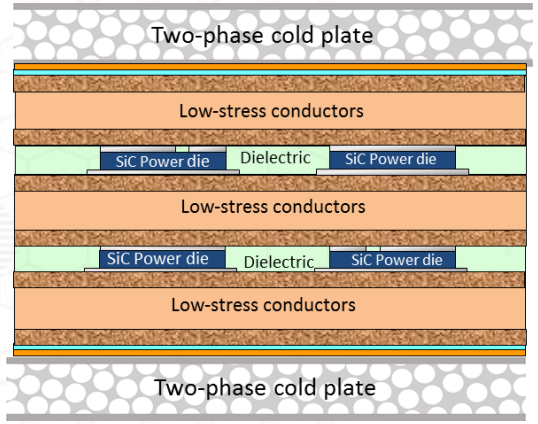
- Two ways to solve the problem: topology, **packaging**

What we can do on packaging side to address the transition to SiC

Conventional Packaging



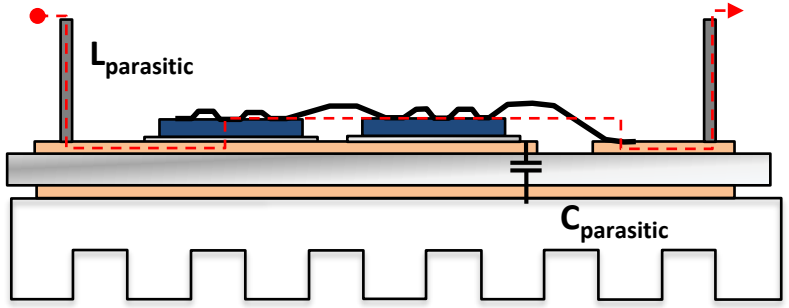
PRC's Solution: 3D Power Package with Die Stacking



Parameters	Current Packaging Solutions	Our Targets
Heat Flux	200W/cm^2	1kW/cm^2
Breakdown Voltage	10kV	>30kV
Max. Junction Temperature	150-175°C	>200°C
Thermal Performance	No thermal transient control	Thermal transient suppression
Reliability	Poor at full device rating	Improved

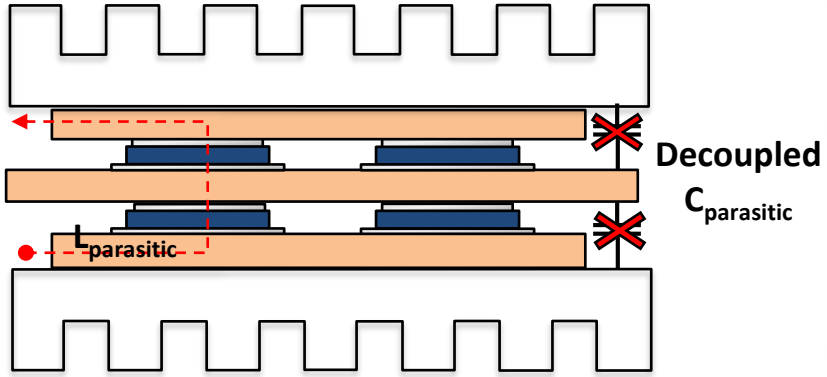
Beyond Traditional 3D: Die Stacking

Electrical



Minimum Parasitic inductance

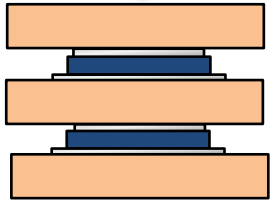
Decoupled Parasitic capacitance

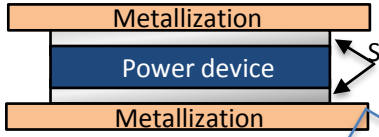


10X ↓ parasitic C with <1nH parasitic L

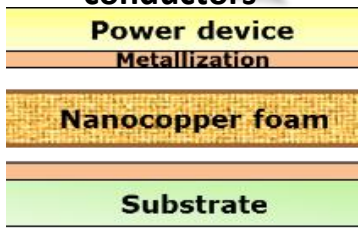
Thermal & Reliability

Metallization thickness scaling up to X10 for thermal management

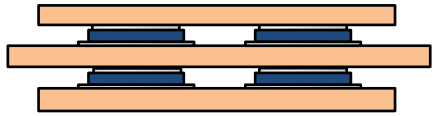




Stress buffering w/ advanced die-attach / conductors

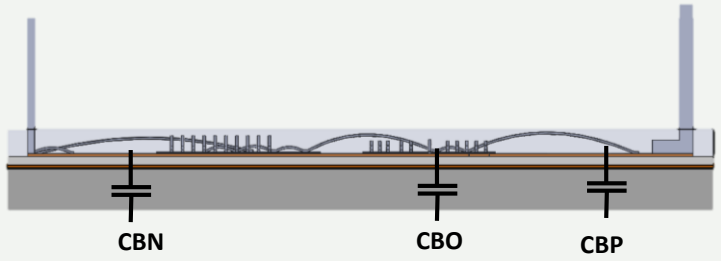


Symmetric 3D structure



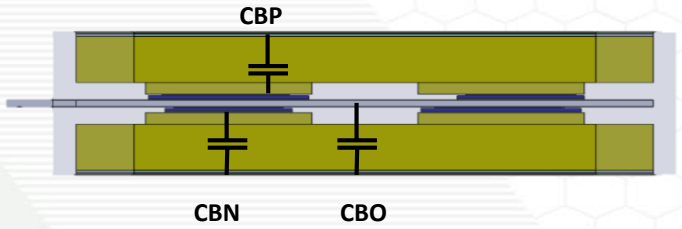
Package Parasitic Capacitance

Conventional Design

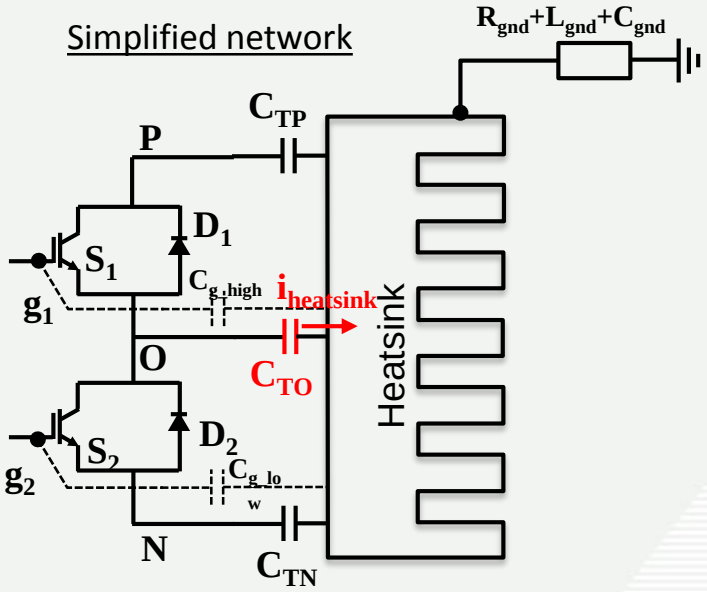


Vs.

Novel 3D Design



Simplified network

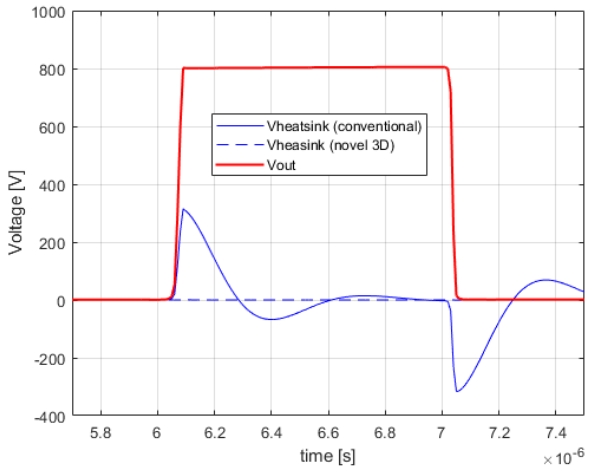


ANSYS MAXWELL simulations

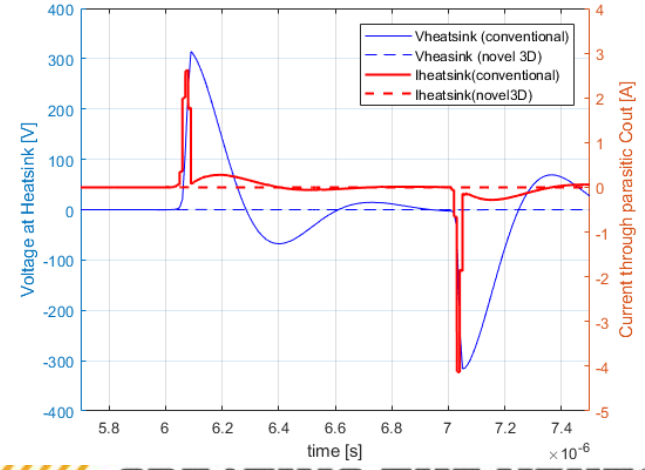
	Conventional	Novel 3D
BP-TN	123 pF	85 pF
BP-TO	**140 pF**	**0.08 pF**
BP-TP	15 pF	85 pF
BP-g_low	12 pF	0.015 pF
BP-g_high	9 pF	0.015 pF

LTSPICE simulations

Voltage at heatsink node



Common mode current (noise)

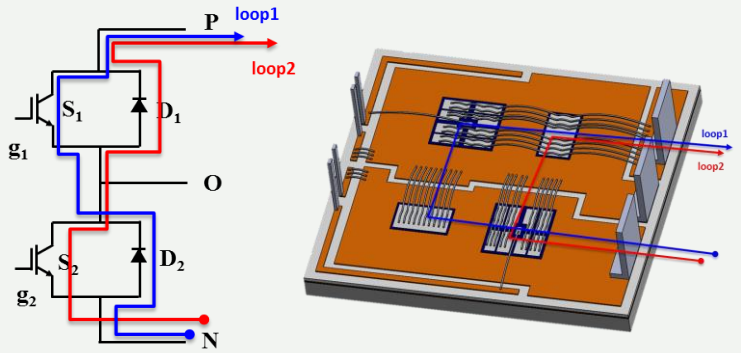


- Minimized output capacitance with new design (die stacking)
- Impact of dv/dt coupling with parasitic capacitance of package significantly reduced

Simulations by H. Lee

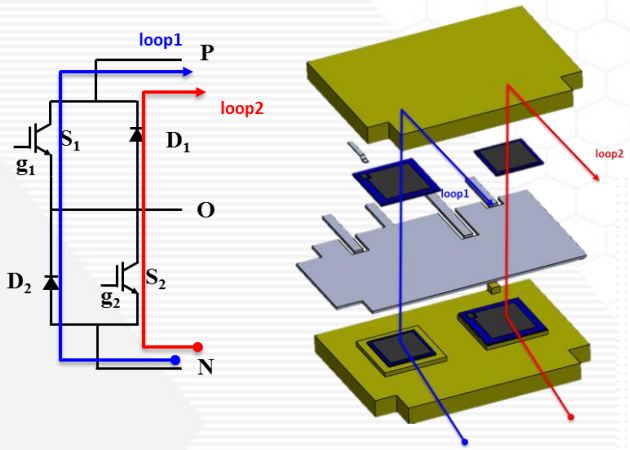
Package Parasitic Inductance

Conventional Design

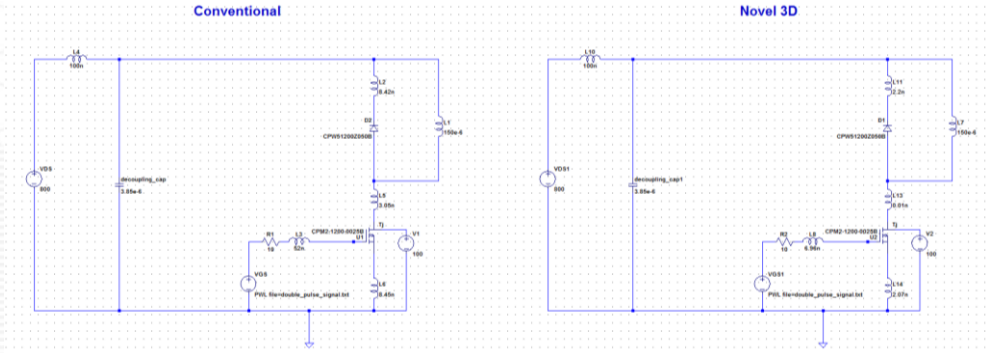


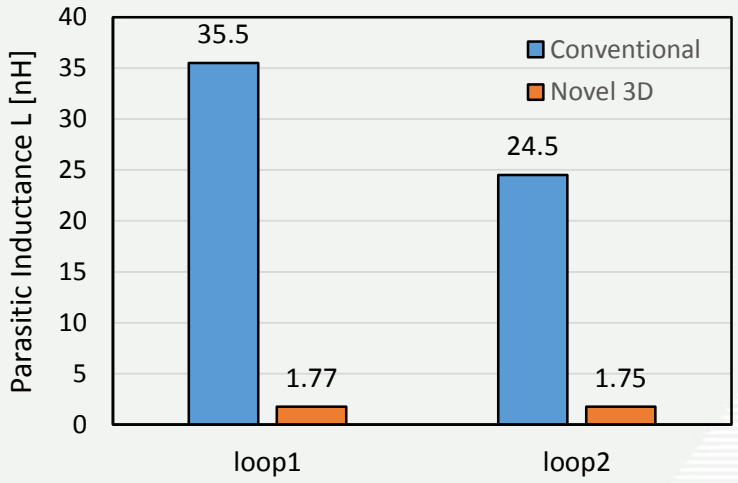
Vs.

Novel 3D Design



Double pulse tester setup for switching performance comparison

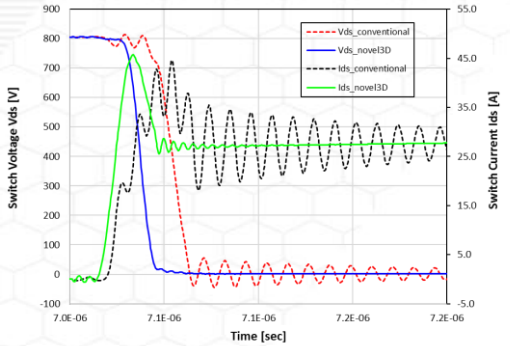




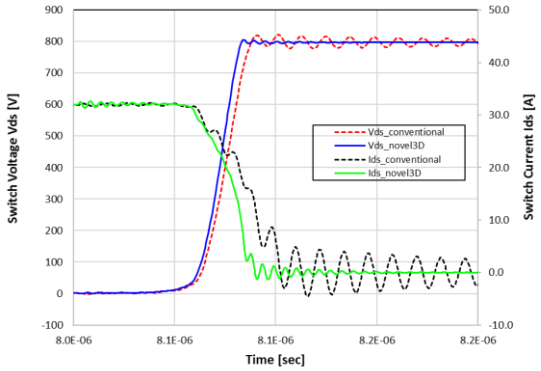
Switching energy loss

	Eon [mJ]	Eoff [mJ]
Conventional	0.80	0.27
Novel3D	0.48	0.19

Turn-on



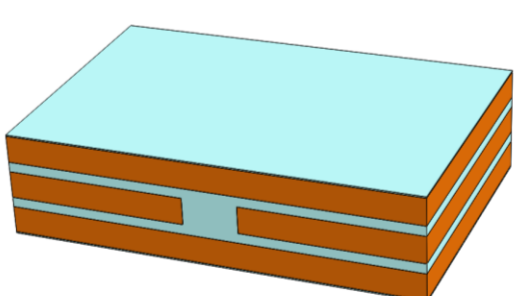
Turn-off

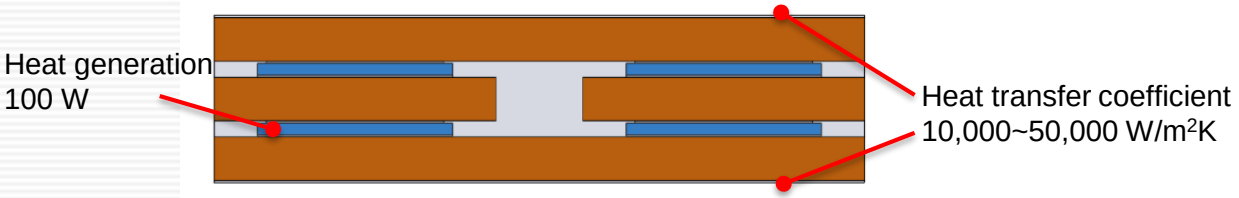


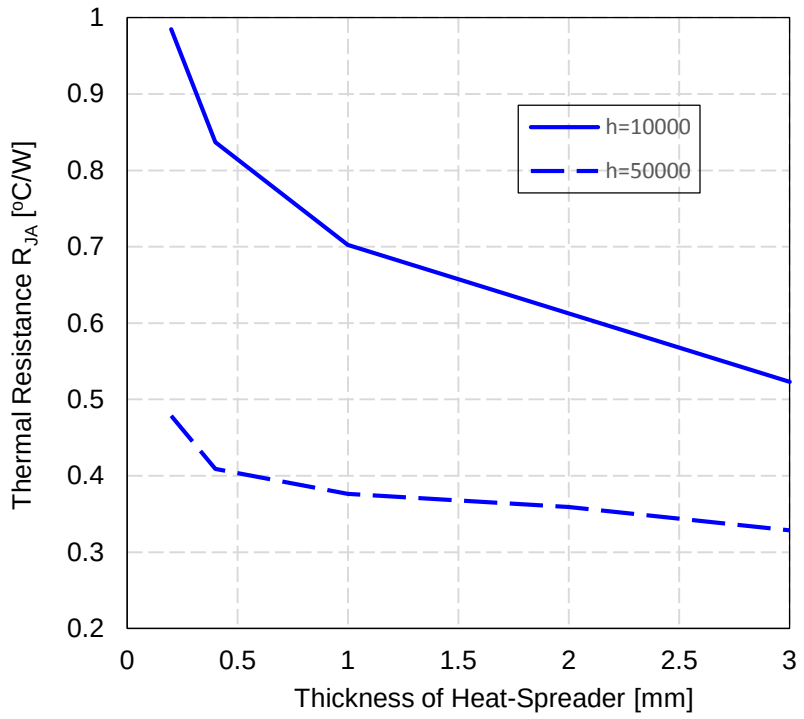
- Significant reduction in parasitic inductance – matching other 3D solutions
- Faster response achieved with less resonance in the waveforms
- Significant reduction in switching losses

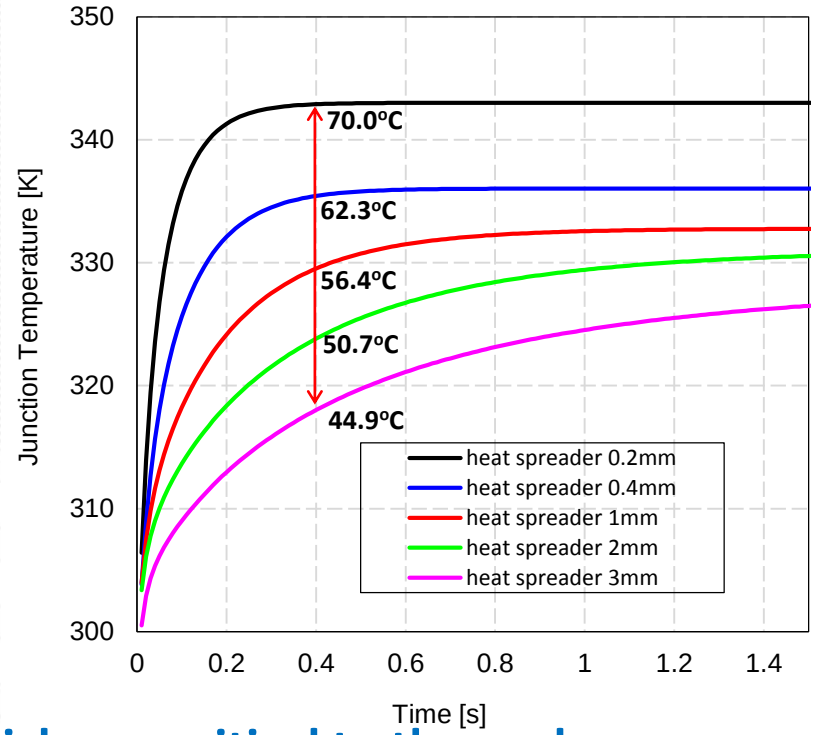
Simulations by H. Lee

Package Thermal Design – Effect of Cu Thickness





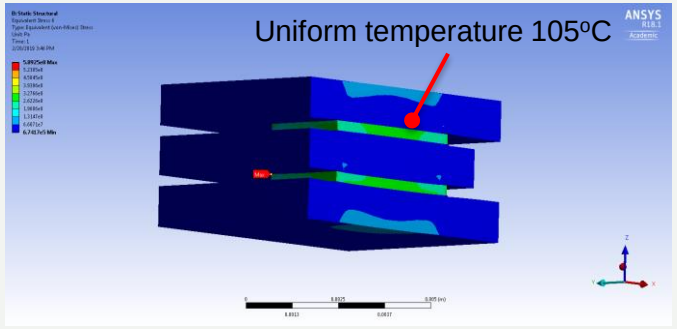


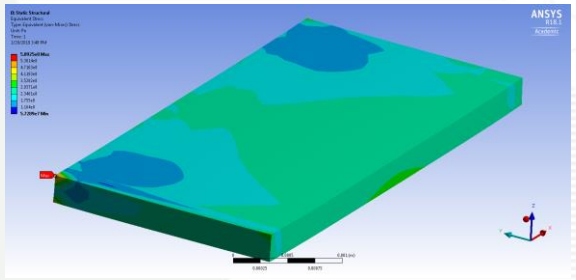


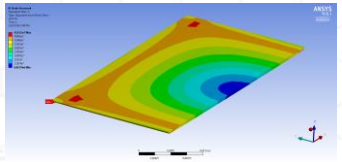
Contrary to 2D integration, increasing heat spreader thickness critical to thermal management in 3D

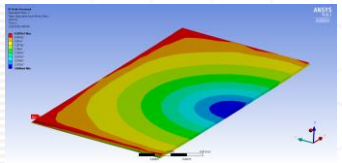
Modeling by H. Lee

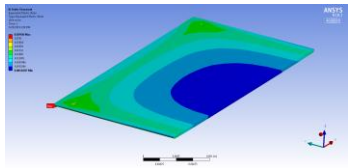
Thermomechanical Modeling – Effect of Cu Thickness

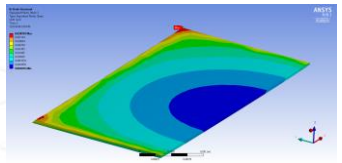




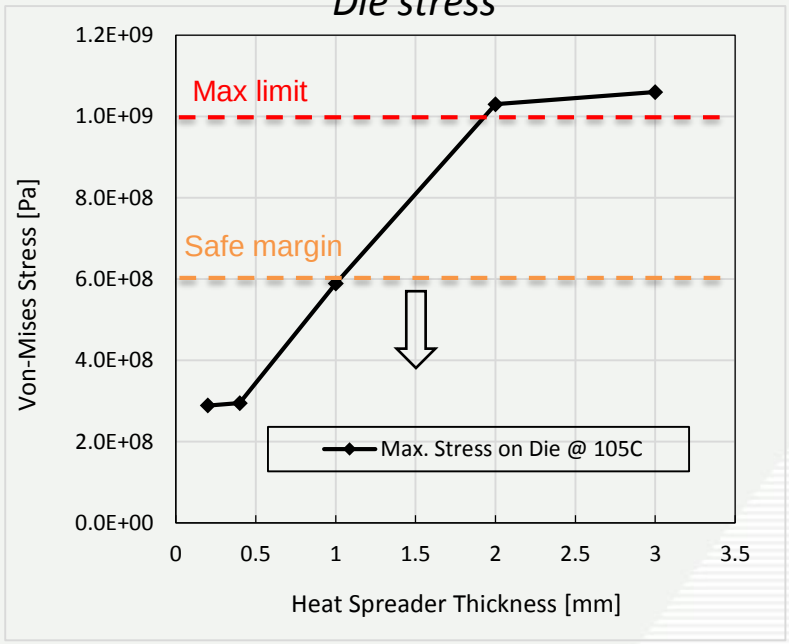




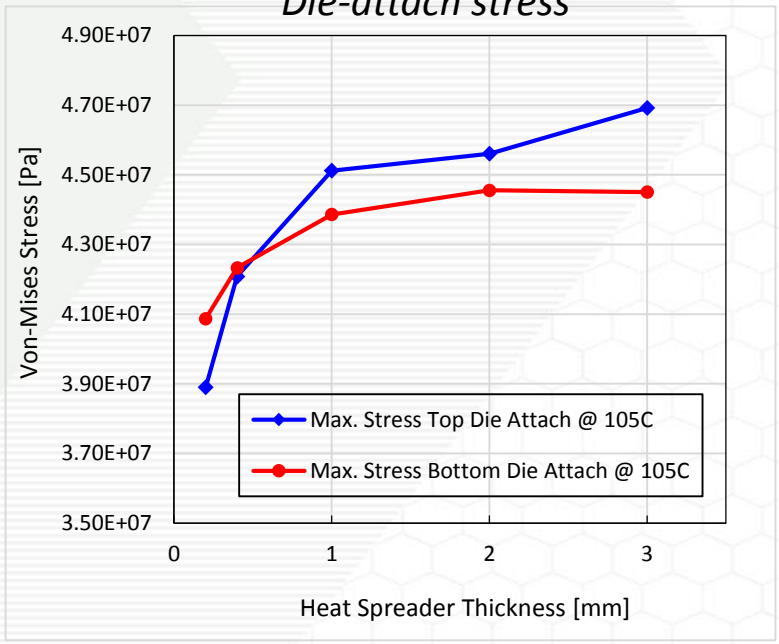




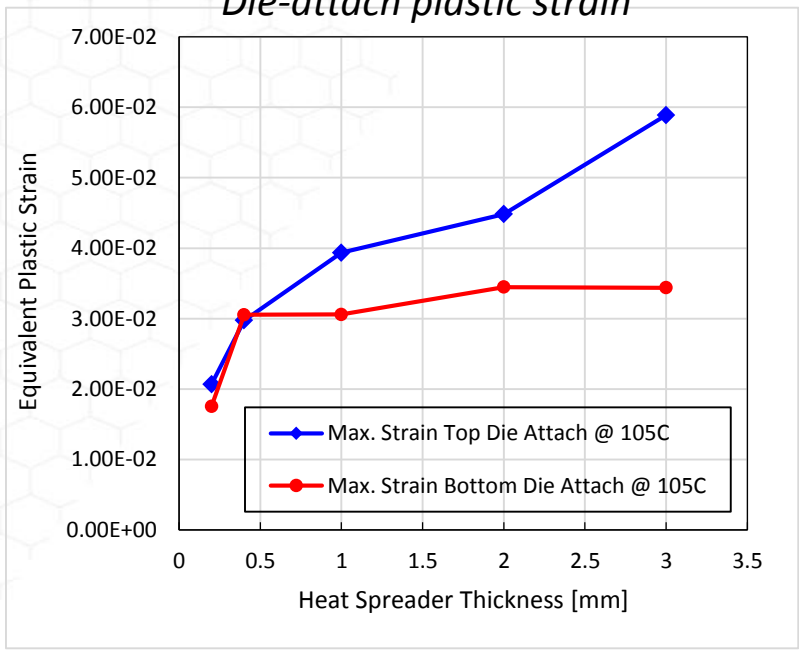
Die stress



Die-attach stress



Die-attach plastic strain



Trade-offs between thermal & reliability performances → material innovations to improve reliability

CREATING THE NEXT®

Modeling by H. Lee

Key Basic Technologies For Next-Gen SiC PKG

Multiphysics Design

- Transition from sequential electrical → thermal → mechanical to true multiphysics design
- Understanding of tradeoffs

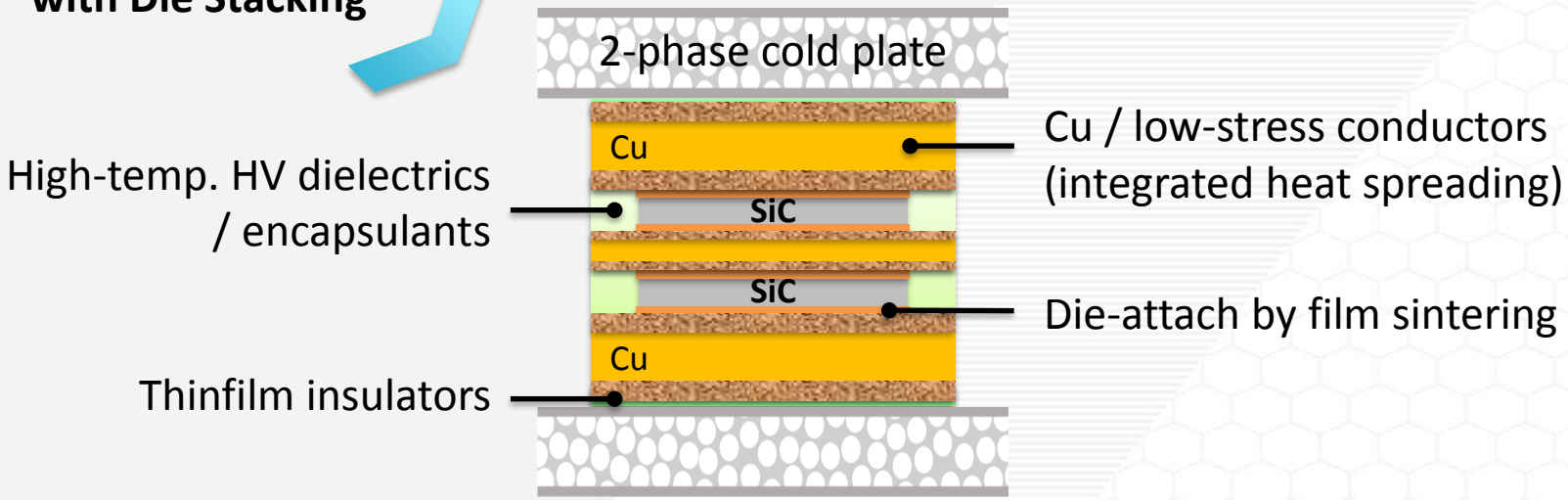
Materials Innovations

- Die-attach film sintering (Cu, organics-free, compliant)
- Low-stress, high-conductivity conductors (Cu-graphene)
- High-temp. HV dielectrics / encapsulants / thinfilm insulators

Manufacturing

- Standard panel-scale processing
- Co-develop with supply chain

3D Power Card with Die Stacking



System-level Cooling

- Single phase: ↑temperature uniformity
- Two phase: ↑dryout performance

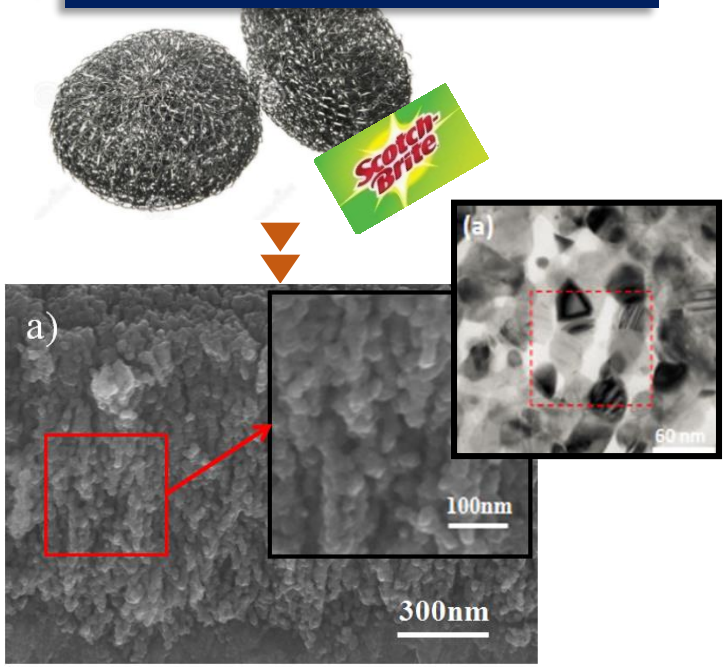
Reliability

- Power & thermal cycling
- ↑ max. junction temp.

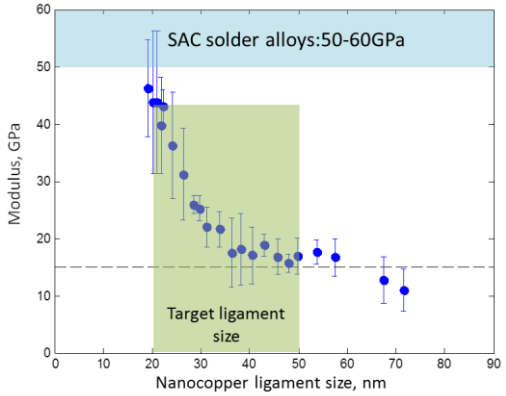
PRC's Die-Attach Solution: Nanoporous-Cu Film Sintering

Collaboration with Prof. Antoniou

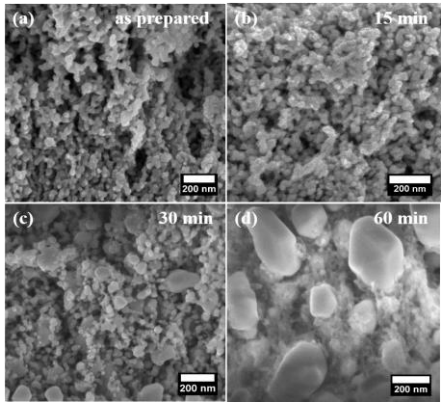
Nanoporous (NP) Cu: nanoscale metal sponges



High compliance pre-sintering

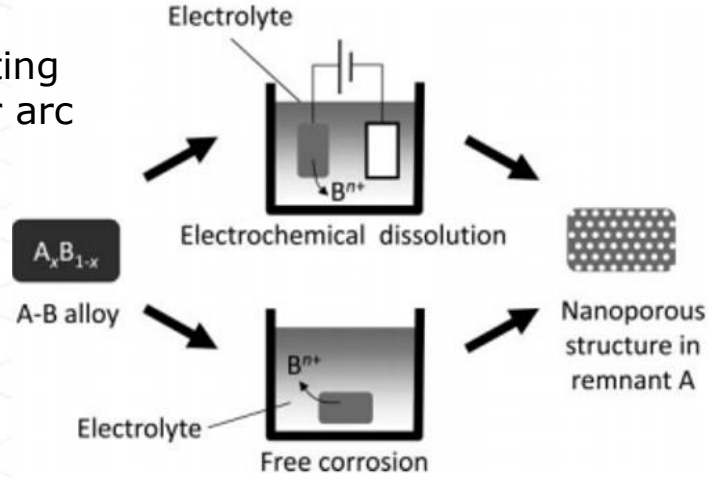


Controlled densification

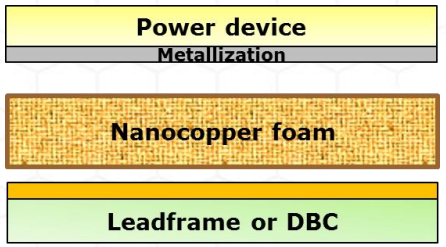


Low-cost synthesis by selective etching

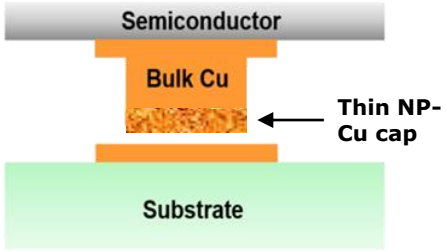
- Electroplating
- Furnace or arc melting



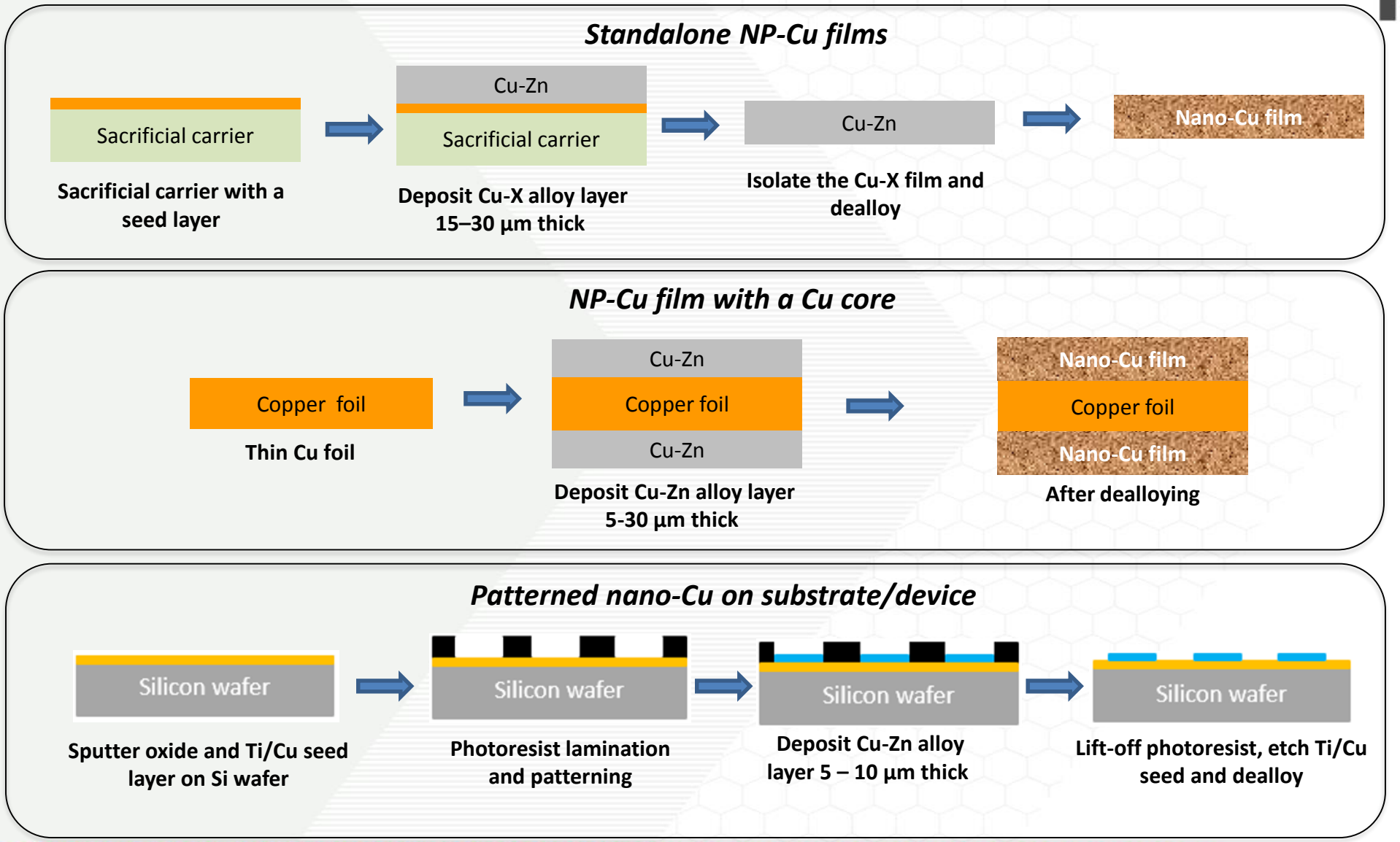
Die-attach films, inserts or preforms



Cu pillar with NP-Cu caps (semi-additive processing)

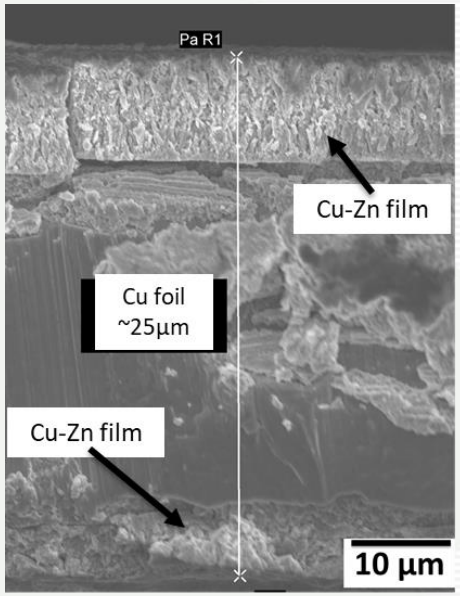


Versatility in Implementation

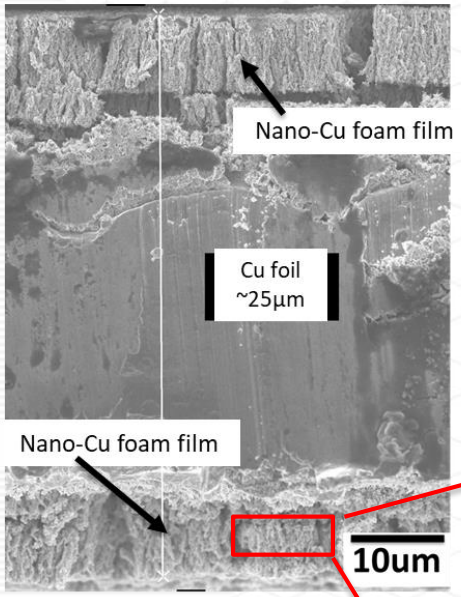


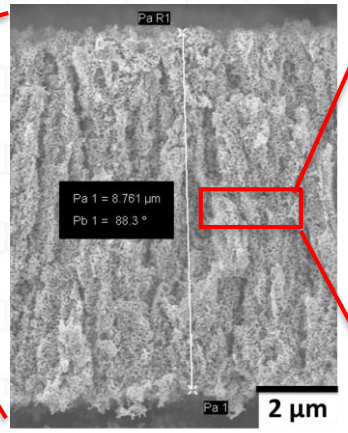
Collaboration with Prof. Antoniou

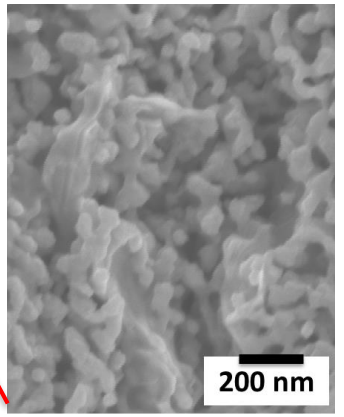
NP-Cu Die-Attach Films on Thinfilm Cu Core



Dealloying





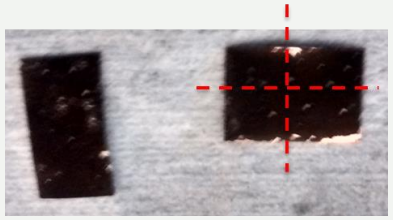


- **Total thickness easily adjustable**
- **8-10µm nano-Cu films on both sides**

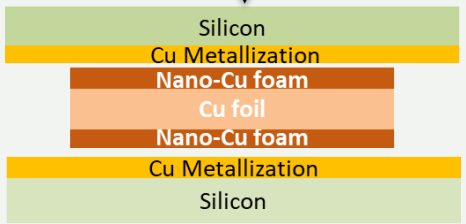
Collaboration with Prof. Antoniou

Data collected by K. Mohan

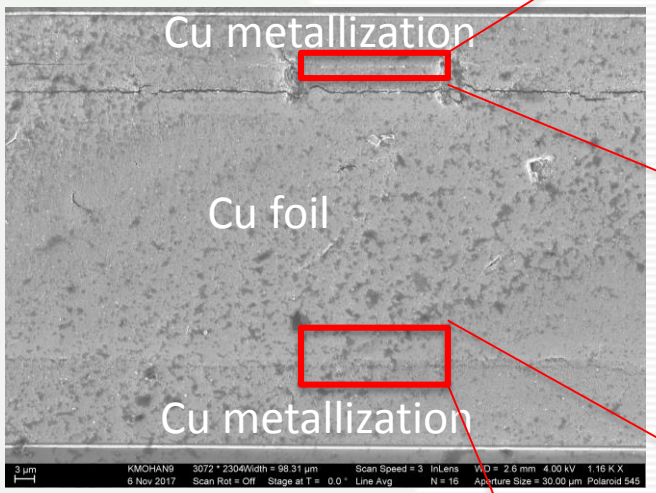
Sintering Demo of NP-Cu Film on Bulk Cu

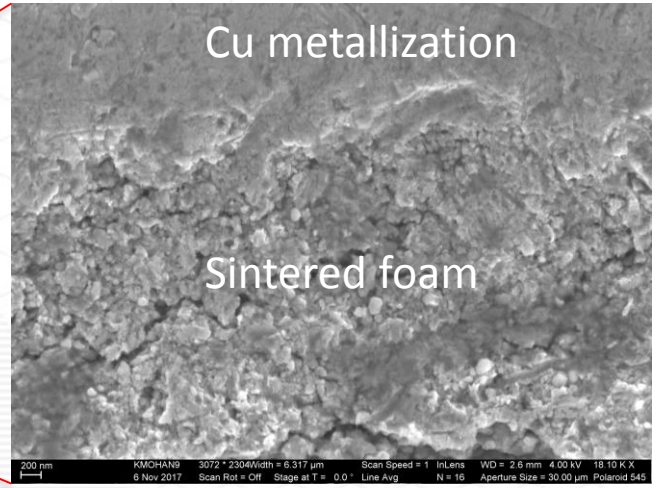


~1.5cm x 1.5cm
Diced into sections ~25mm^2

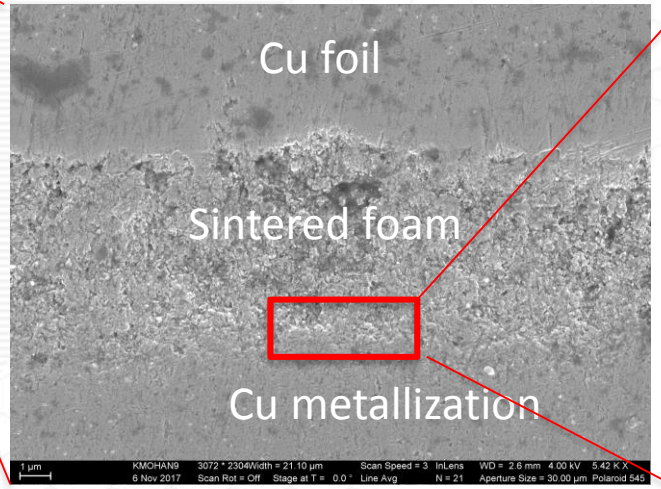


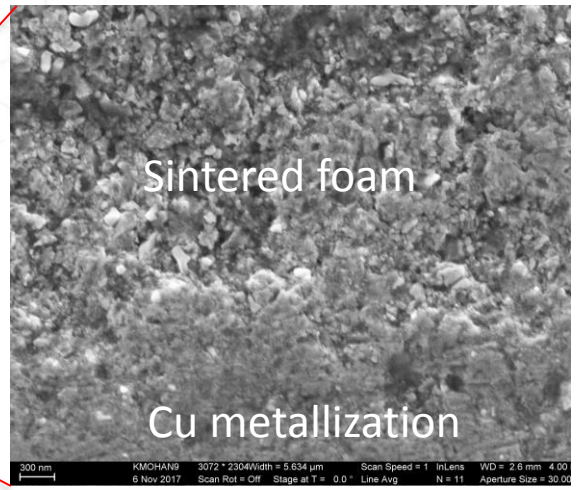
10MPa, 250C, 30min, forming gas





>99% density achieved

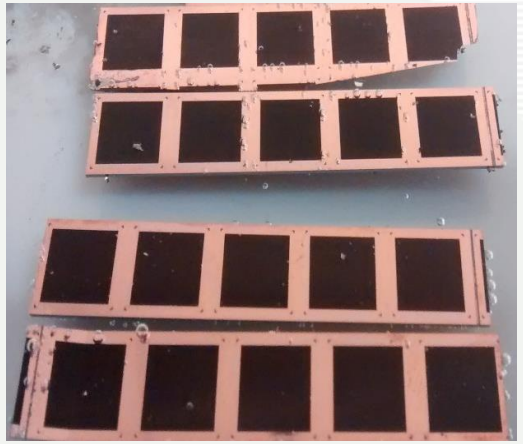




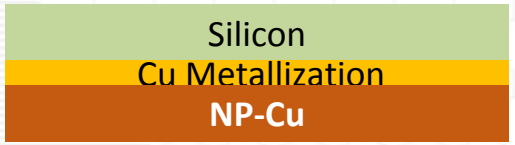
Collaboration with Prof. Antoniou

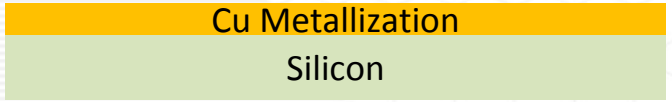
Data collected by K. Mohan

Direct Patterning by Semi-Additive Processing



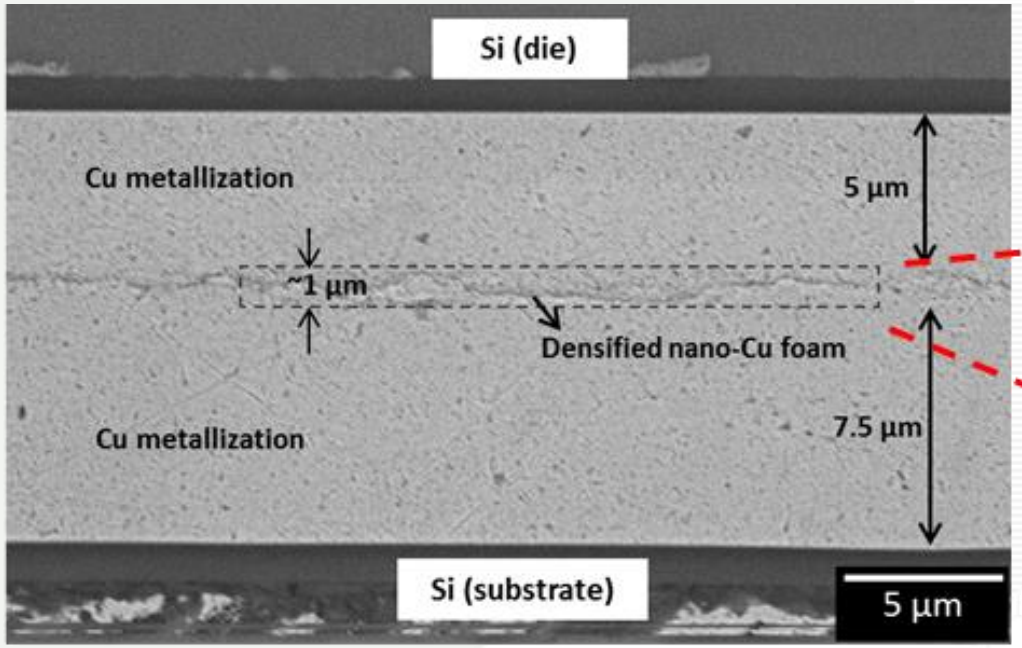
9MPa, 250C, 30min, forming gas

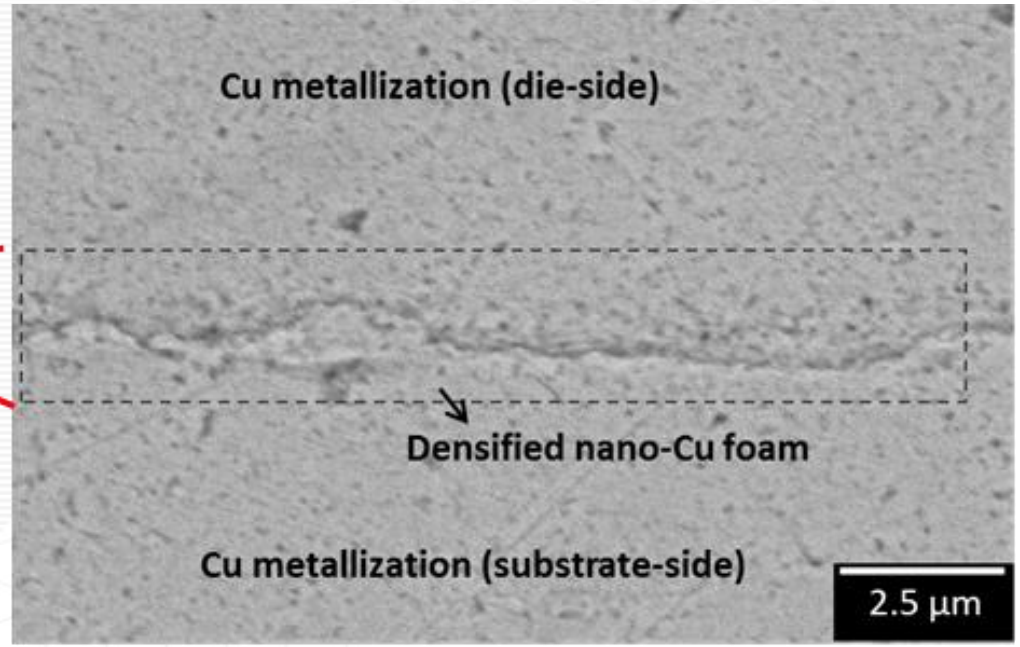




Die: 6.5mmx6.5mm
Substrate: 10mmx10mm

Apply & pattern on substrate, wafer, busbar, etc

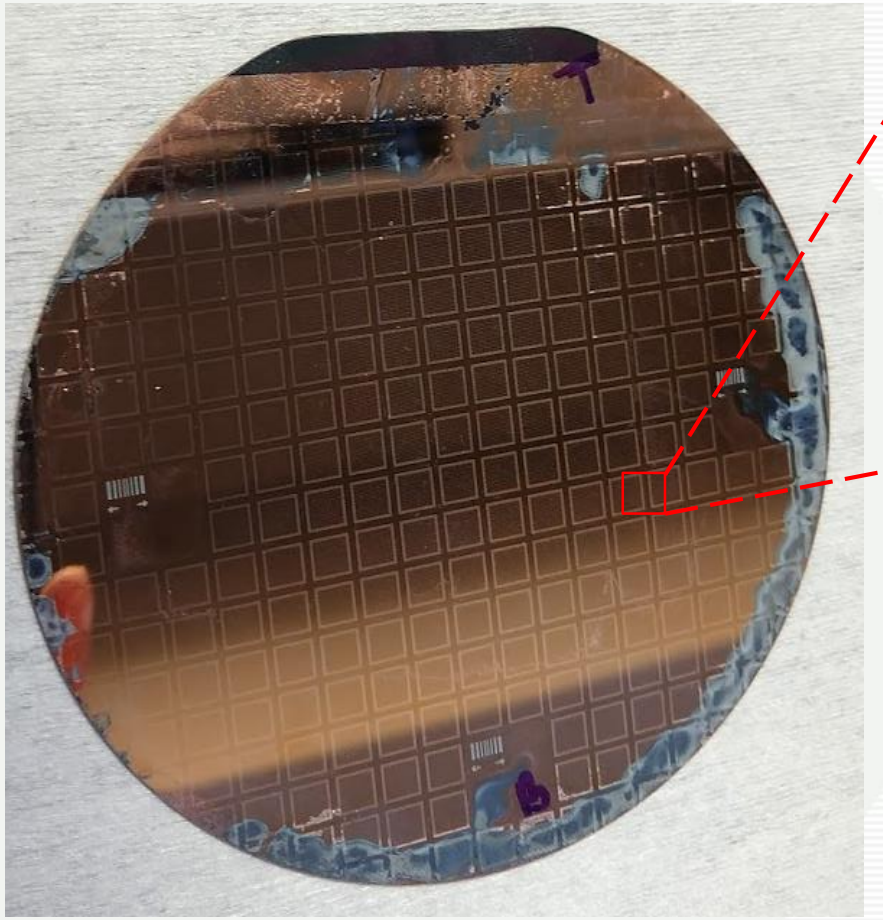




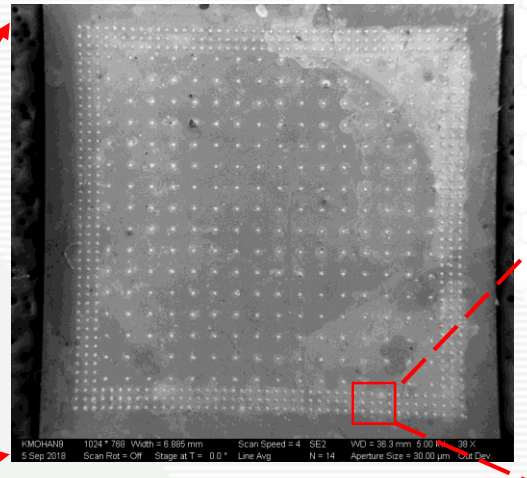
Collaboration with Prof. Antoniou

Data collected by K. Mohan

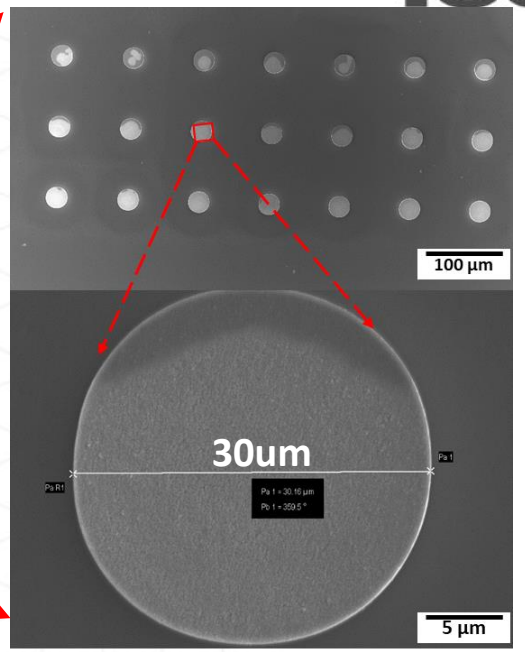
4” Wafer Bumping – Semi-additive Process

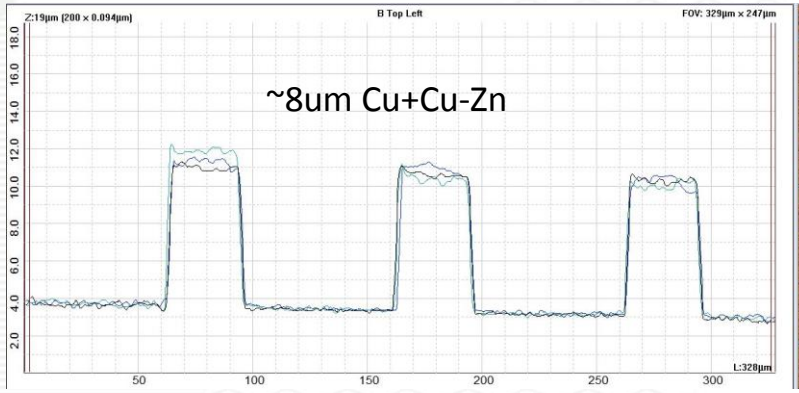


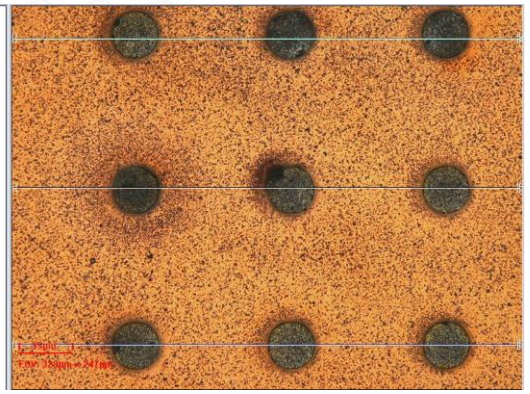
Precursor alloy: Cu-Zn



5mmx5mm die size





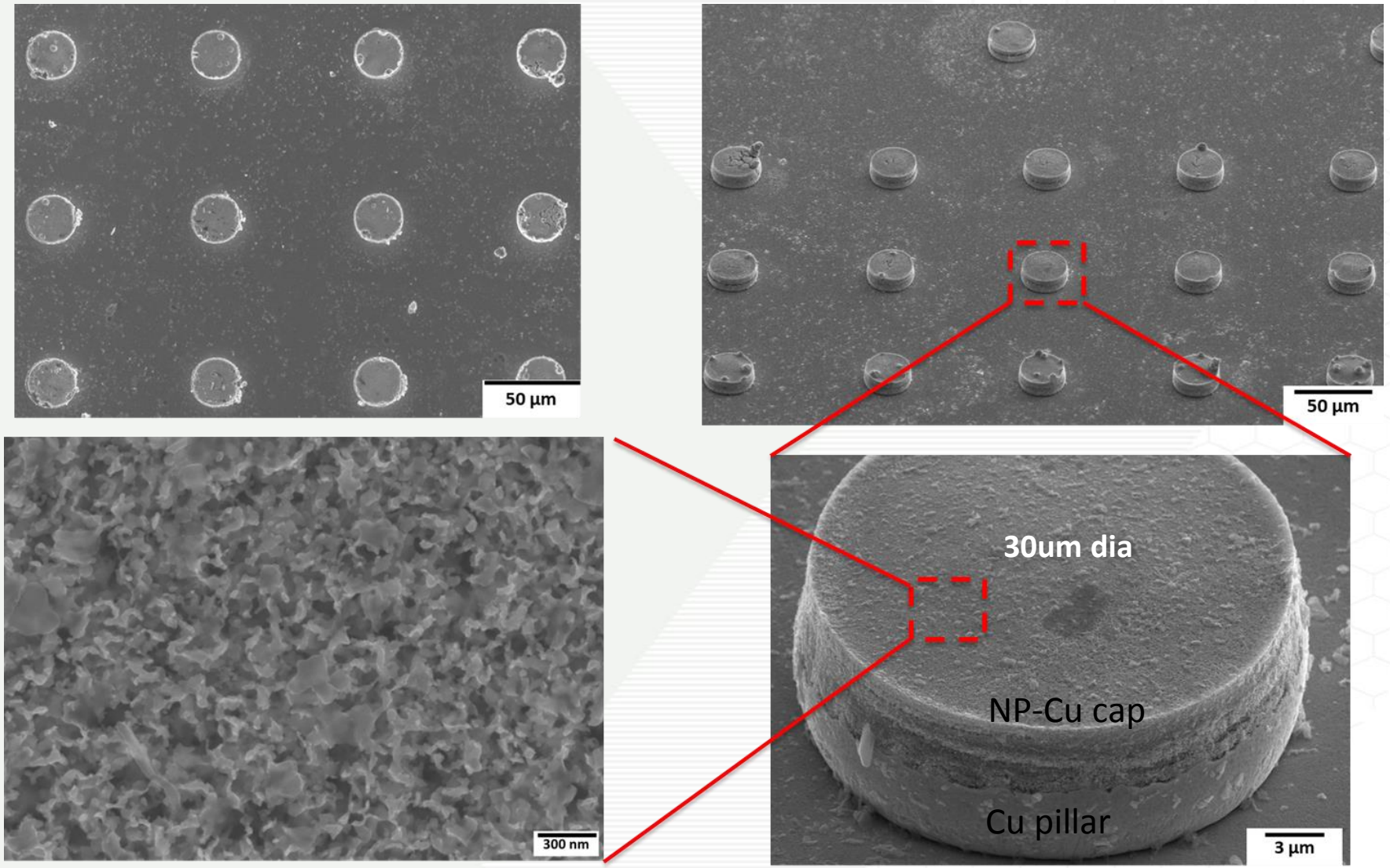


Successful plating of Cu-Zn in all the patterns, smooth surface profile, uniform Cu-Zn composition across wafer

Collaboration with Prof. Antoniou

Data collected by K. Mohan

4” Wafer Bumping – NP-Cu Cap Formation



- **Initial Cu:Zn ~ 35:65**
- **Dealloying time in dil. HCl: 90-120min**
- **Feature sizes: 40-250nm**

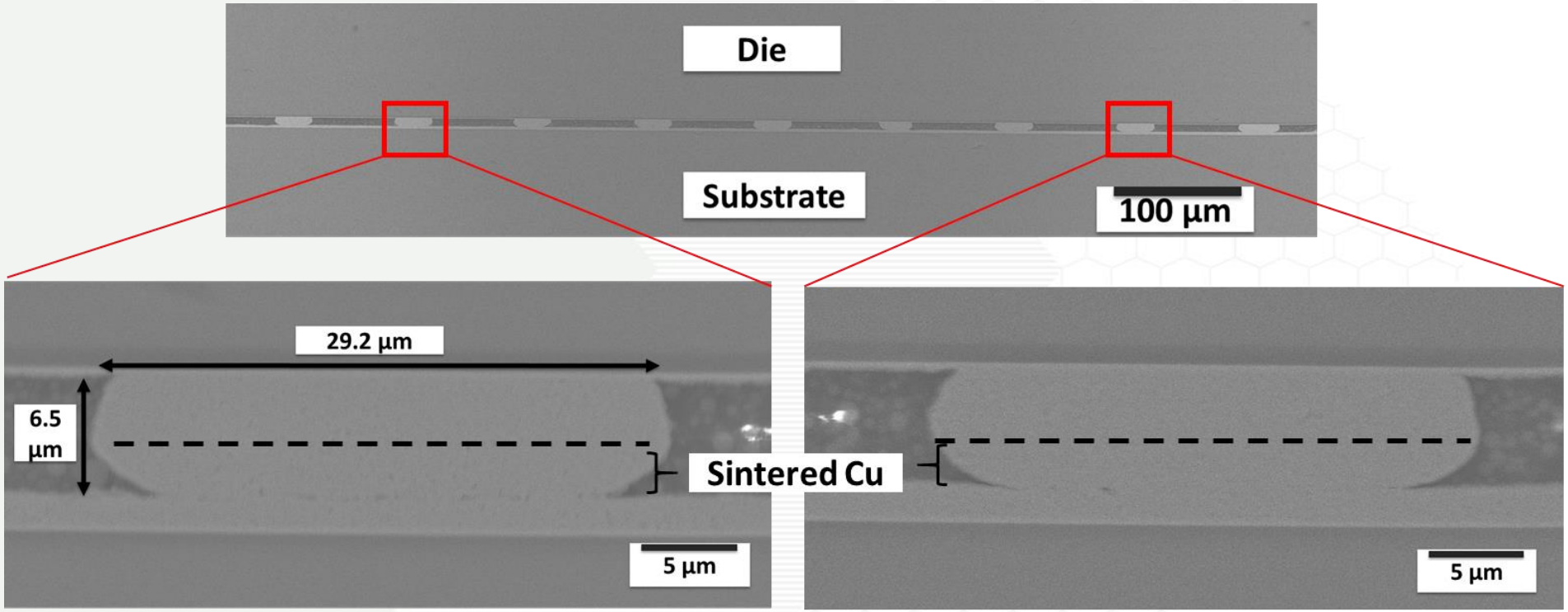
Uniform and smooth surface morphology of NP-Cu caps after dealloying

Collaboration with Prof. Antoniou

Data collected by K. Mohan

Cu Pillar with NP-Cu caps – Assembly Demo

Assembly parameters: 30MPa, 300C, 30min, forming gas

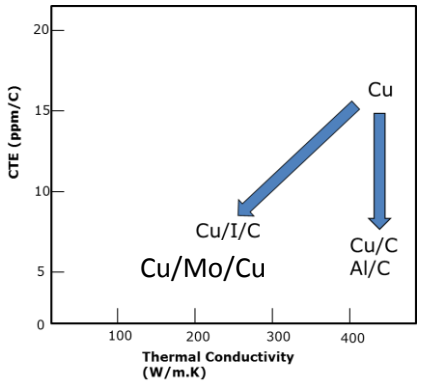


Collaboration with Prof. Antoniou

Data collected by K. Mohan

Low-stress Conductors: Cu-Graphene Composites

Laminates vs. Composites



Cu composites preferred to retain thermal conductivity of Cu while offering a CTE range

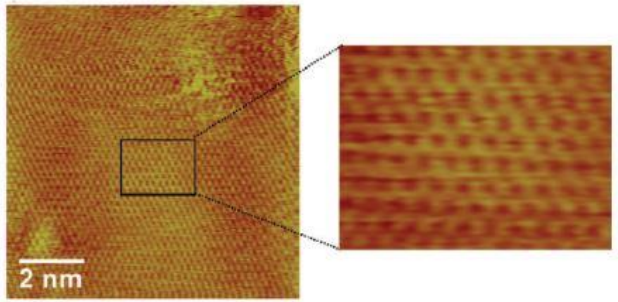
PRC's Solution

Cu-graphene bulk composites

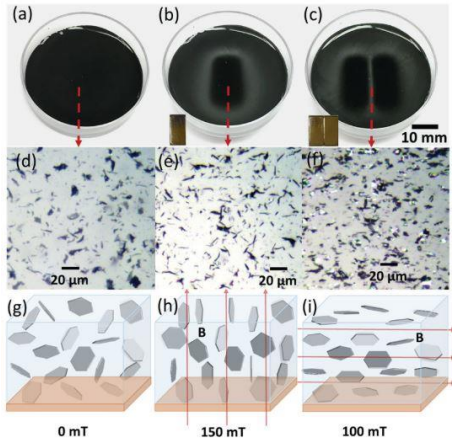
- Tailorable CTE 3-15ppm/K with λ ~ 460W/m·K
- "Second sound" effect in graphene
- Direct plating & vacuum powder processing
- *Applications*: Cu functionalization, metallization on DBC/AMB substrates, integrated heat spreaders

Low-cost Synthesis

- Electrochemical exfoliation of graphene from graphite



- Orientation control by magnetic field



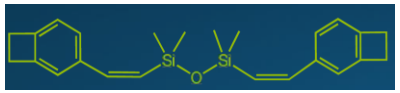
Lin et al (2017)

- Implementation in plating line
- Plasma sintering

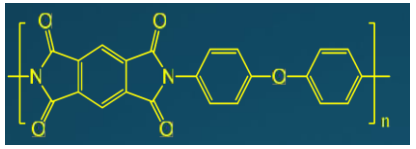
High-Temperature Dielectrics & EMCs

High-temp. dielectrics with improved interfacial reliability & processability

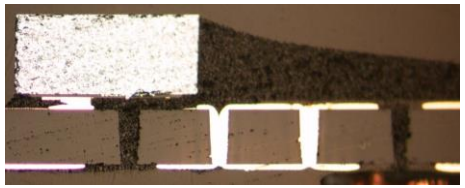
BCB



Polyimide

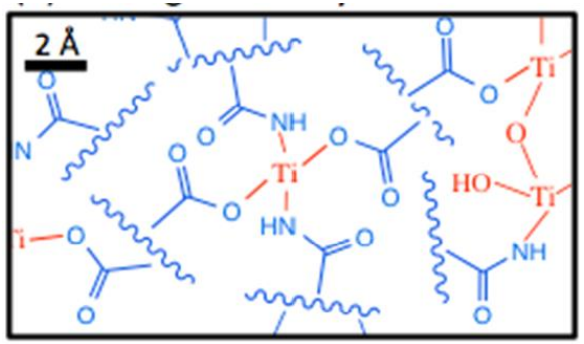


High-temp. glass PKG with BCB



High-temp. & high-conductivity hybrid dielectrics

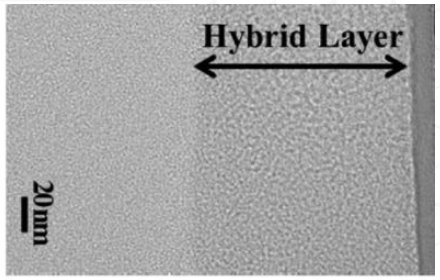
Titania-organic hybrid

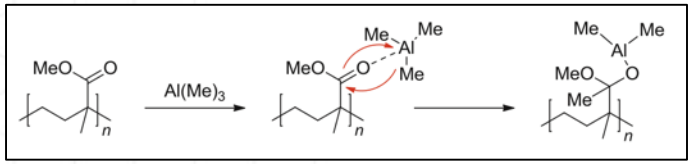


With Prof. Losego

Low-cost and polymer-compatible hermetic coating

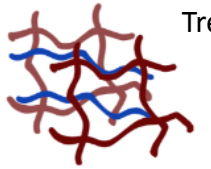
With Prof. Losego



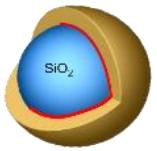


High-temperature HV Mold Compound *(Prof. C.P. Wong)*

New concept for high-temp. stability



Treated/ coated silica

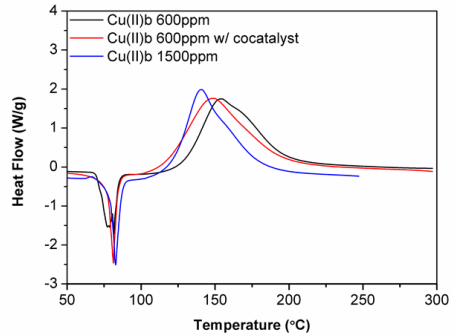


CE/EP chemistry

Unreacted -OCN | Moisture ingression | **Metal catalyst**

Formulation design for:

- *High-temperature stability*
- *High breakdown voltage*

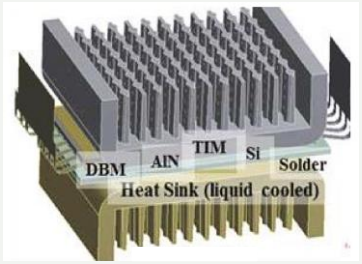


System-level Cooling: Advanced Cold Plates

Collaboration with Prof. Joshi

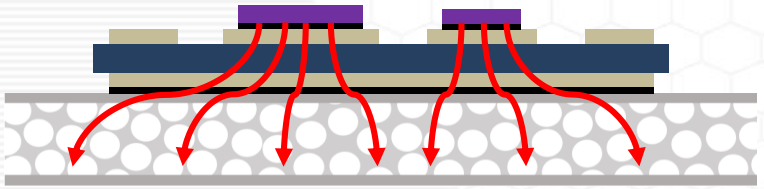
Prior Art

- Aluminum channels brazed onto substrate, single phase, WEG (Prius)

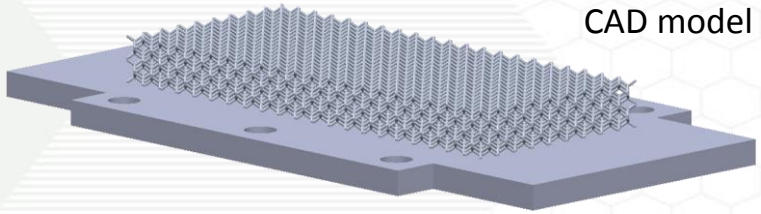


- Snaking injection-molded copper channels, single phase, WEG (Volt)

New Concept



CAD model



- Decrease temperature non-uniformity and hotspot formation in single phase
- Increase critical heat flux by delaying dryout failure for reliable two-phase cooling

NEW CONCEPTS

- Additively manufactured (AM) foam-type structures
  - Rhombic dodecahedron unit cell for stochastic foam imitation
- Elimination of contact resistance
  - Direct printing to eliminate thermal interface materials
- Local control of parameters such as pores per inch (PPI), porosity (ε), elongation, etc.
  - Allows for localized hotspot cooling, thermal gradient management, vapor pathways

Summary

- Advances in several building block technologies from low to high power electronics for next-gen 3D power modules
  - High-density passives
  - Package designs for high dv/dt capability vs. soft switching topologies
  - Low-cost sintered Cu die-attach films
  - Low-CTE high-conductivity conductors
  - High-temperature dielectrics and interfaces
  - Low-cost panel-based fabrication with supply chain
- First prototype (SiC full-bridge rectifier) expected in 2019 end

Acknowledgements

- This work is funded by PRC's Industry Consortium & SRC's "Global Research Collaboration"

- Collaborators: GRAs K. Mohan, H. Lee, R. Sosa, J. Li, J. Broughton,
  GT Profs. Antoniou, Joshi, Losego, Wong, Center for Distributed Energy

- PRC & IEN staff & infrastructures

Georgia Tech

CREATING THE NEXT®

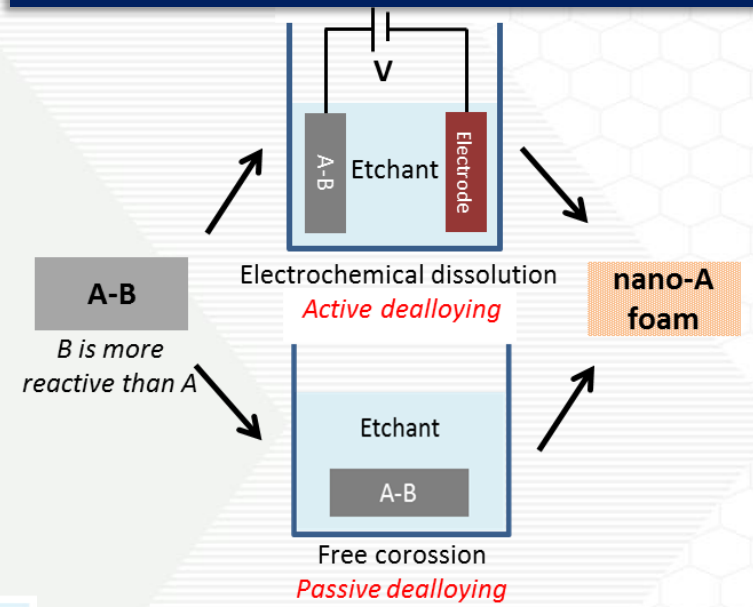
Back-Up Slides

Nanoporous (NP) Cu Synthesis – Concept

A-B alloy fabrication:

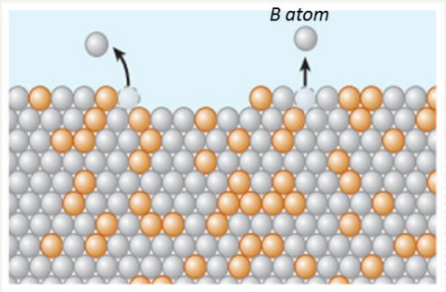
- Electro-deposition
- Co-sputtering
- Melt spinning
- Furnace melting

Alloying and chemical delalloying

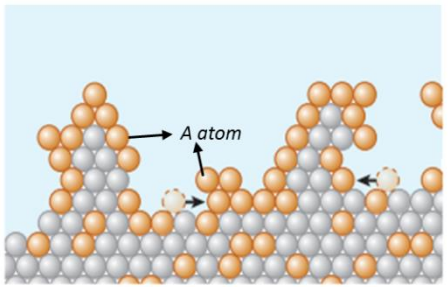


Dealloying parameters are:

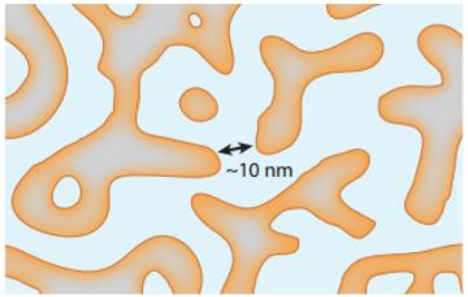
- Etchant chemistry
- Dealloying time
- Applied potential (V_c)
- Temperature



Dissolution of more reactive 'B' element in the etchant



Rearrangement of 'A' by surface diffusion

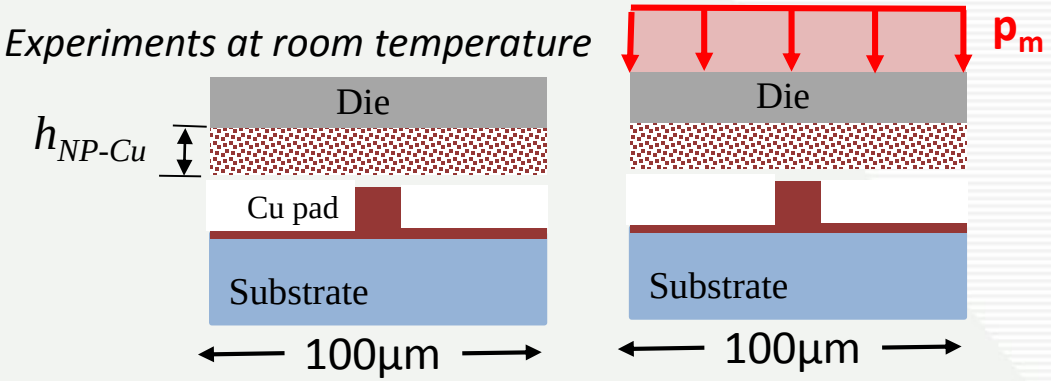


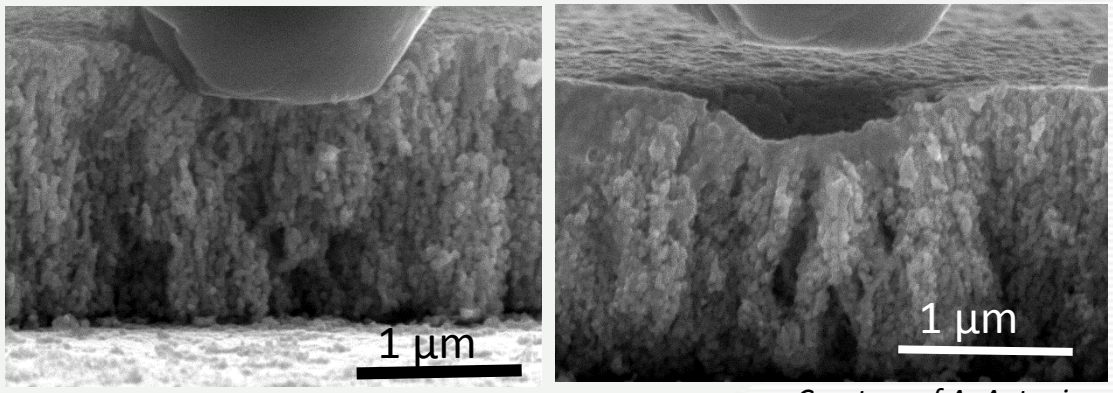
Final nanoporous structure after dealloying

Hakamada, M. and M. Mabuchi (2013)." Critical Reviews in Solid State and Materials Sciences **38**(4): 262-285.

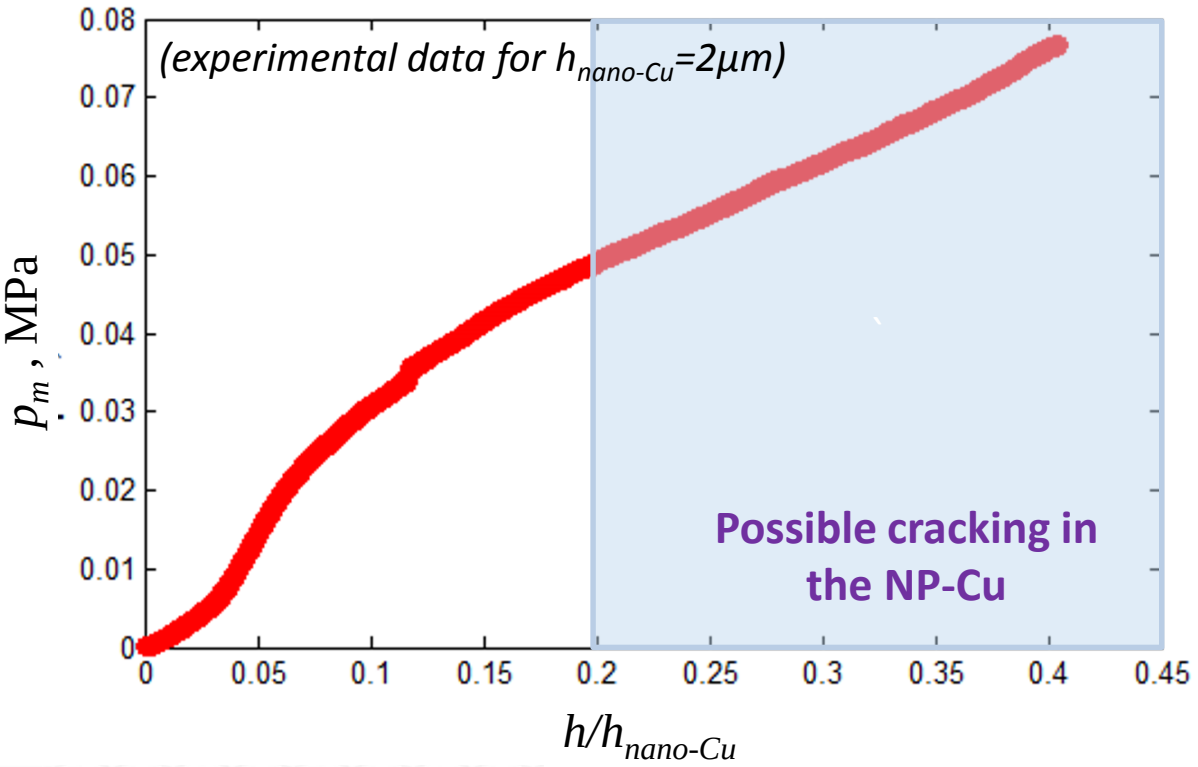
The Promise of Nanoporous (NP) Cu: Compliance

Experiments at room temperature





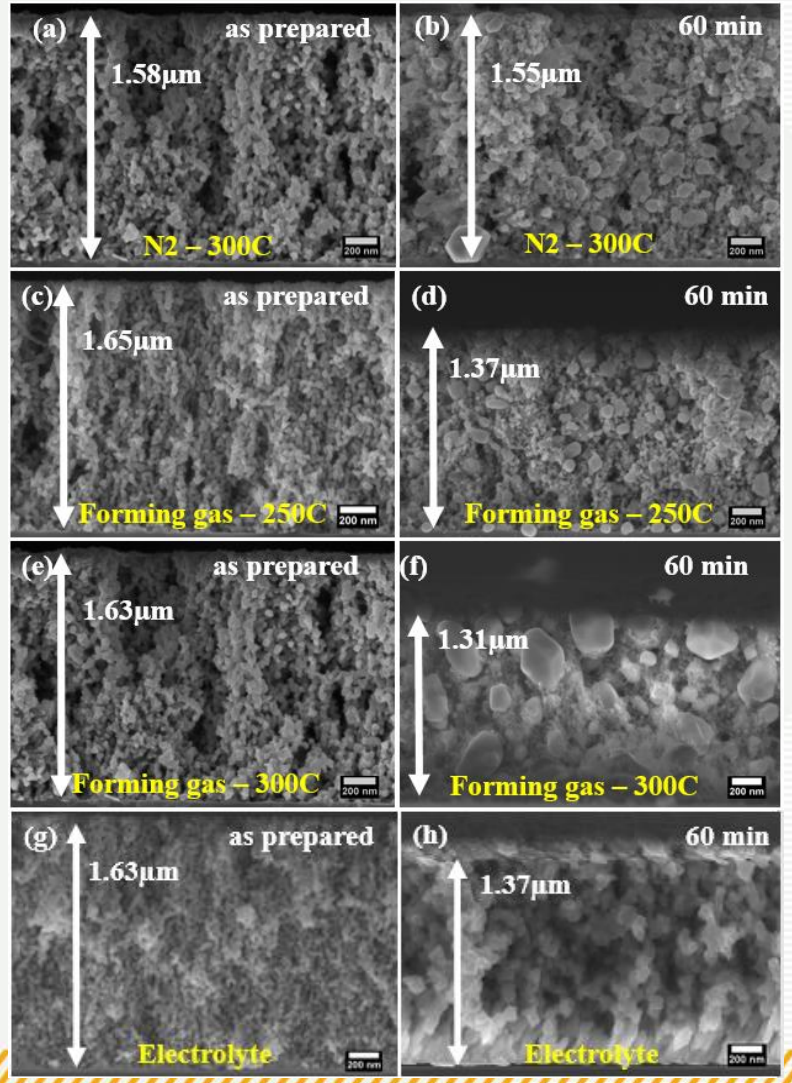
Courtesy of A. Antoniou

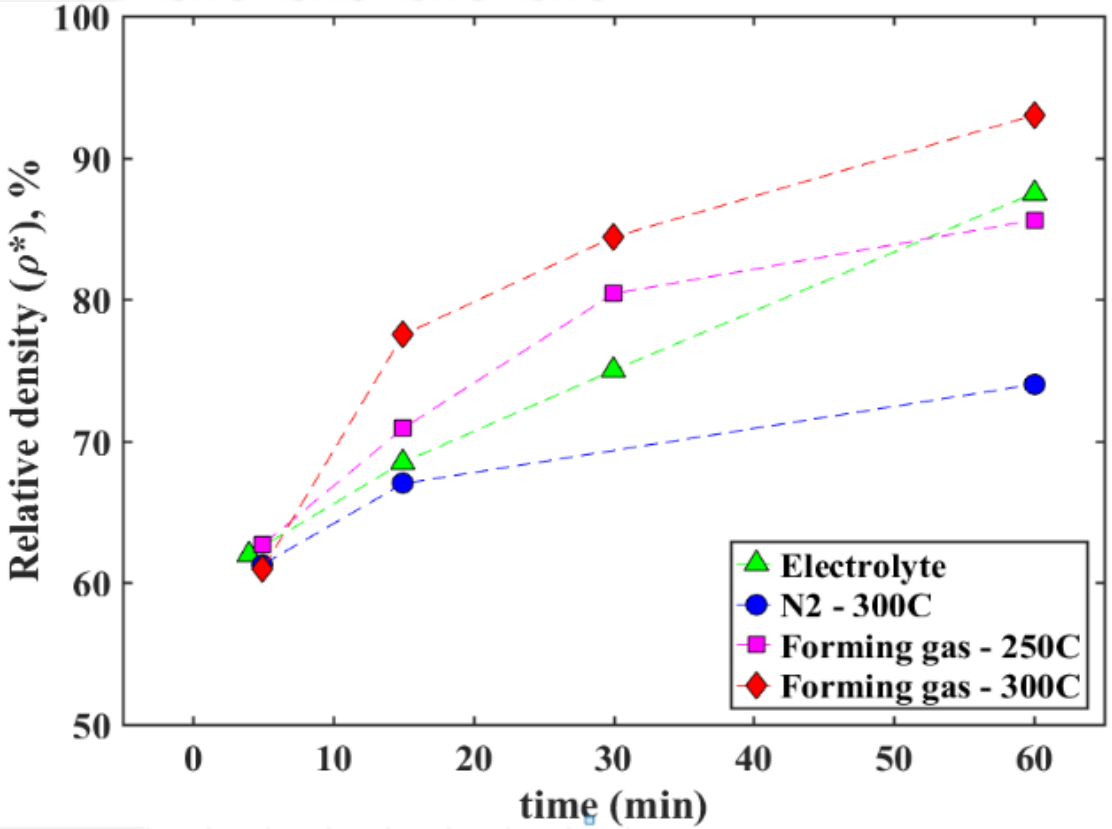


- NP-Cu deforms at very low load
- Limit to amount of displacement of the NP-Cu before micro-cracking starts: ~20% of initial height (conservative estimate)

The Promise of Nanoporous (NP) Cu: Sintering Kinetics

Thermal sintering carried out in inert N_2 and reducing environments (N_2 + 3% H_2)

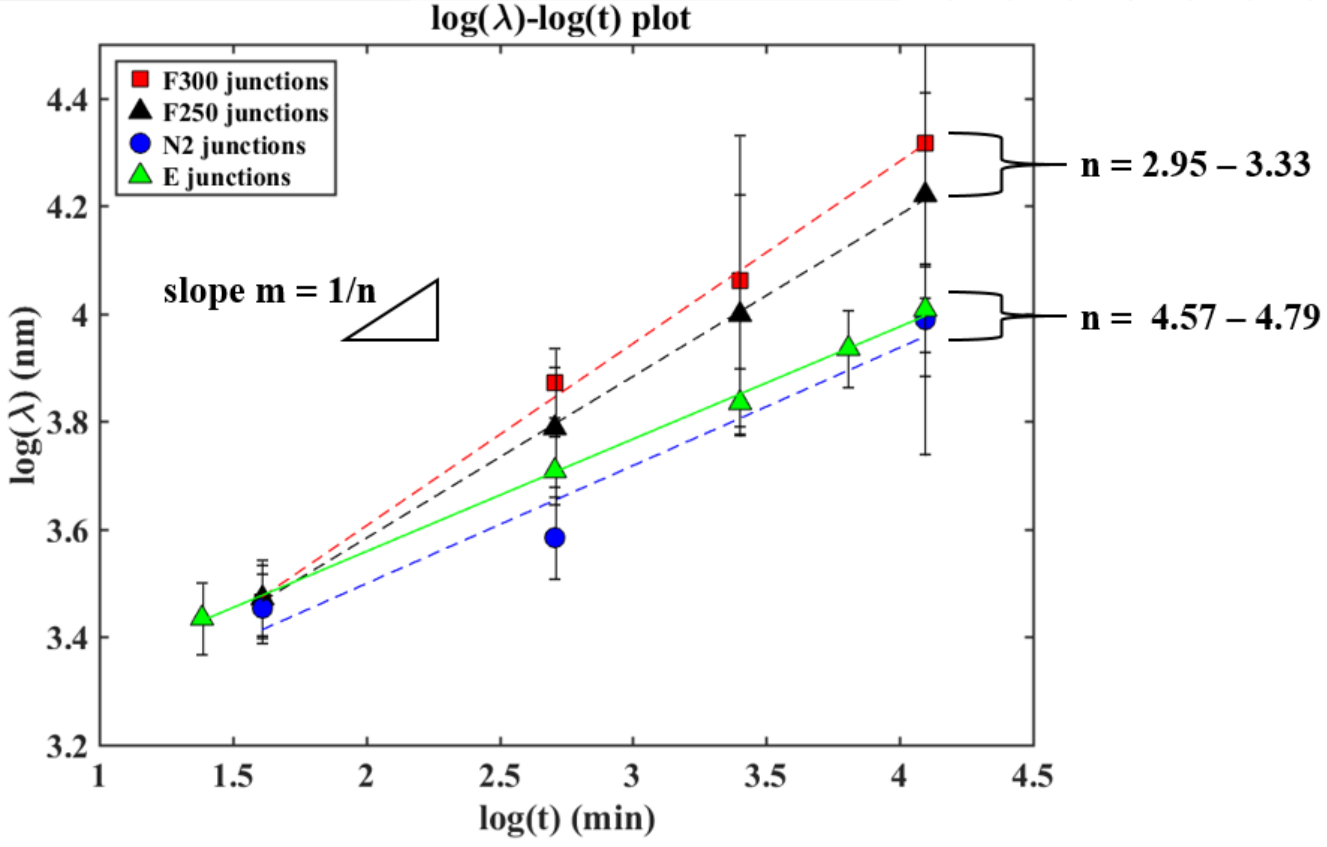




Studies ongoing to understand nature of sintering under different environments to be able to design NP metals for sintering applications

N. Shahane, V. Smet, A. Antoniou "Anomalous coarsening in nanoporous metals" (nearing submission)

The Promise of Nanoporous (NP) Cu: Sintering Kinetics



$$d^n = KtD_s$$

Grain-growth model

$$D_s = D_0 \exp\left(\frac{-E}{RT}\right)$$

Arrhenius function

$$d^n = KD_0 \exp\left(-\frac{E}{RT}\right)t.$$

Combined equation

- More complex mechanism than simple surface diffusion under heat
- Surface diffusion driven kinetics under electrolyte coarsening

The initial results indicate NP metals have very high surface energy resulting in complex sintering kinetics that need to be further studied and understood

N. Shahane, V. Smet, A. Antoniou "Anomalous coarsening in nanoporous metals" (nearing submission)

Wafer Bumping Process Flow – Solder vs. NP-Cu Caps

Chip/Substrate

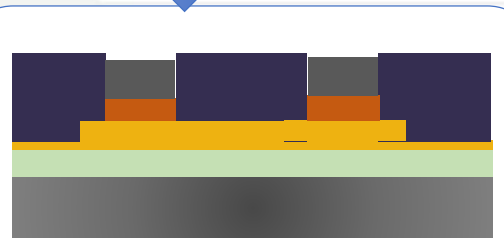
Substrate (Si, Organic, Glass)

Package RDL

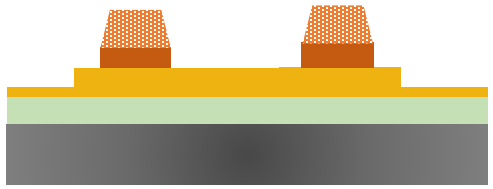
Seed layer deposition (Ti/Cu)

PR patterning

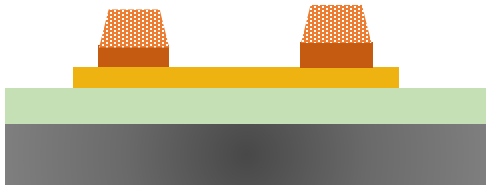
Nanocopper foam caps fabrication



Cu-Zn co-plating



PR strip and dealloying

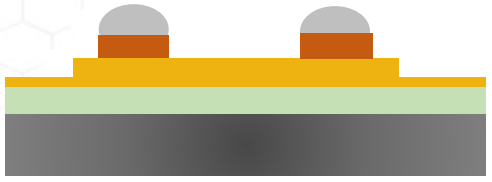


Etch seed layer and dicing

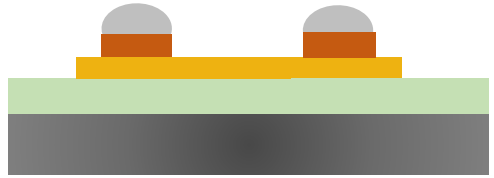
Assembly

Solder cap fabrication

Sn-Ag co-plating

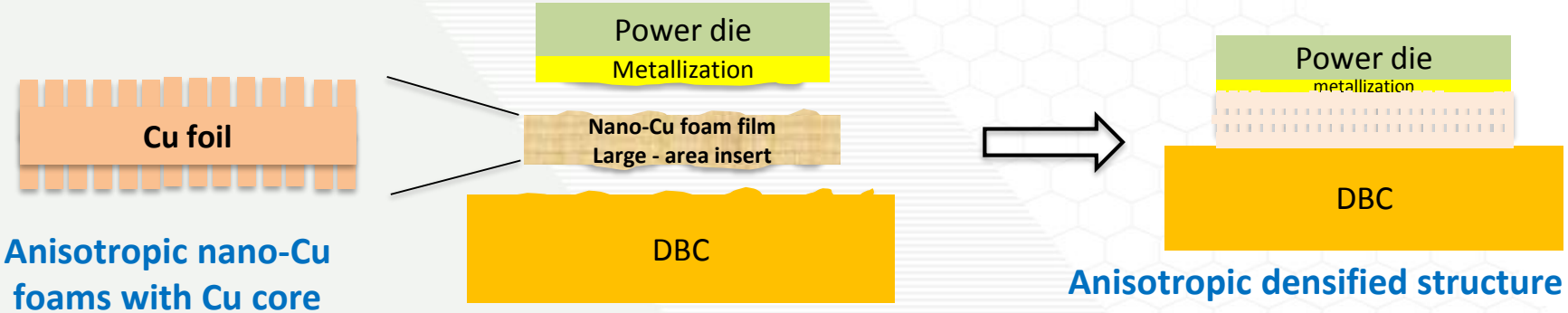


PR strip and solder reflow



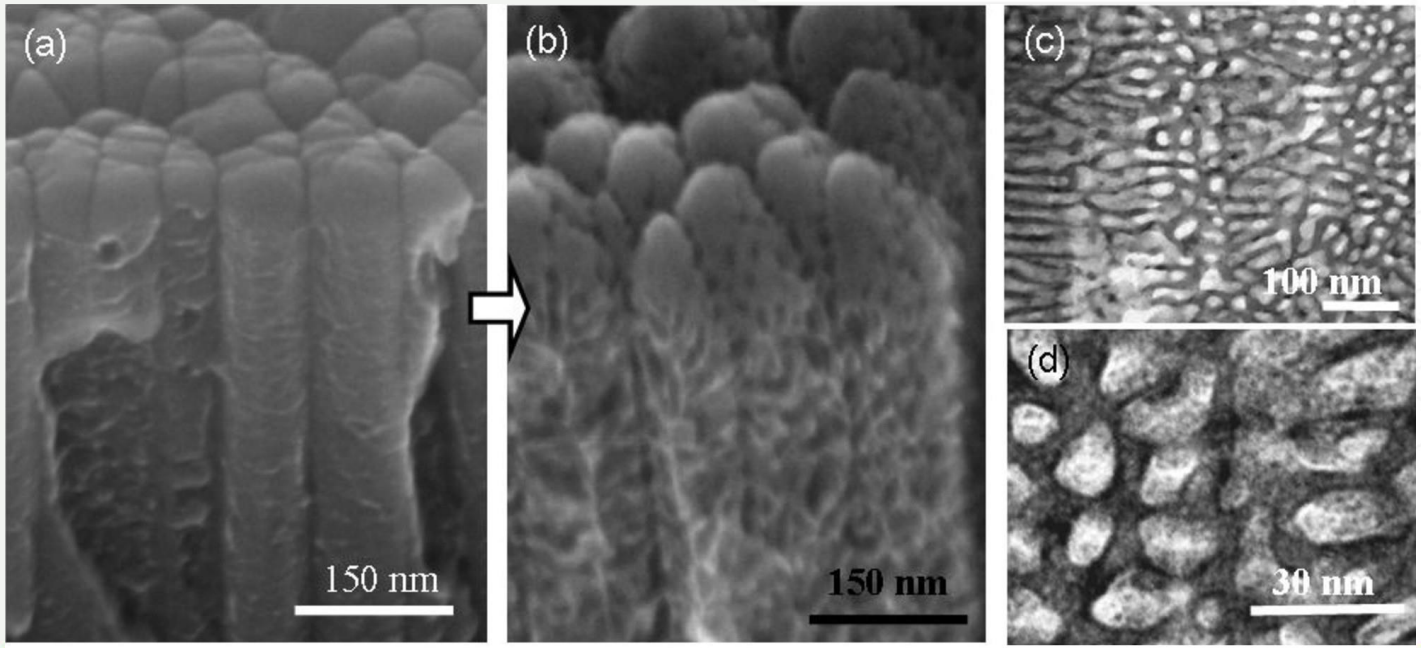
Etch seed layer and dicing

Concept of anisotropic foams for stress buffering in die-attach



Anisotropic nano-Cu foams with Cu core

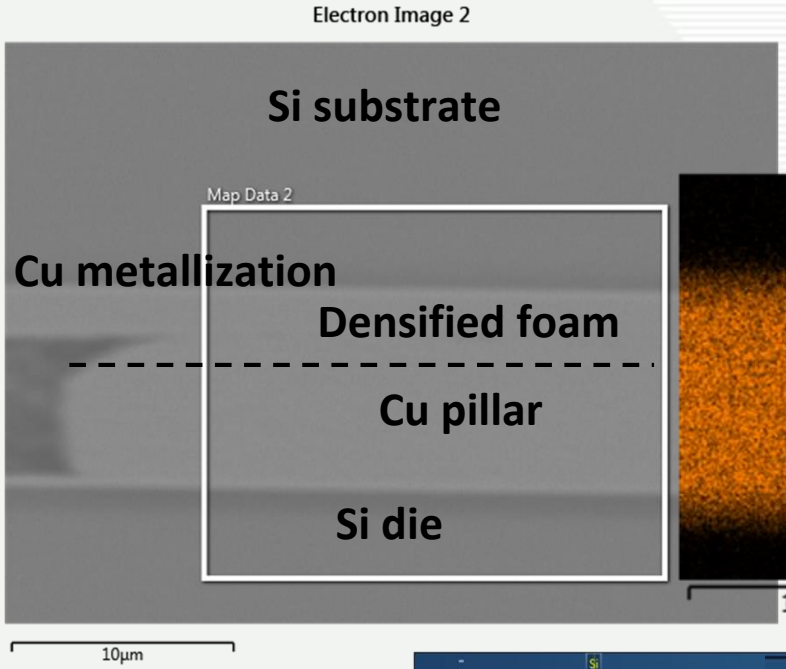
Anisotropic densified structure with good thermal and electrical performance in Z direction and compliance in X-Y plane

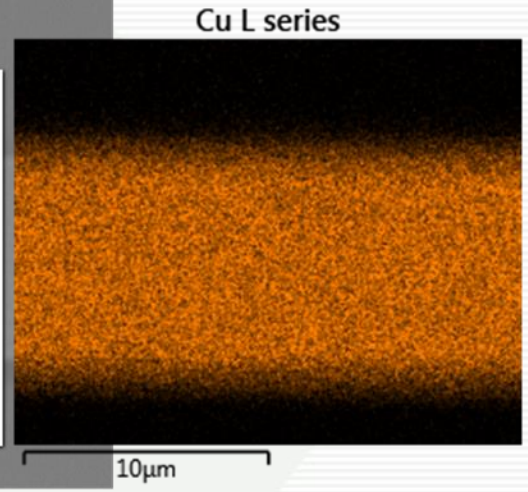


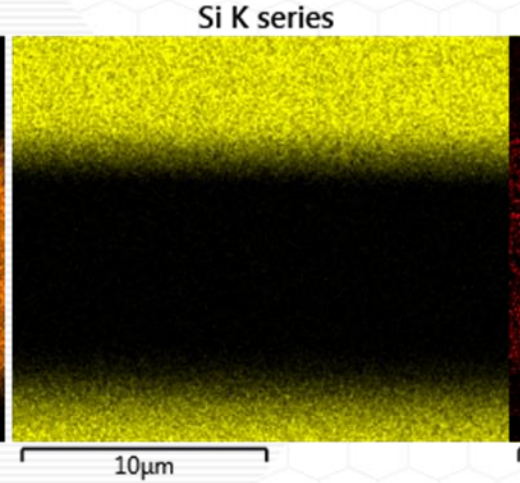
Anisotropic platinum foams with vertical channels

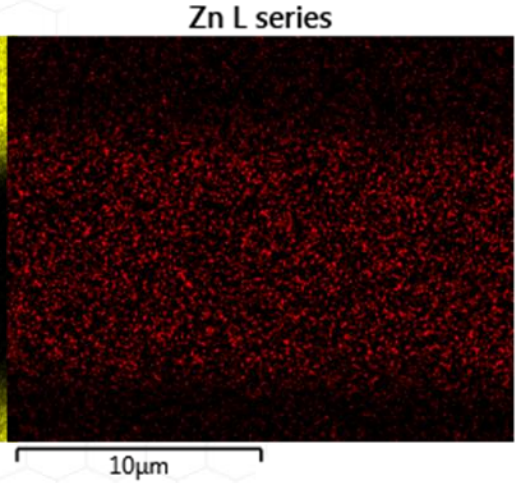
Antoniou, Antonia, et al., 2009

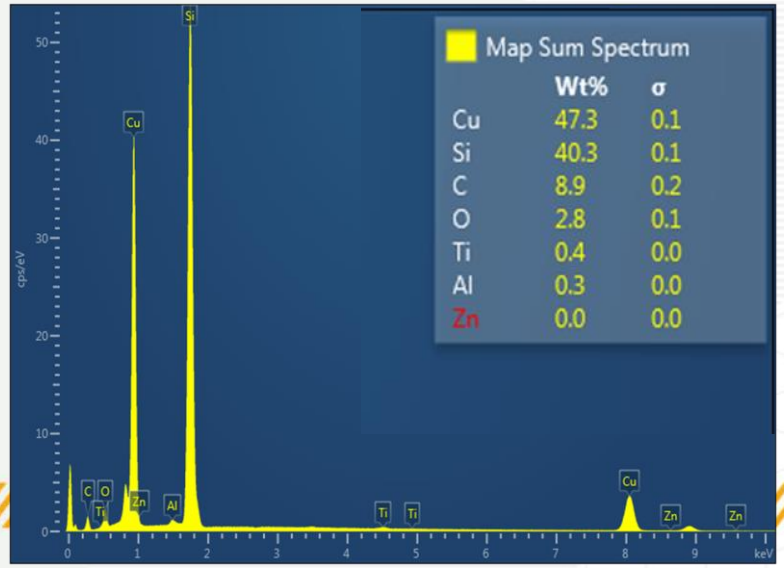
EDX Analysis of Sintered Joint









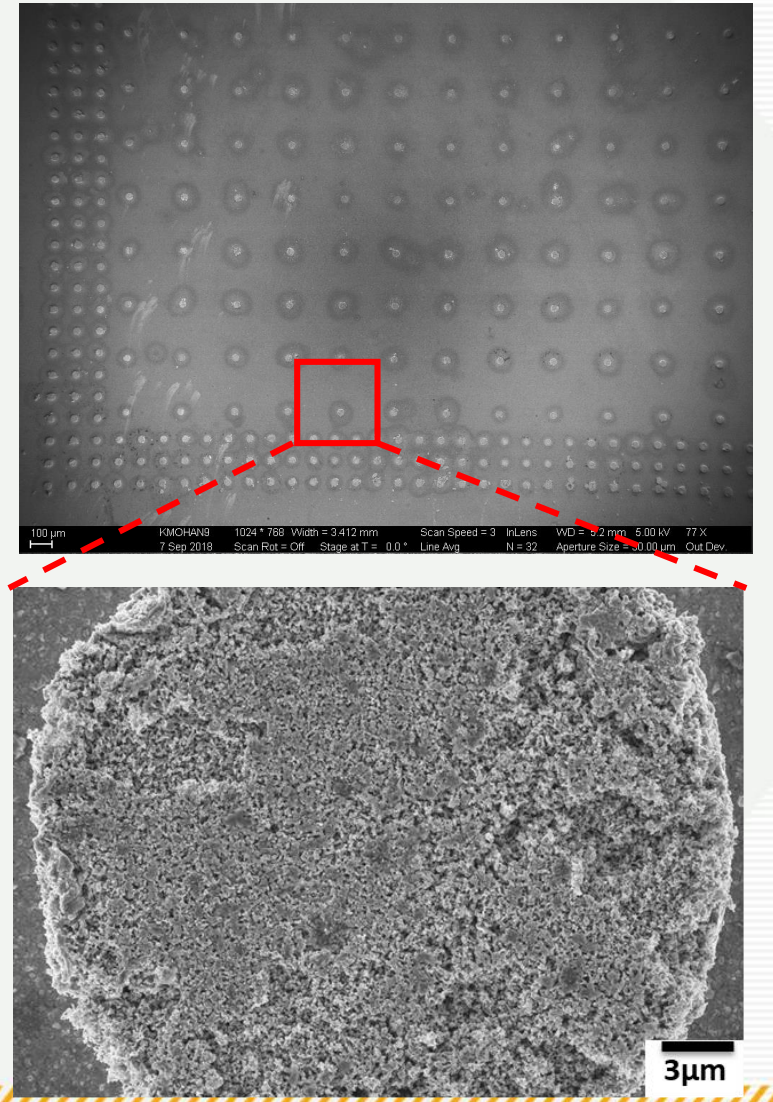


- **All-Cu joints**
- **Residual Zn<0.2%**

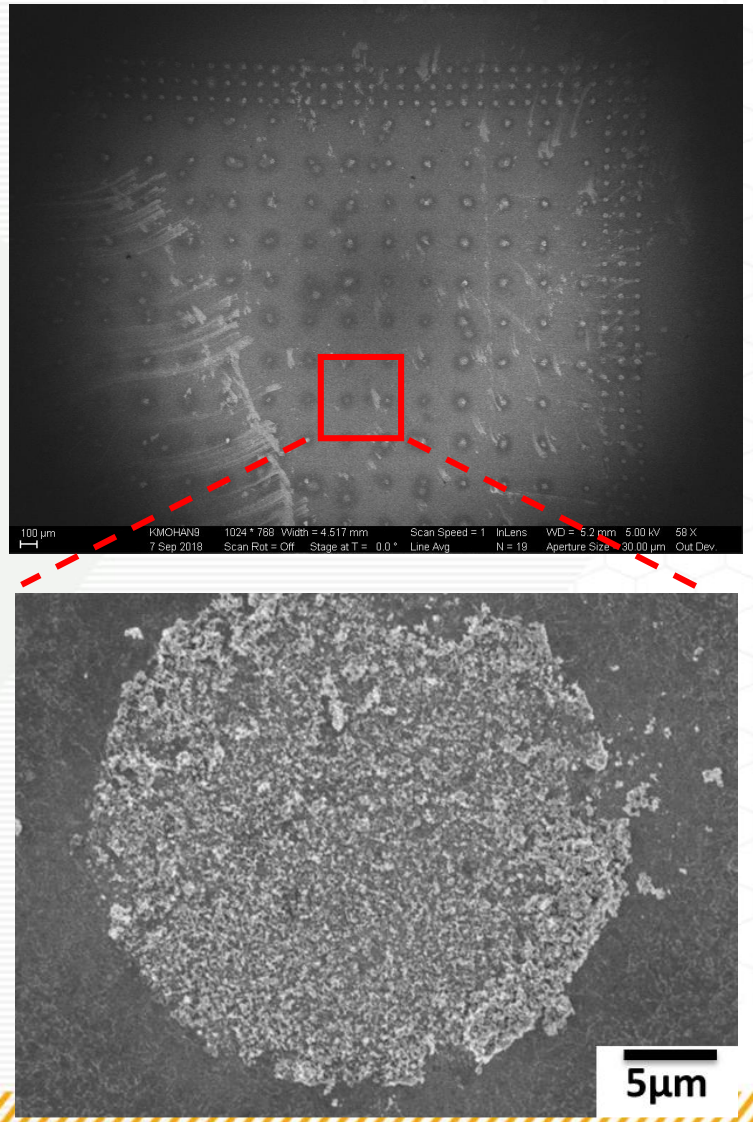
Data collected by K. Mohan

Fracture Interface Analysis after Die Shear Test

Die-side



Substrate-side



- **Failure within the sintered foam layer, not at the interface, signifying good metallurgical bonding between NP- and bulk-Cu**
- **NP-Cu caps were able to compensate for the variation in their heights as well as the surface roughness of the substrates**

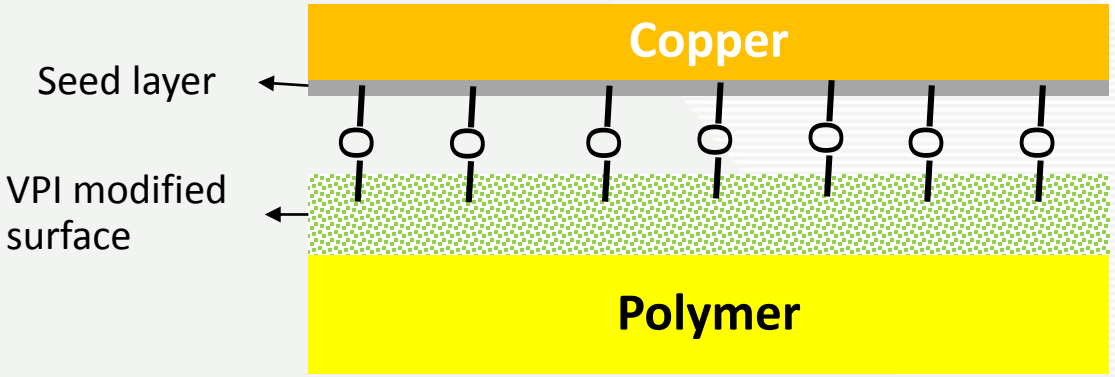
Data collected by K. Mohan

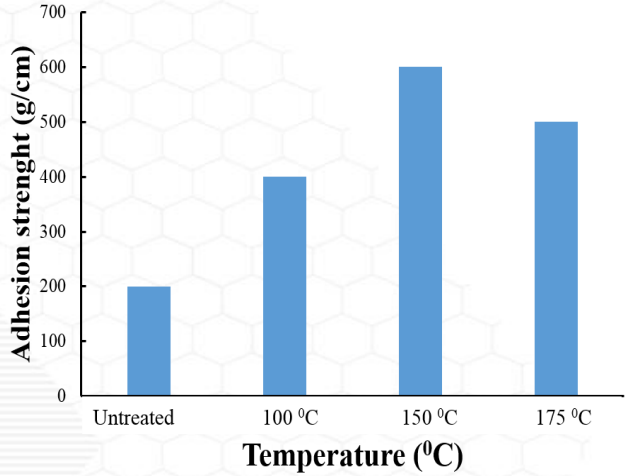
Improve Dielectric-Metal Adhesion: Vapor-Phase-Infiltration

Collaboration with Prof. Losego

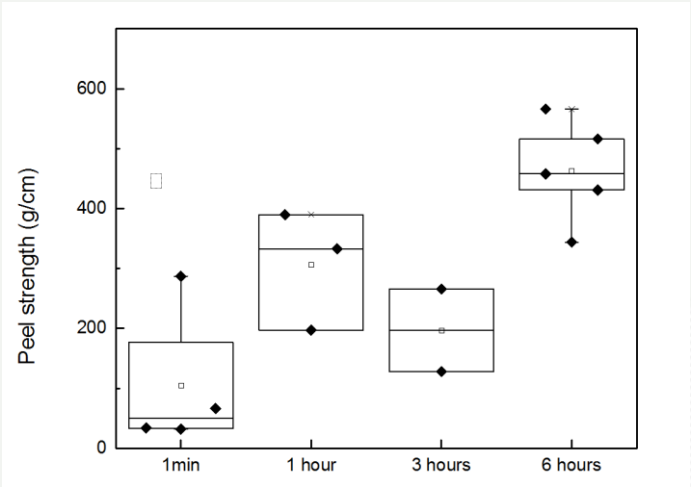
Georgia Tech

Adhesion improvement by chemical modification

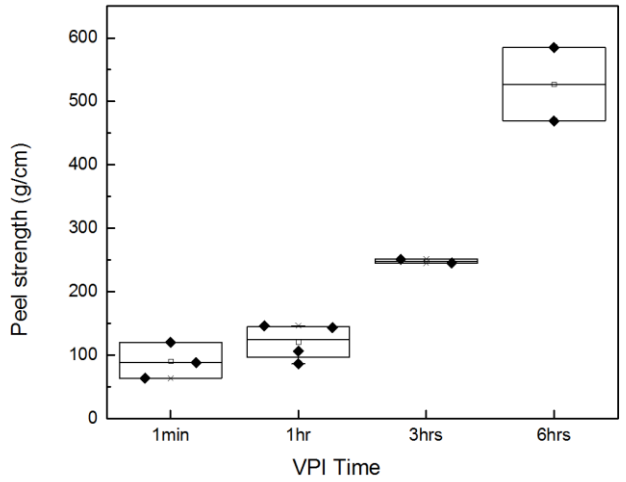




VPI Temperature 120 C



VPI Temperature 150 C



- Peel strength increases with time of infiltration, indicating that more exposure to precursor is favorable