Quilt Packaging® For Power Electronics

21 March 2013

Jason M. Kulick

President, Co-Founder

Indiana Integrated Circuits, LLC

Indiana Integrated Circuits LLC

Overview

- Introduction
- Quilt Packaging (QP) technology
  - Concept
  - Examples
  - Advantages
  - QP progress in power

Indiana Integrated Circuits, LLC (IIC)

Formed to commercialize QP

- Located in South Bend, IN
- Licensing/prototyping biz model
- Successive funding rounds through Series A (8/2012)
- Steady growth in QP & R&D

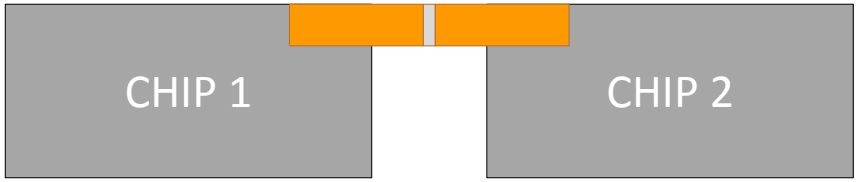
Contract R&D Experience:

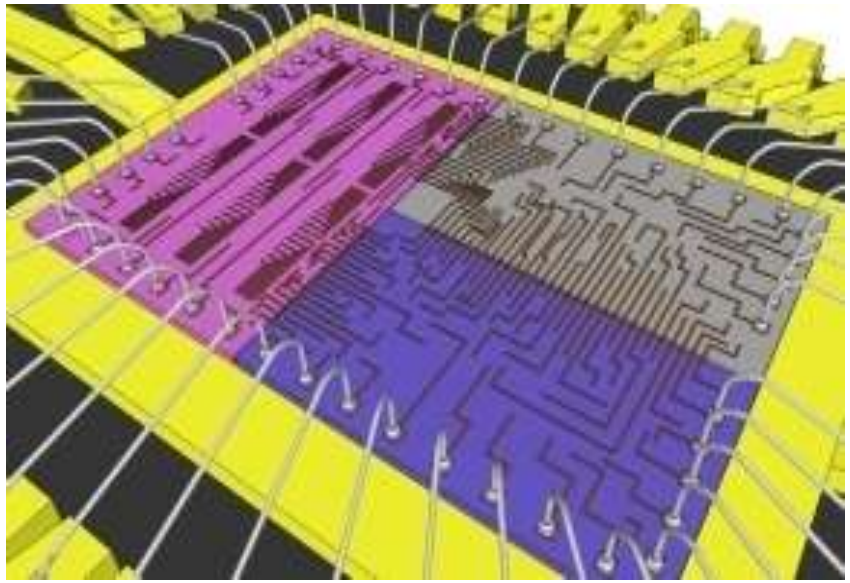
- E-Beam Lithography
- Specialty Plating
- DRIE & ICP etching
- IC & MEMs prototyping
- Magnetics/nanomagnetic fabrication & testing

Indiana Integrated Circuits LLC

Quilt Packaging (QP) Technology

- Edge-connections joined to create multi-chip “quilt,” developed at Notre Dame
- “Monolithic” assemblies from same or disparate materials & process technologies
- Extremely low impedances
- Enables optimization for cost and functionality
- Industry-standard tools and fabrication processes

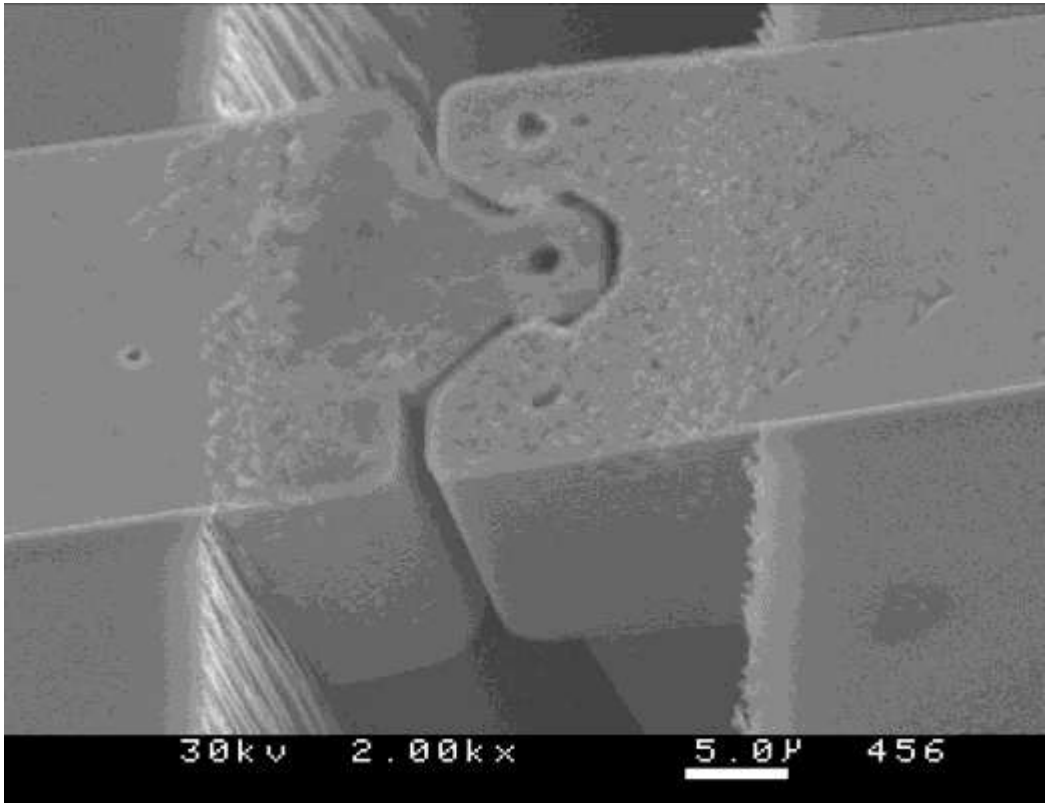




Indiana Integrated Circuits LLC

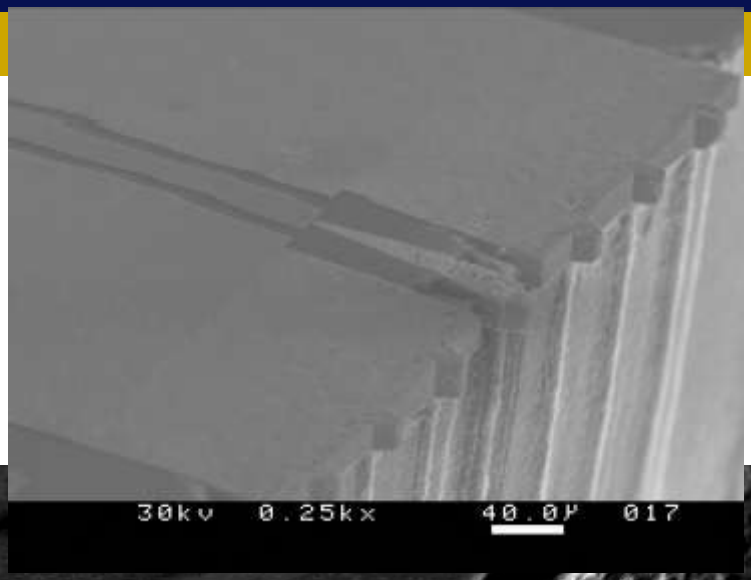
QP-Interconnect Structures

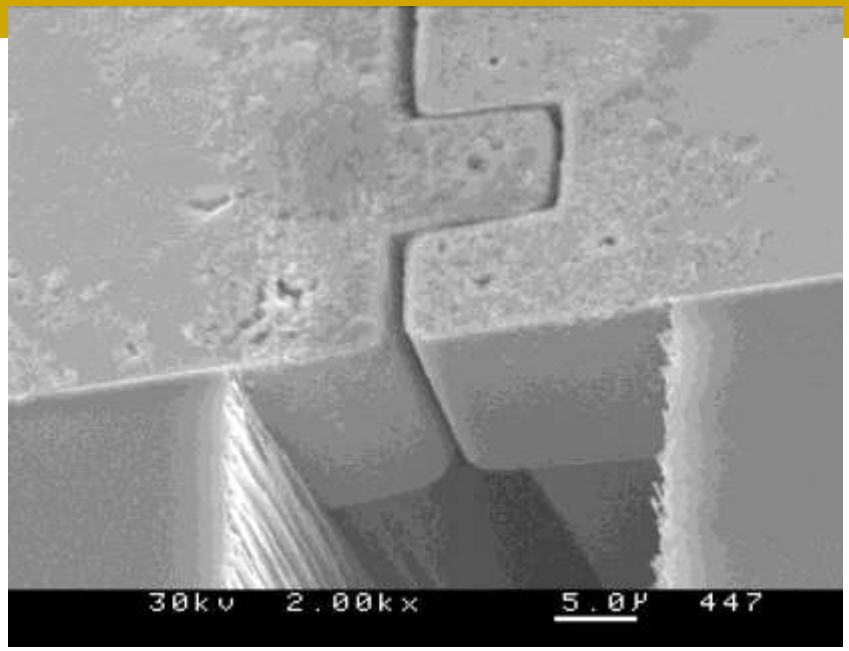
- Edge connection structures called “nodules”
- Solid metal, typically 10-200 um wide, ~ 20-50 um thick
- Customizable shapes-including interlocking-enables sub-micron chip alignment

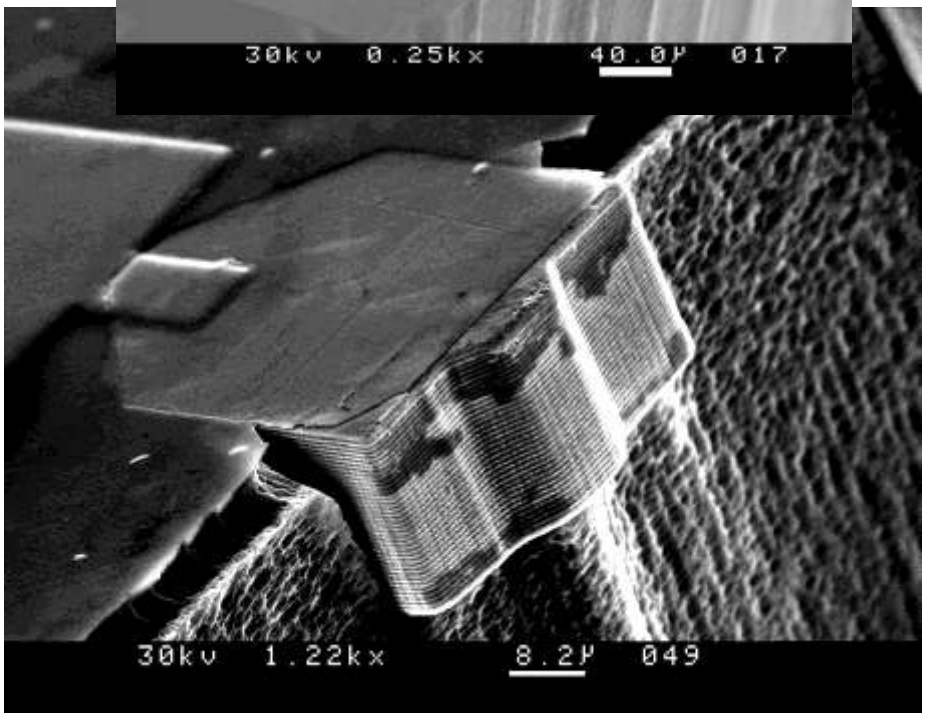


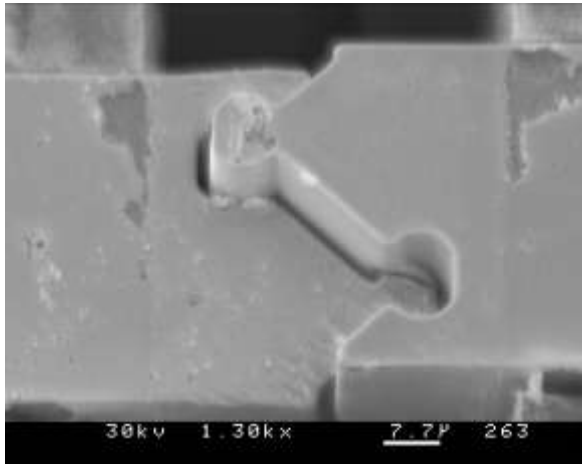
Indiana Integrated Circuits LLC

QP Customizable I/O



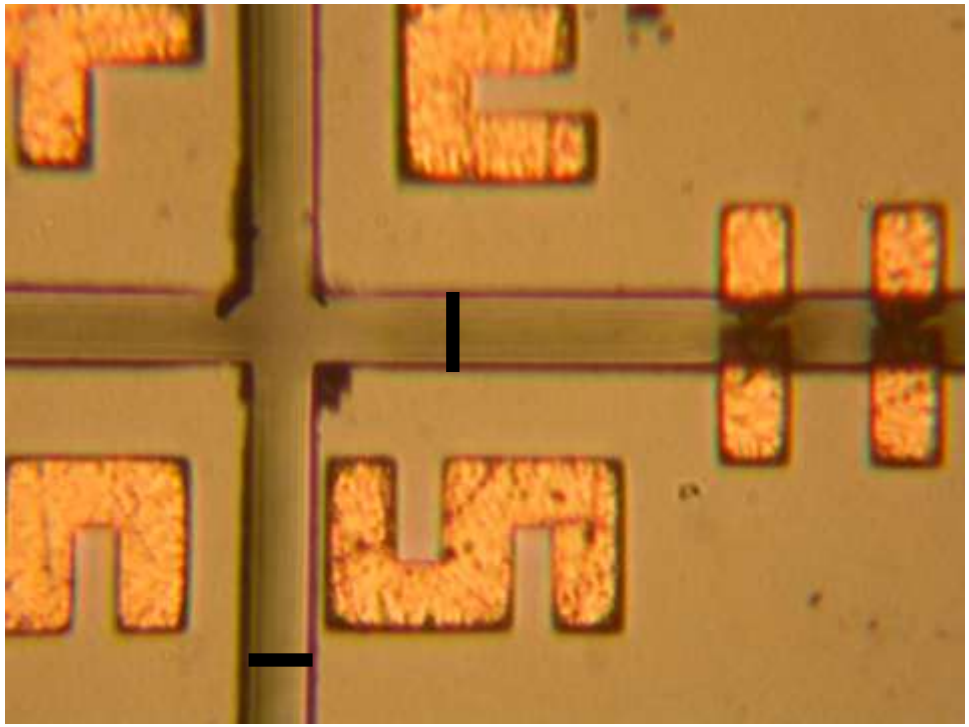




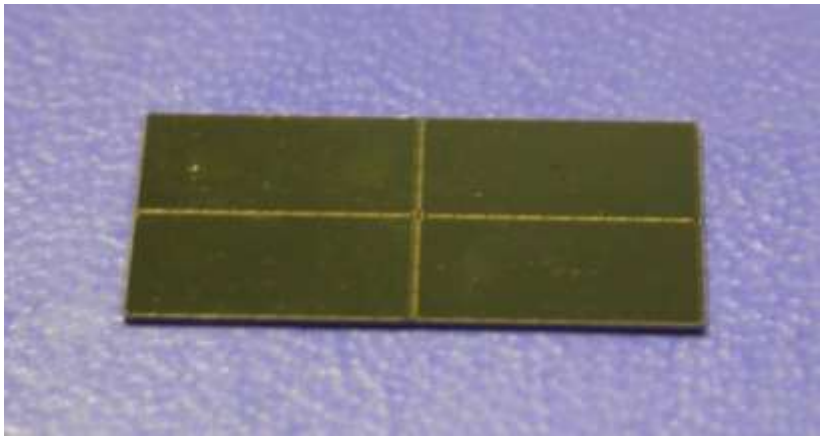


Indiana Integrated Circuits LLC

Sub-Micron Chip Alignment



= 30 micron



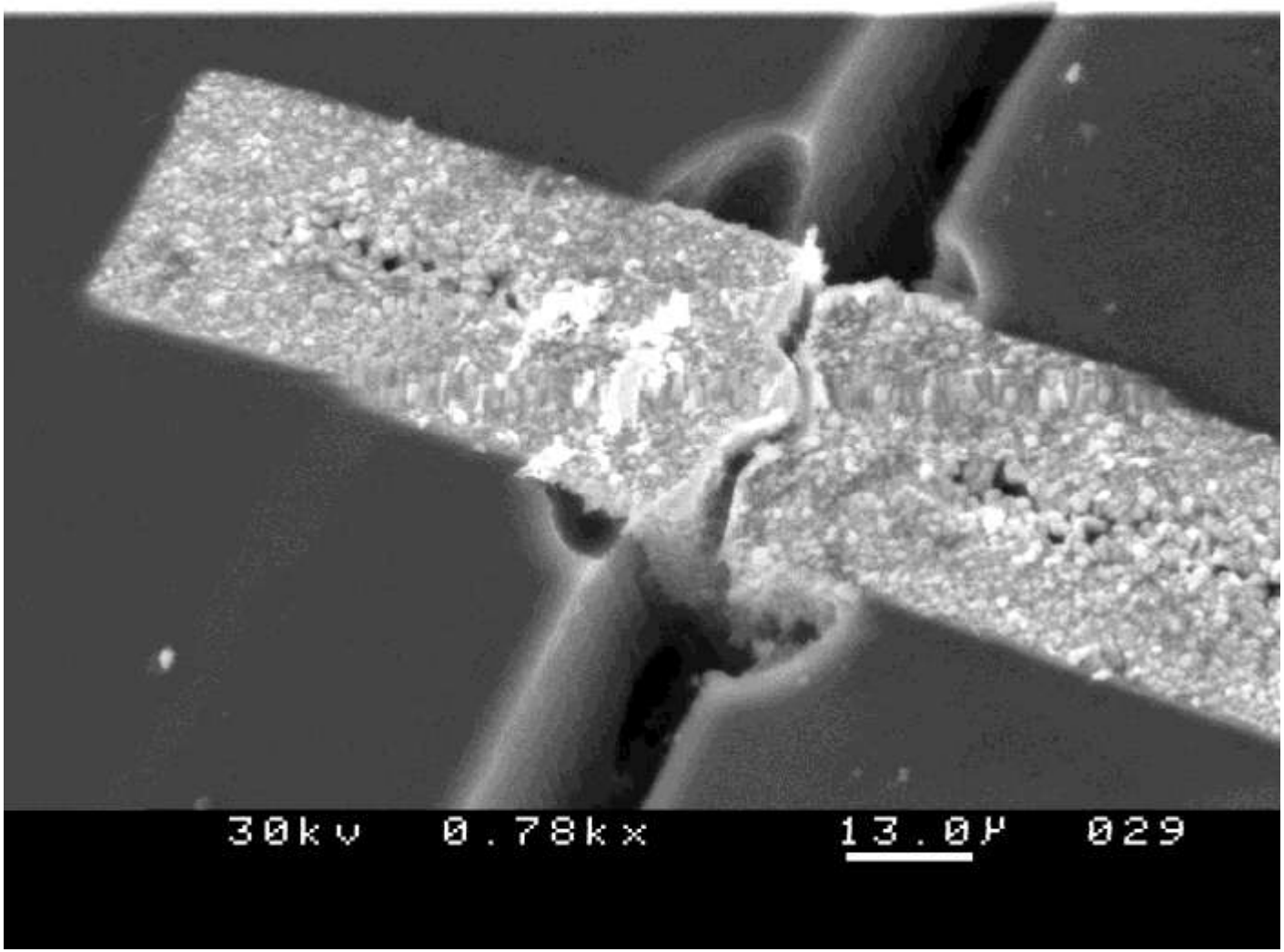
Interior (left) of four-chip quilt (above)

QP enable extremely accurate alignment

Indiana Integrated Circuits LLC

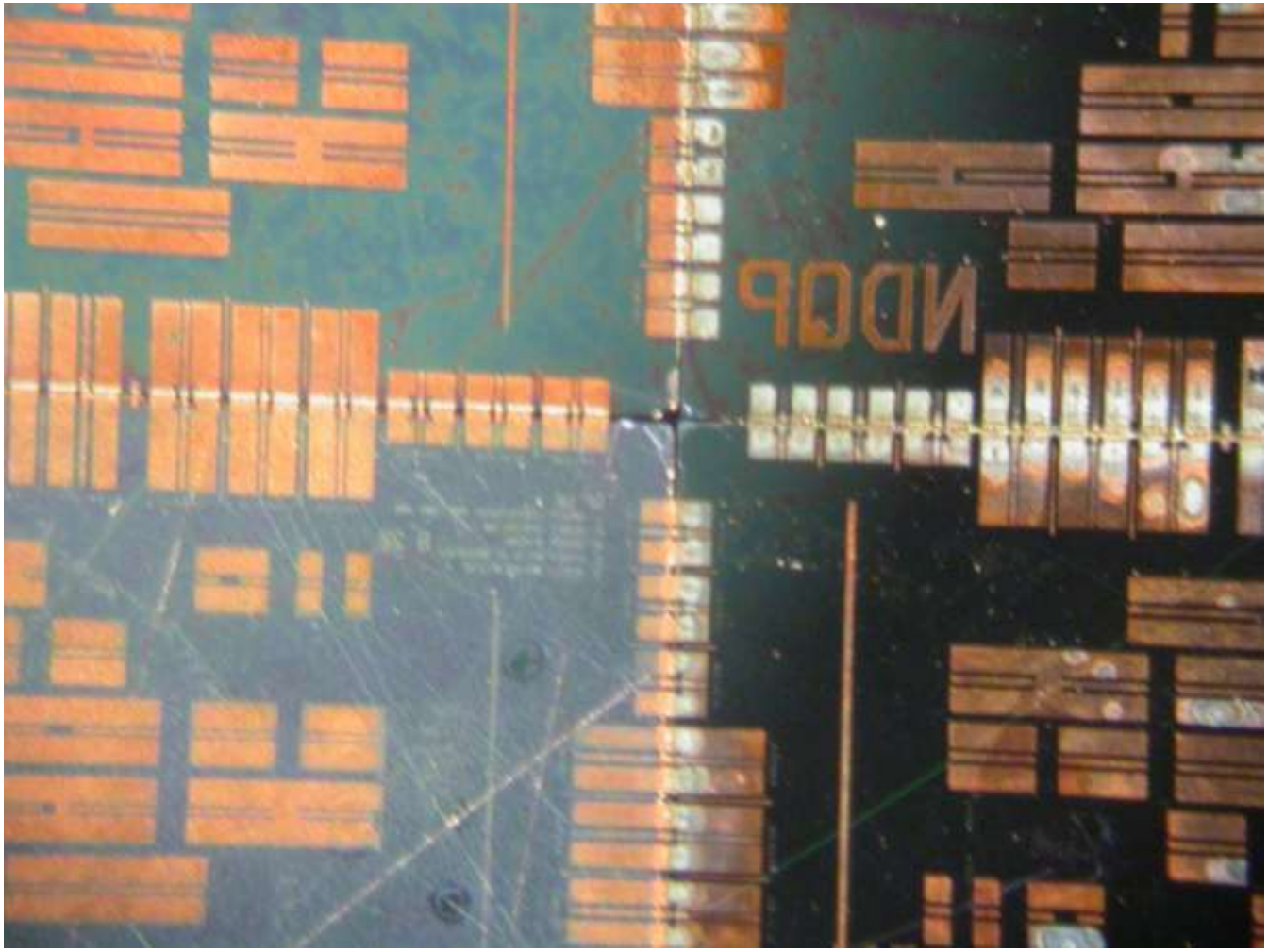
Si QP 2x2 Array (1 in^2 chips)

~15 um gap post-solder



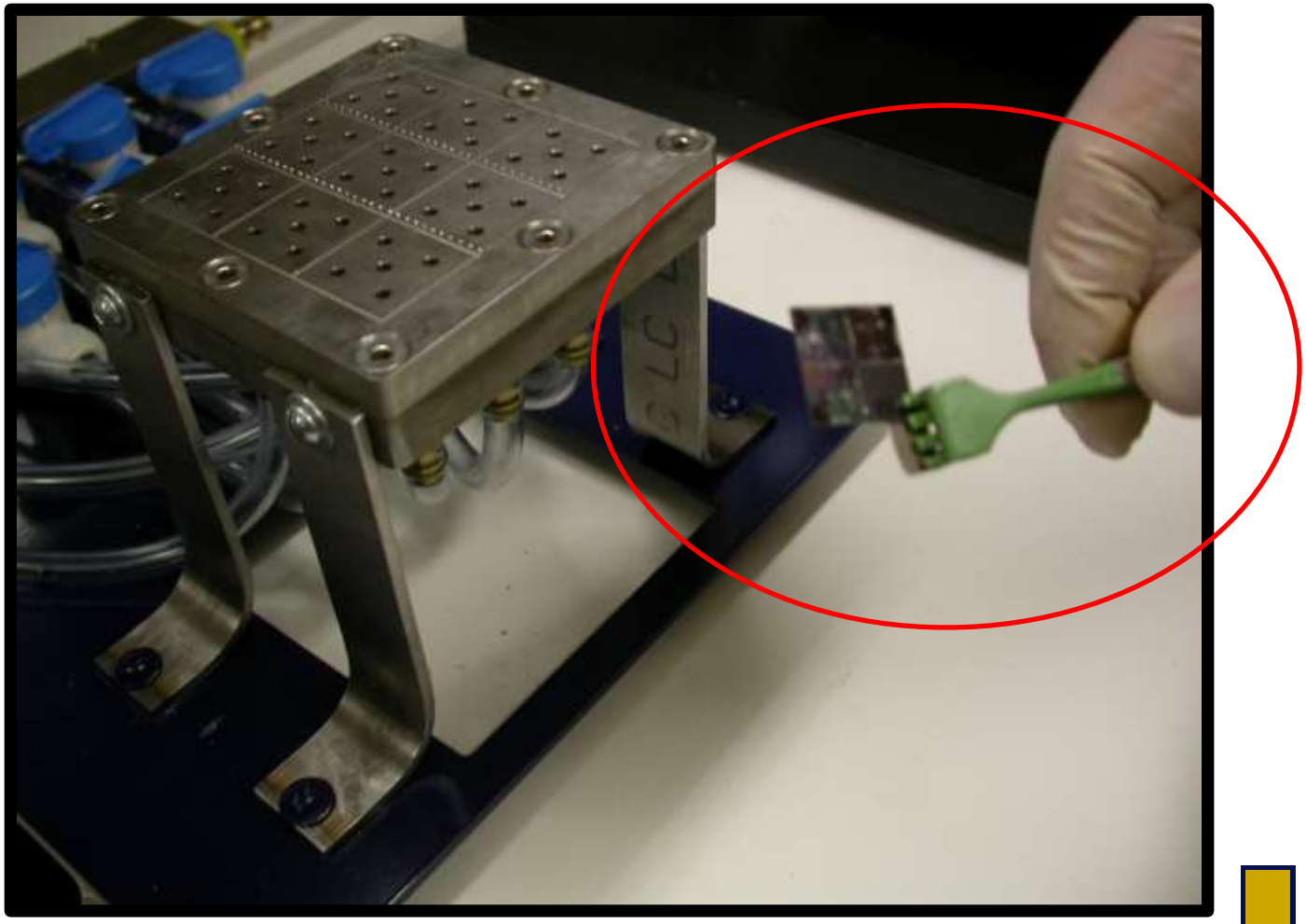
Indiana Integrated Circuits LLC

Inner seam of 4-chip Si test quilt

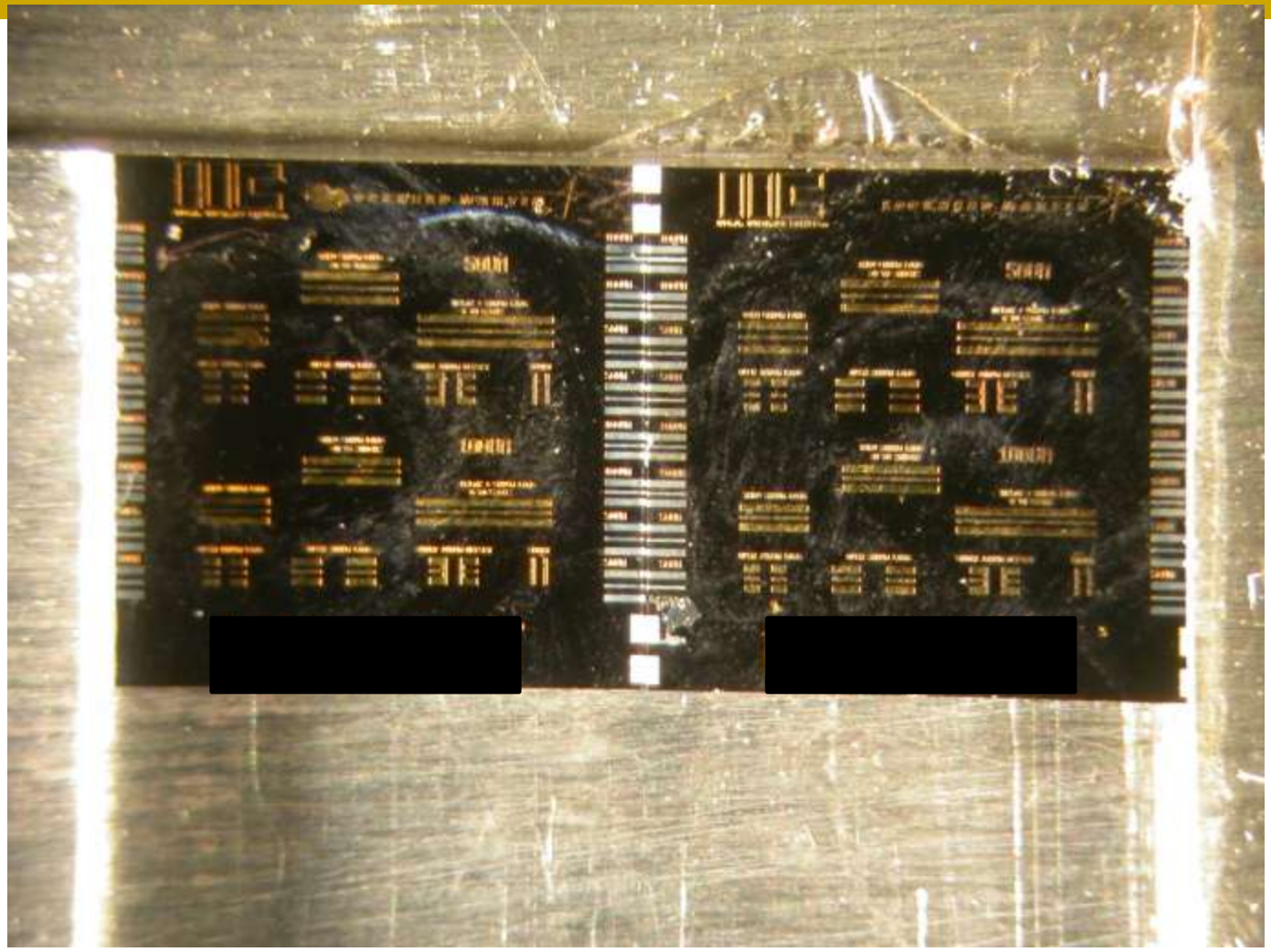


Indiana Integrated Circuits LLC

4-chip quilt mechanically strong



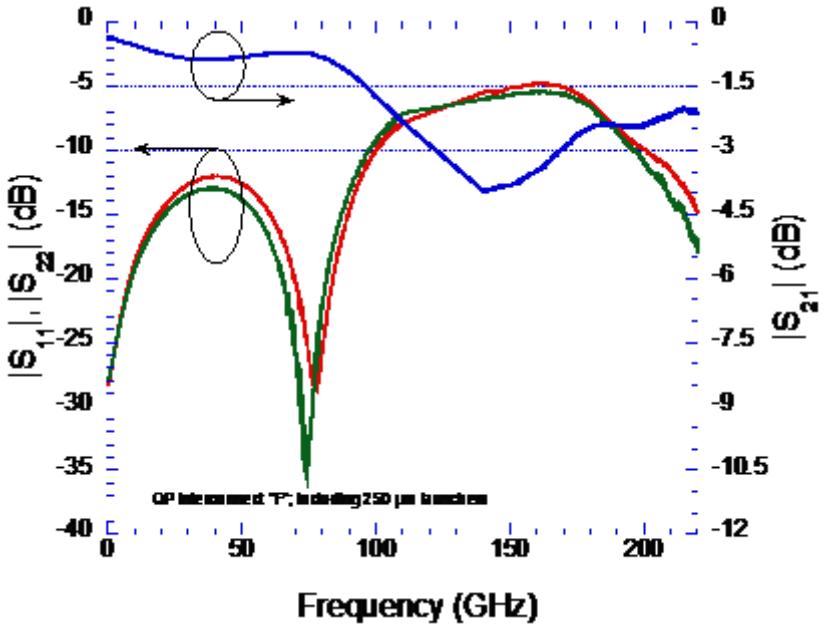
GaAs QP Chipset



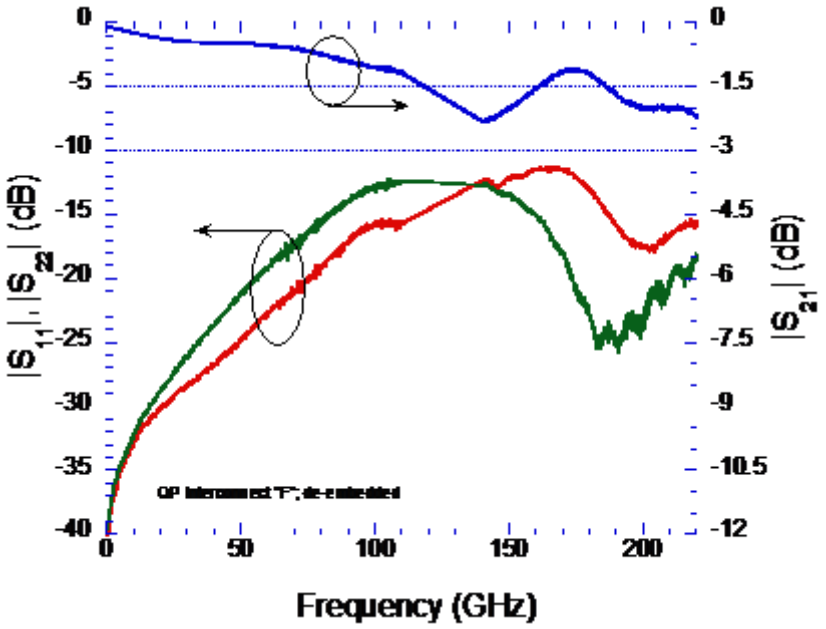
Indiana Integrated Circuits LLC

GaAs Measurement Data Sample

Raw S-parameters



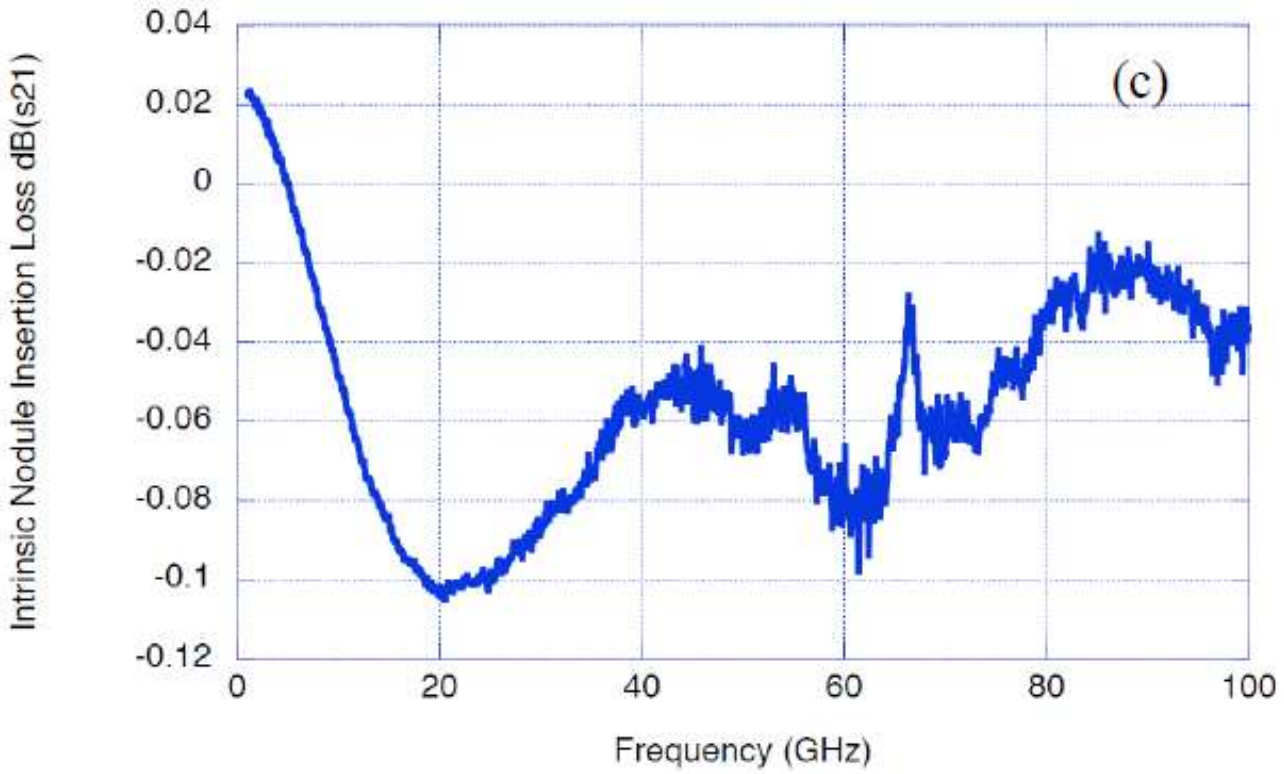
De-embedded S-parameters



*Less than 3 dB insertion loss at 220 GHz

Indiana Integrated Circuits LLC

QP Microwave Performance

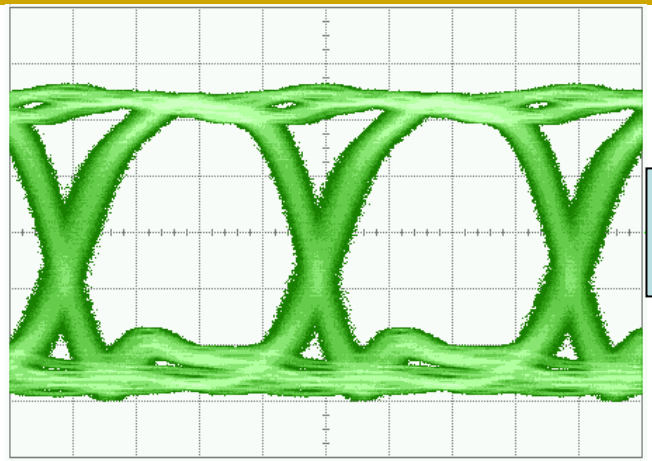


Less than 0.1 dB insertion loss from 50 MHz past 100 GHz, with no resonances. Recent unpublished results under 0.9 dB at 180 GHz

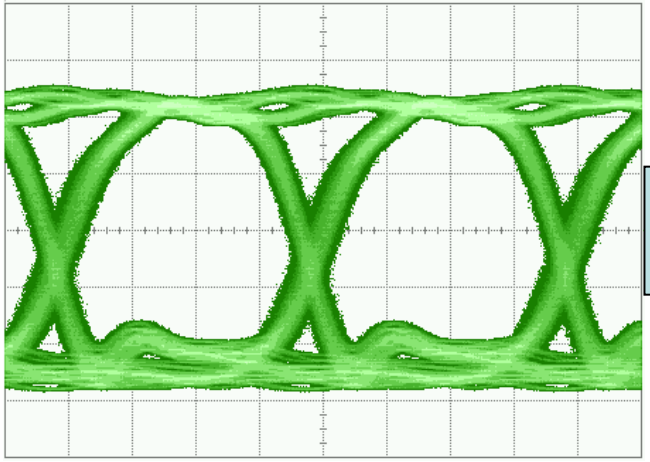
Indiana Integrated Circuits LLC

QP Eye diagrams

- Measurement of 12 Gb/s eye pattern (Anritsu MP1763B)
  - Horiz. 100 mV/div
  - Vert. 20 ps/div
- Data stream: 2^{31}-1 pseudo-random bit sequence
- Nearly ideal interconnect performance; indistinguishable from PG.
- Error-free operation
  - SNR (Q) = 12.9 for pattern generator alone, 12.4 after chip-to-chip interconnect



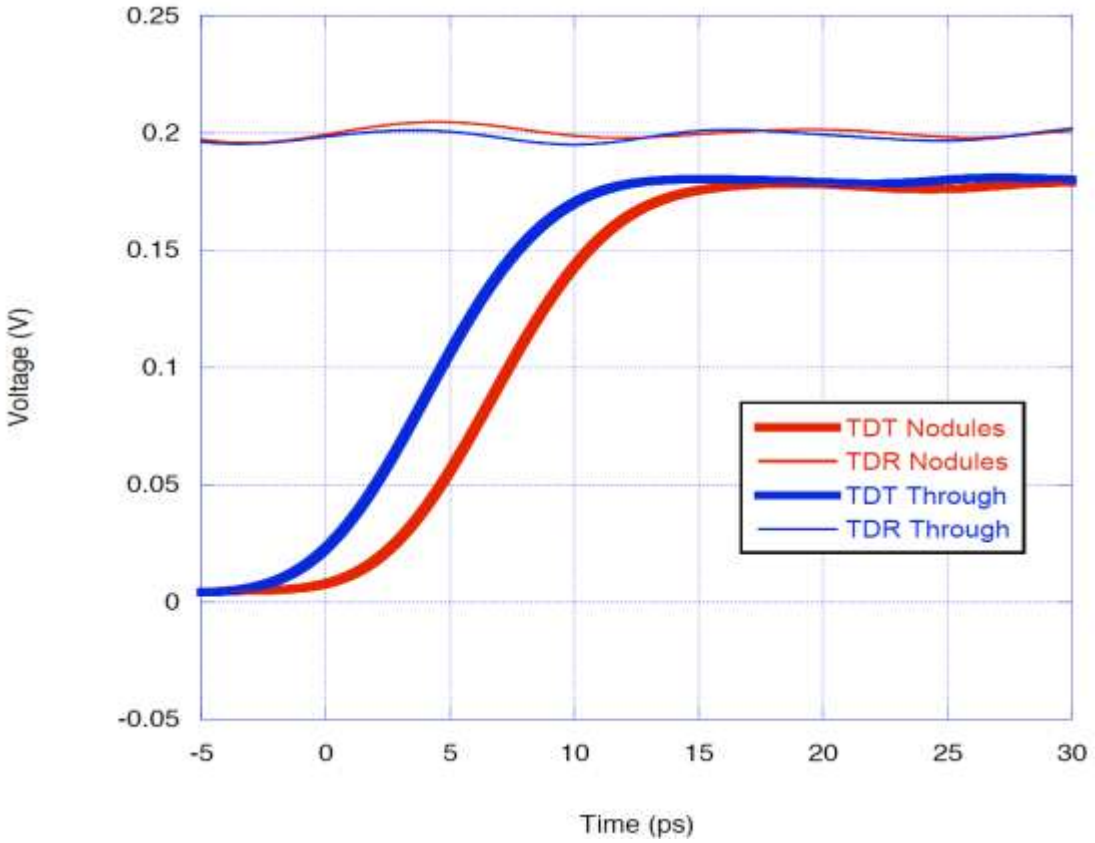
Raw pattern generator



50 µm GSG eye

QP Time-Domain Performance

- Single-ended GSG CPW configuration
- Picosecond Pulse Labs 4022 TDR pulse enhancement module: < 9 ps risetime
- Total delay including probe pads, launcher: 7 ps (820 µm length)
- Delay due to QP nodules: 2.7 ps

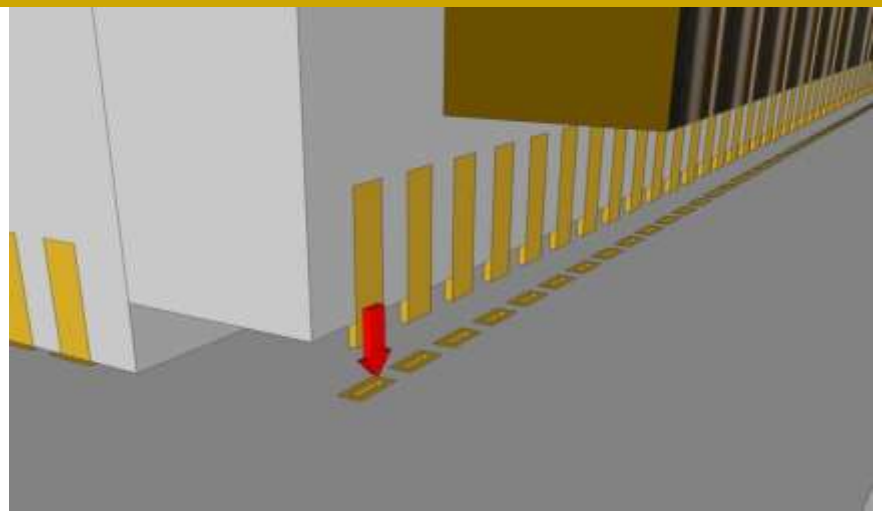


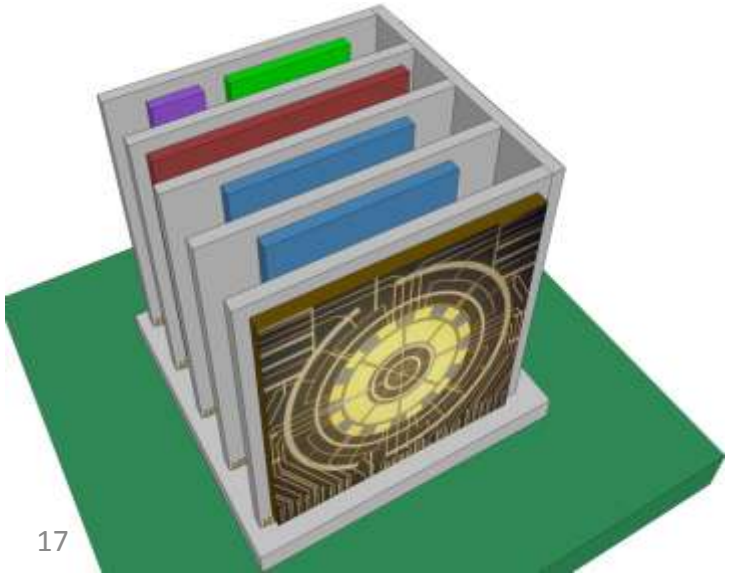
100 µm nodule compared with pads/launcher, GSG

Indiana Integrated Circuits LLC

“3D-QP” and “Interposers”

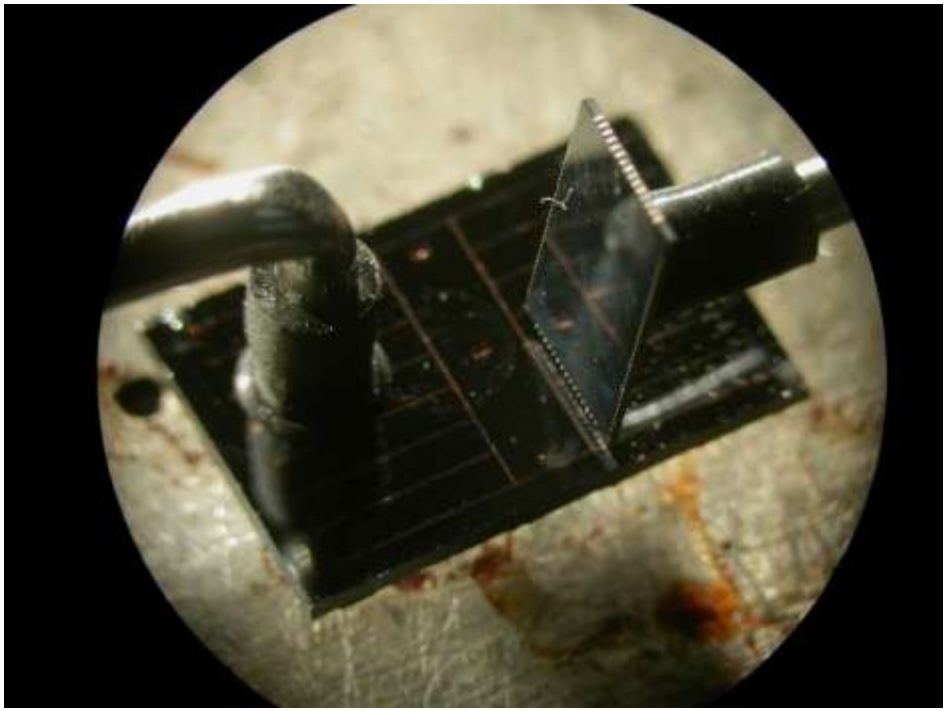
- QP can enable multiple 3D configurations
- 3D-QP retains many advantages of 2D-QP
- “Quilting” interposers can decrease form-factor
- Systems benefit from QP without having to redesign chips

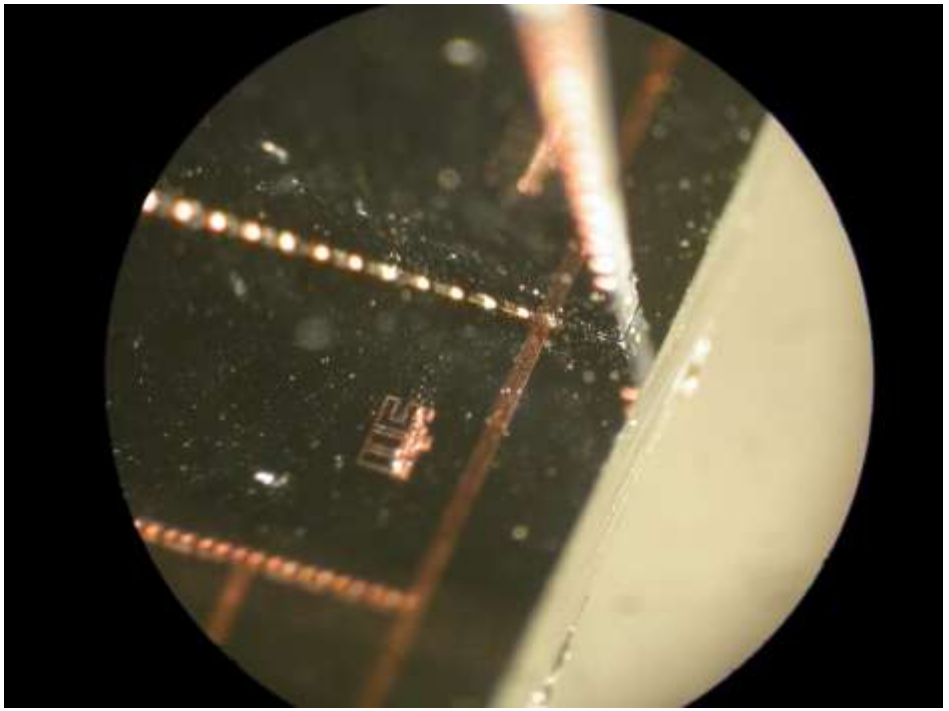




Indiana Integrated Circuits LLC

3D Si QP Test Articles

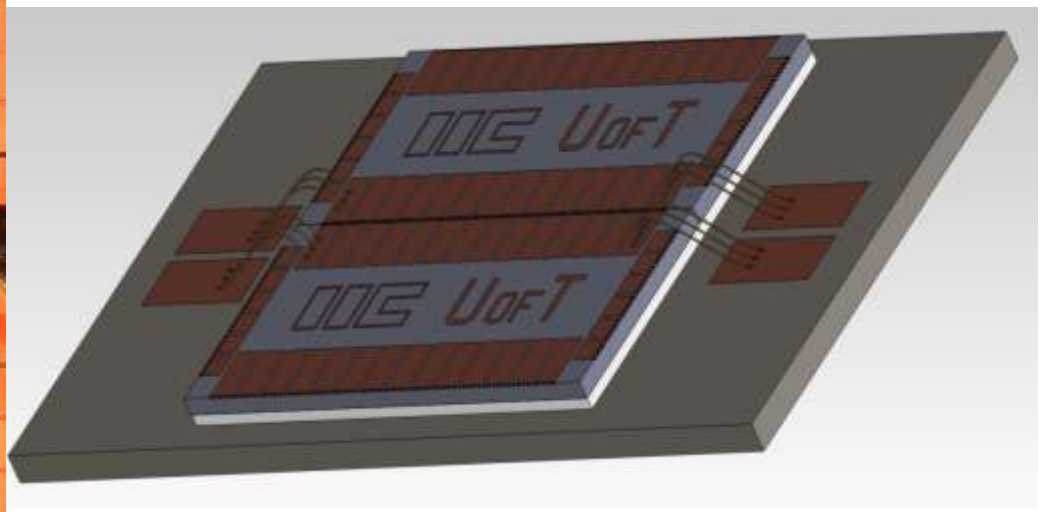




Advantages of Quilt Packaging

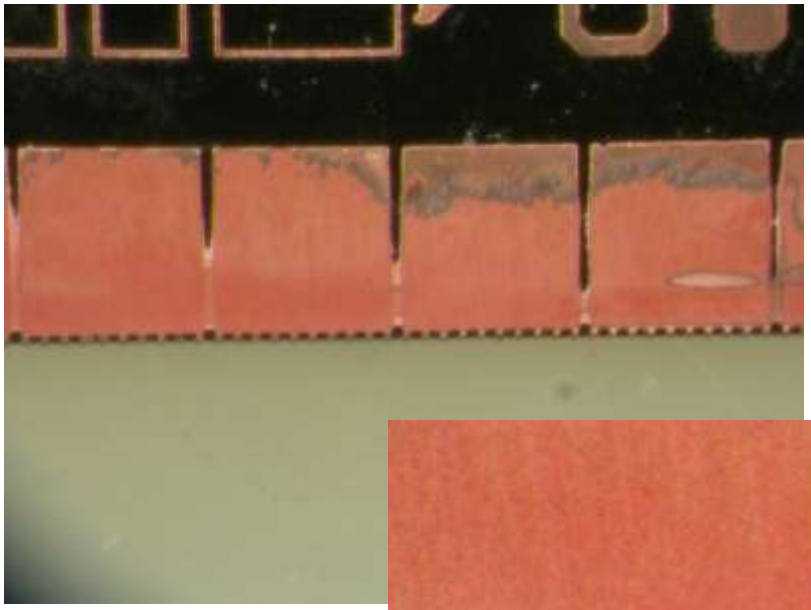
- Optimized integration of disparate materials and process technologies (Si, GaN, GaAs, AlN, more)
- Chip partitioning for optimal yield/functionality
- Increased cross-sectional area vs. WBs, bumps
- Better thermal management & failure modes compared to WB
- Reduced design time due to applicability of current 2-D tools, design re-use
- IP flexibility, security

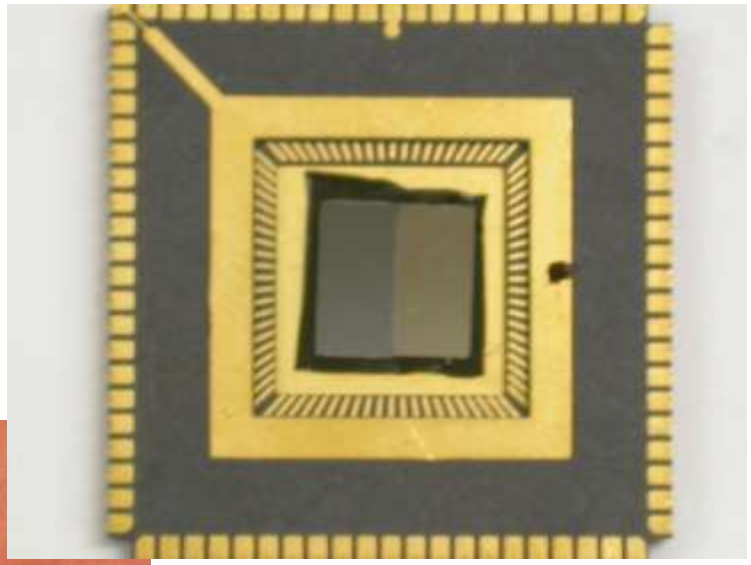
Original intent-test using wirebonds

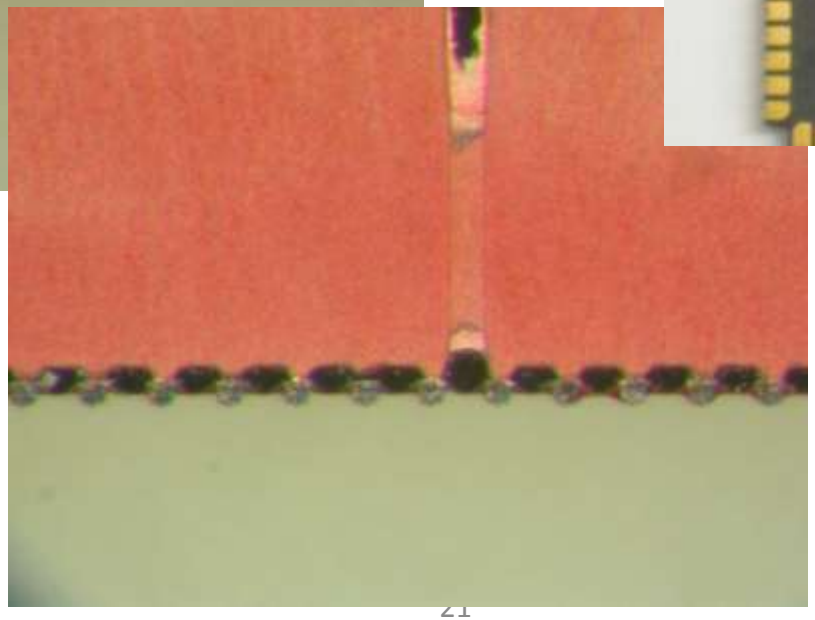


Indiana Integrated Circuits LLC

Early test articles--couldn't wirebond, had to probe directly

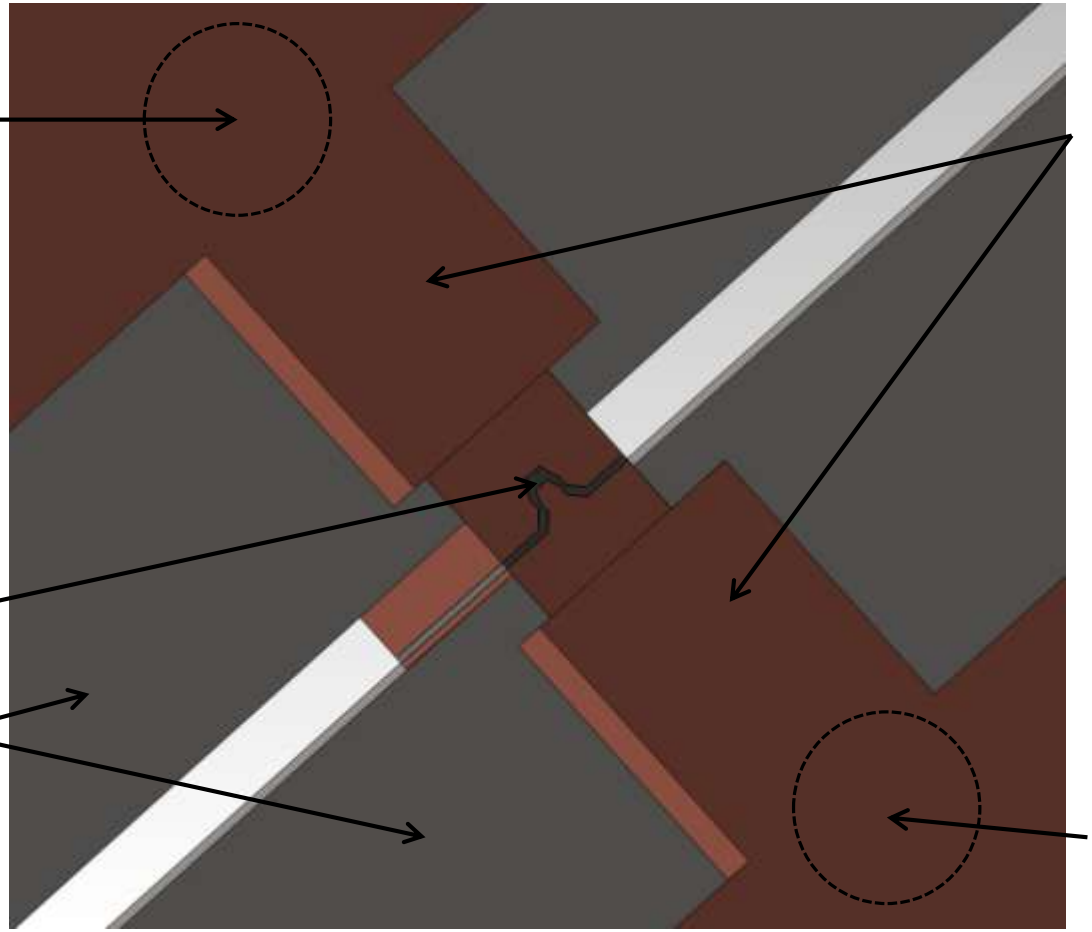






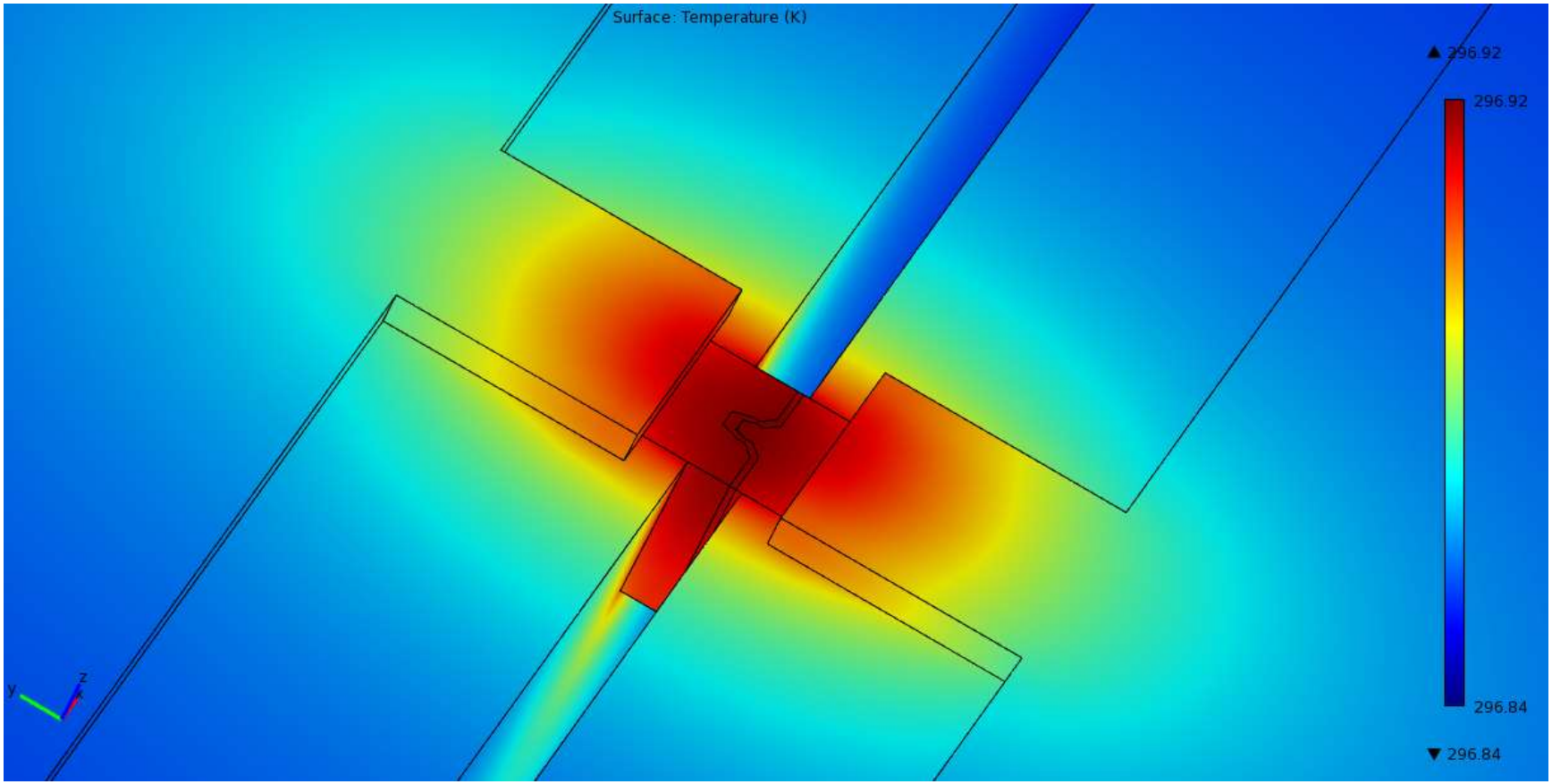
Indiana Integrated Circuits LLC

Joule heating simulation through nodules interconnect (setup)



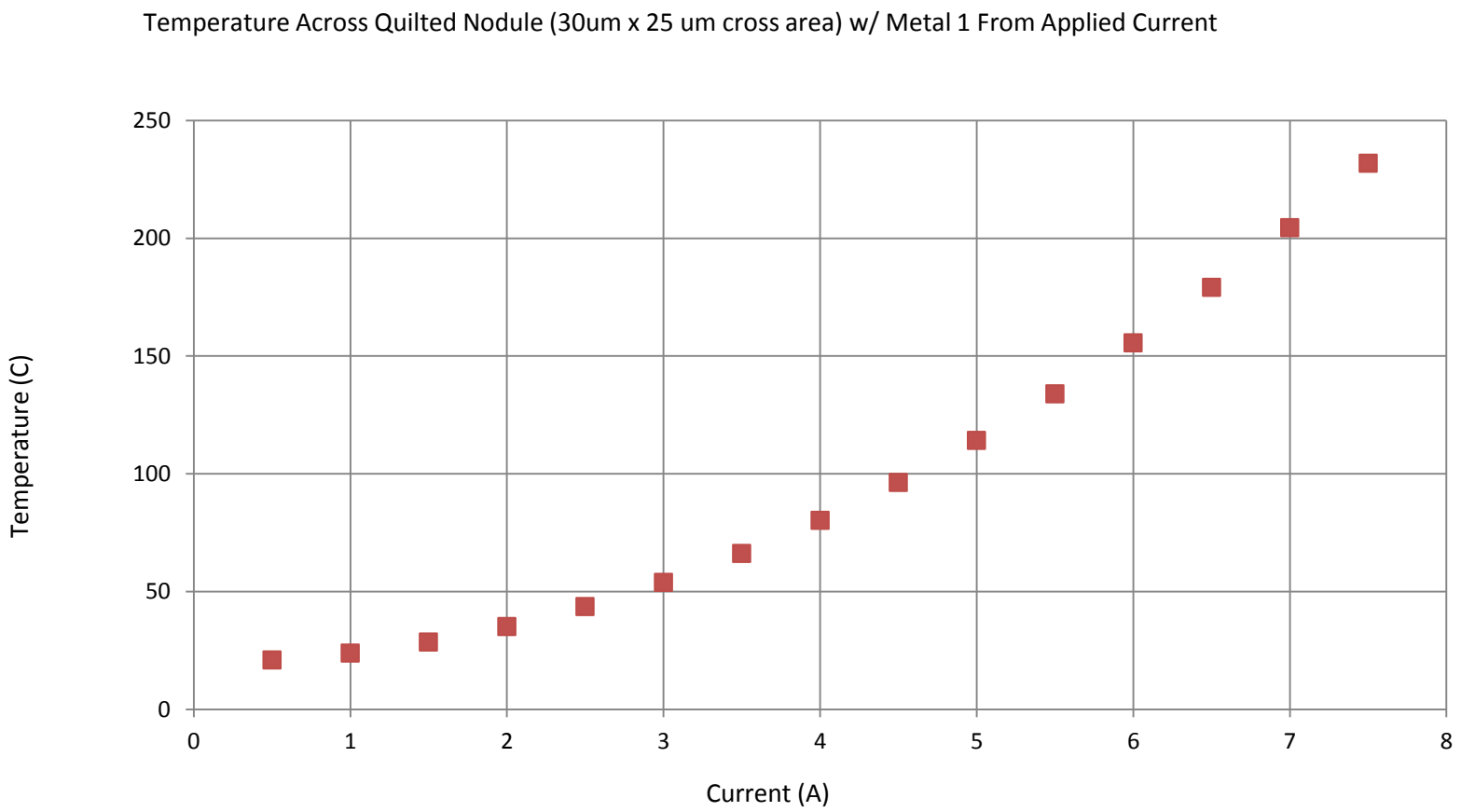
Indiana Integrated Circuits LLC

Joule heating simulation through quilted interconnect (no showstoppers)



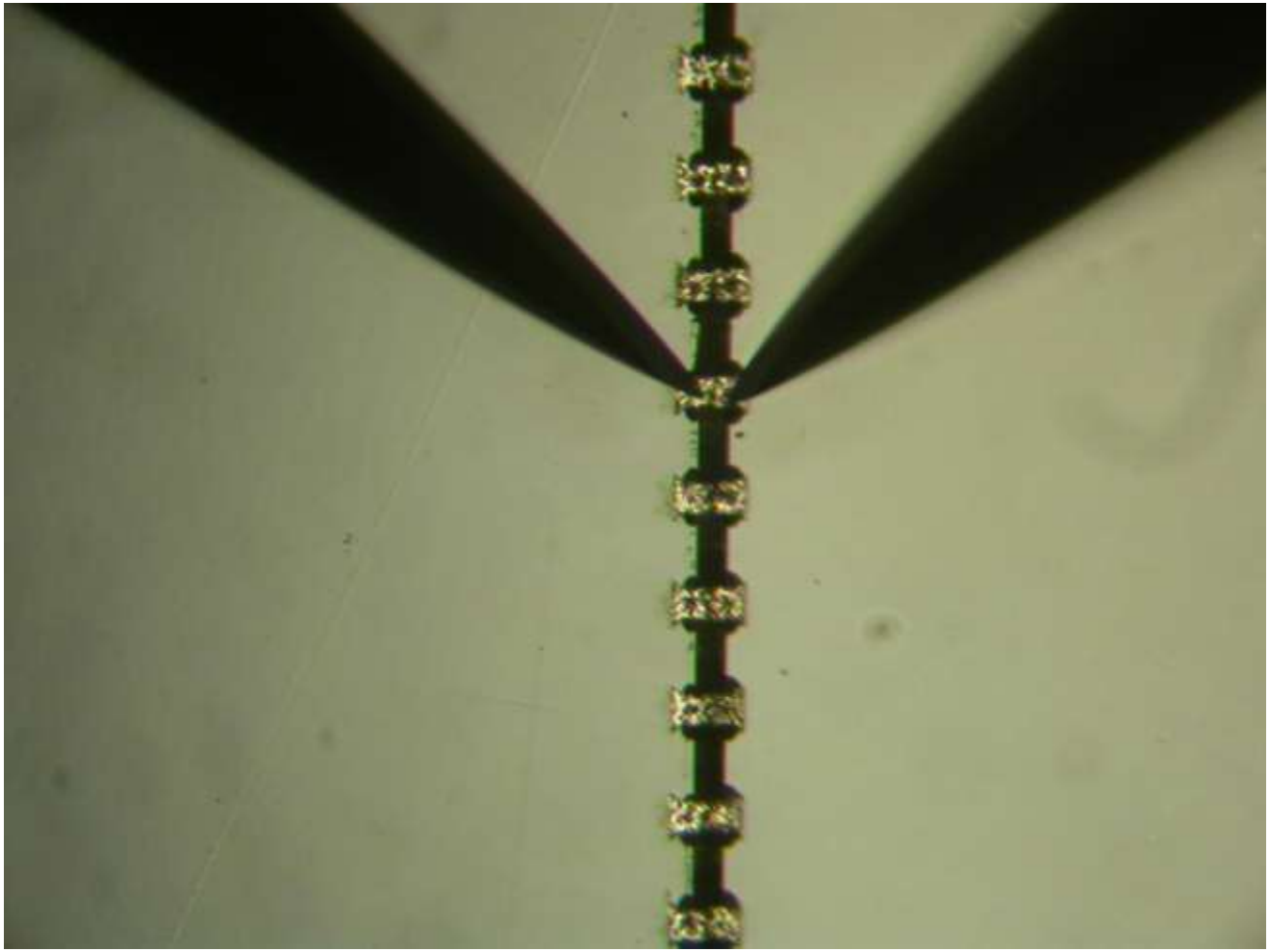
Indiana Integrated Circuits LLC

Simulations don’t include heatsink, nodule size 30 um X 20 um

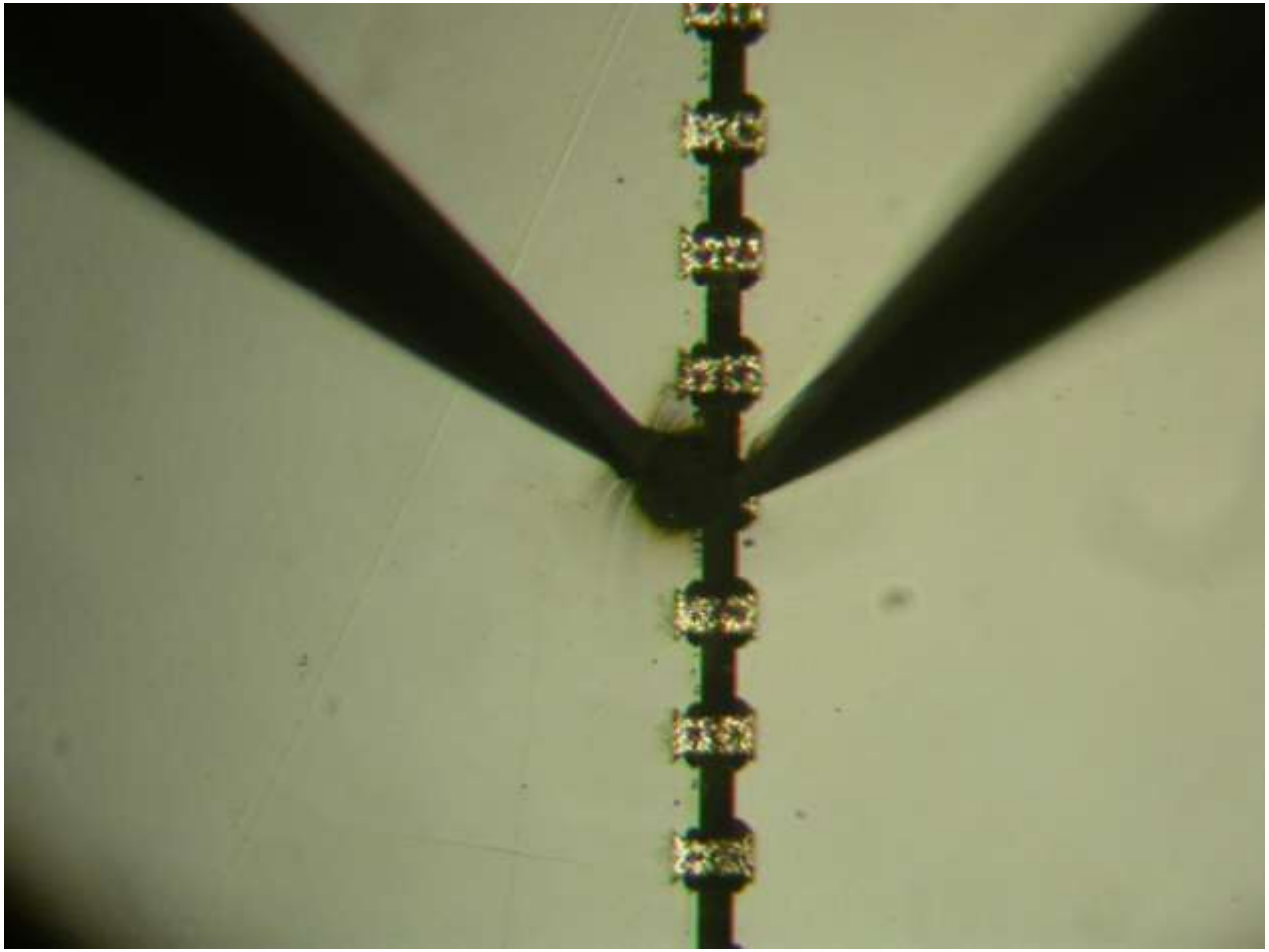


Indiana Integrated Circuits LLC

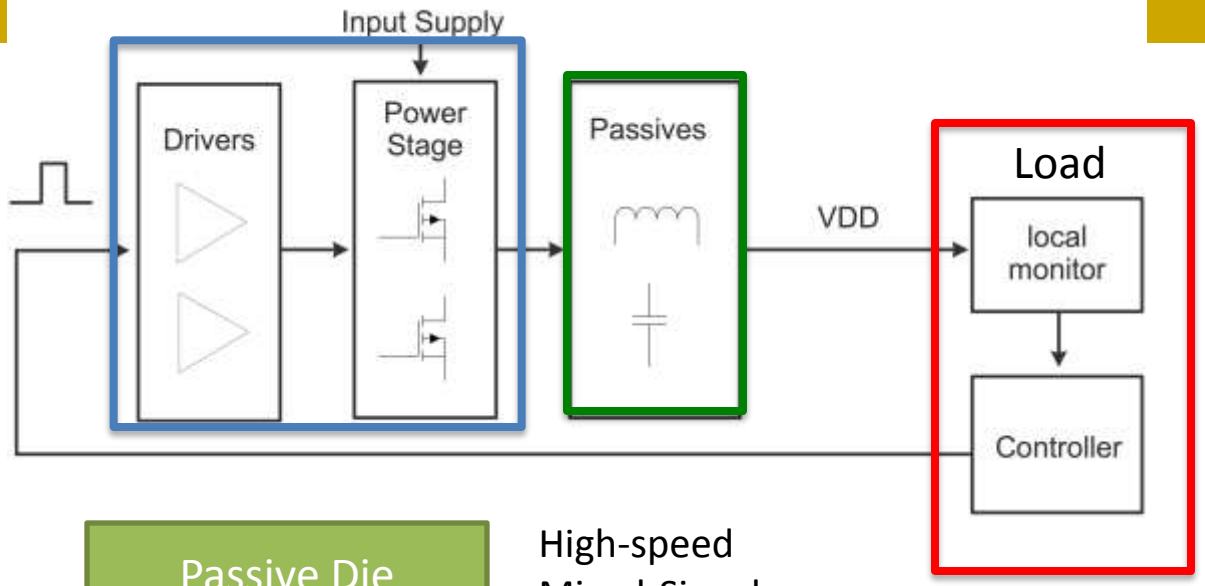
Si QP Max current probe test (before), nodule size 30 um X 20 um



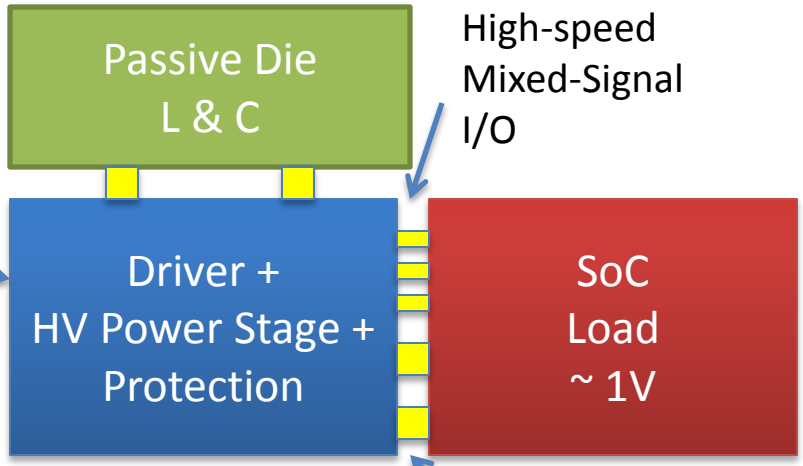
Si QP Max current test--probes fail before nodules (~2.25A)



Potential Uses of QP In Power Electronics



Low-cost
Power-optimized
12V BCD



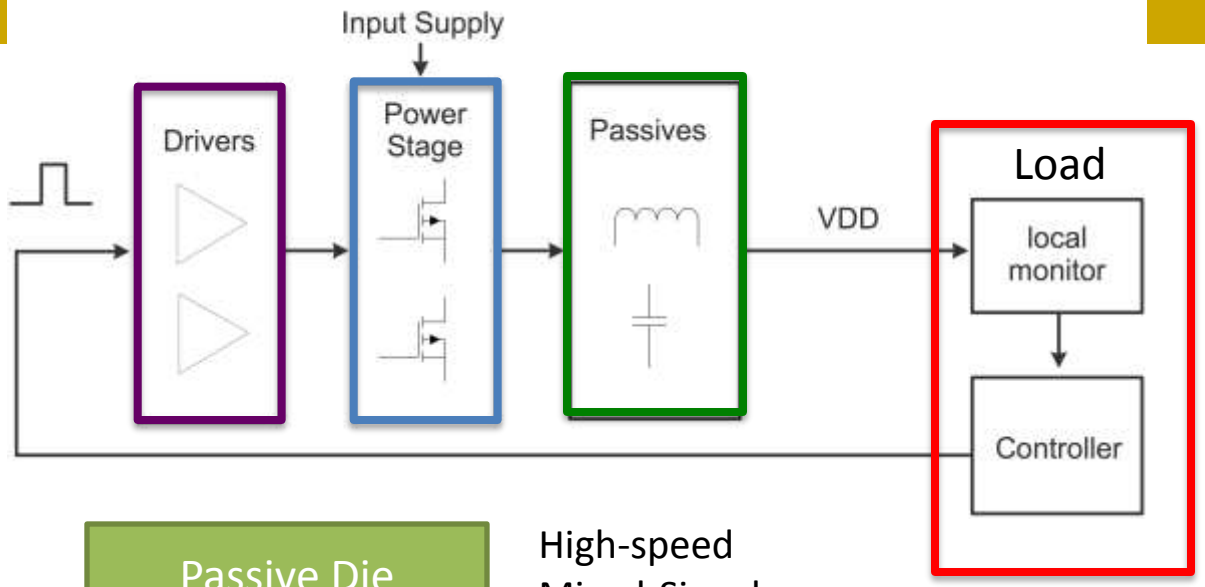
High-speed
Mixed-Signal
I/O

Digital optimized
CMOS

High-current, low ESR, ESL Power Connection

Indiana Integrated Circuits LLC

Potential Uses of QP In Power Electronics



Low-cost CMOS or BCD

Passive Die
L & C

High-speed Mixed-Signal I/O

Optimized High-Speed Driver + Protection

HV GaN/GAs Power Stage

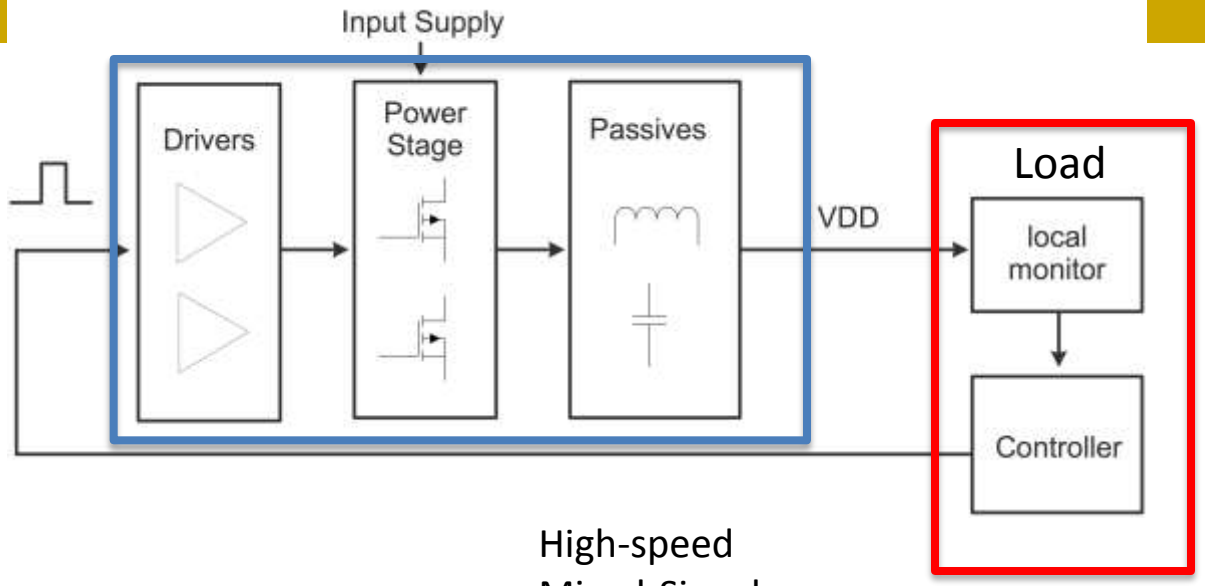
SoC Load ~ 1V

Digital optimized CMOS

High-current, low ESR, ESL Power Connection

Indiana Integrated Circuits LLC

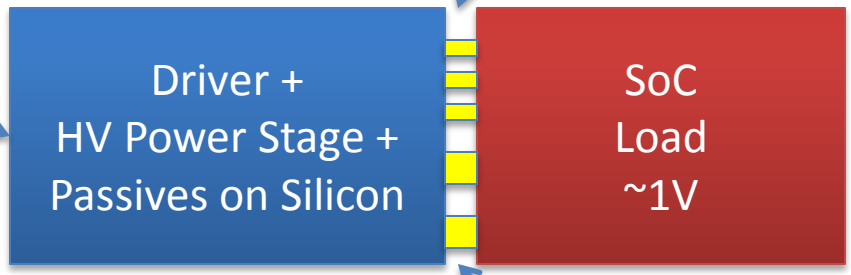
Potential Uses of QP In Power Electronics



BCD or
GaN/GAs with
On-chip drivers

High-speed
Mixed-Signal
I/O

Digital optimized
CMOS



High-current, low ESR, ESL Power Connection

Indiana Integrated Circuits LLC

Future Work

- Thermal cycle/shock testing of preliminary "quilts" (ongoing)
- Completion of DC-DC converter demonstration (3-chip quilt w/QP Si interposer---ongoing)
- GaN QP (just starting)
- Chip architectures & partitioning for power
- Other?---Specific partner applications, etc.

Thank You!

For More Information Contact:

Jason Kulick

jason.kulick@indianaic.com

(574) 217-4612

And/or visit:

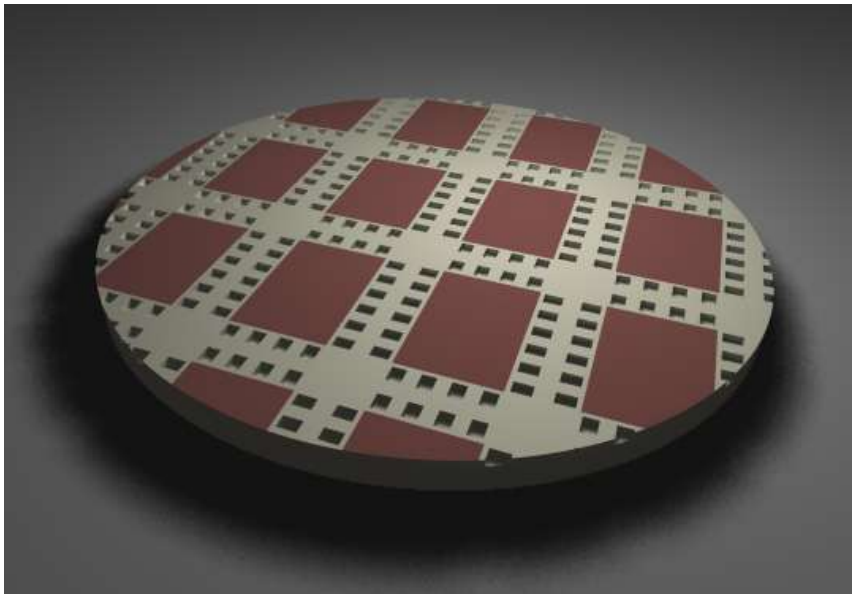
www.indianaic.com

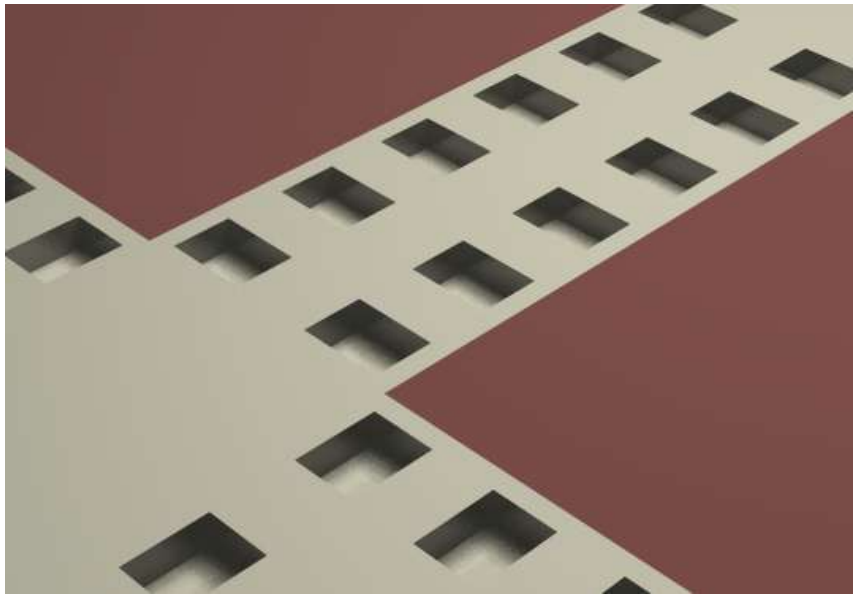
Indiana Integrated Circuits LLC

QP Fabrication Process Flow Overview

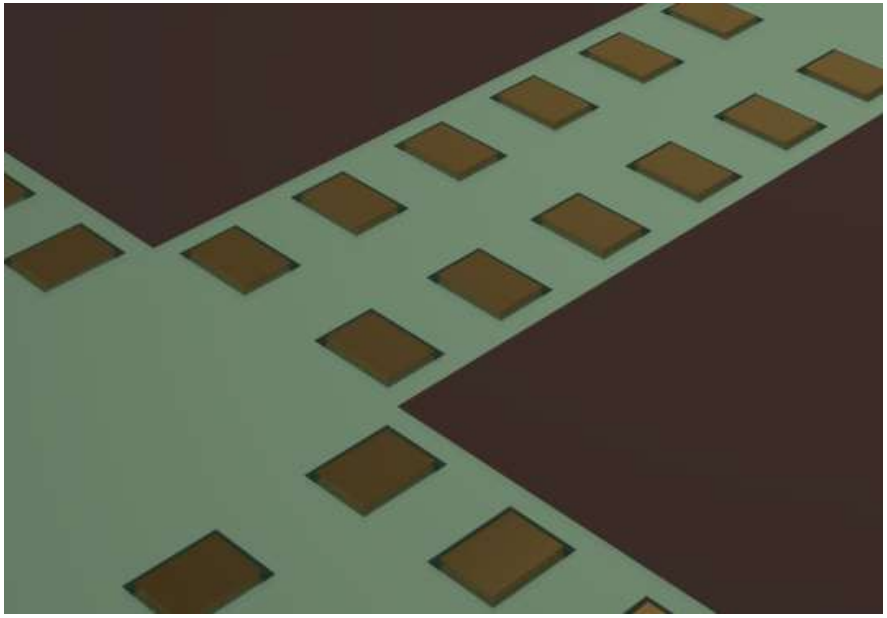
- Very similar to “via-middle” TSV process
- Utilizes industry-standard tools & processes
- At least 2 additional mask steps
  - Nodule definition
  - Separation
- Most unique feature is dry etch step for singulation
- After assembly, handle as if “normal” chip

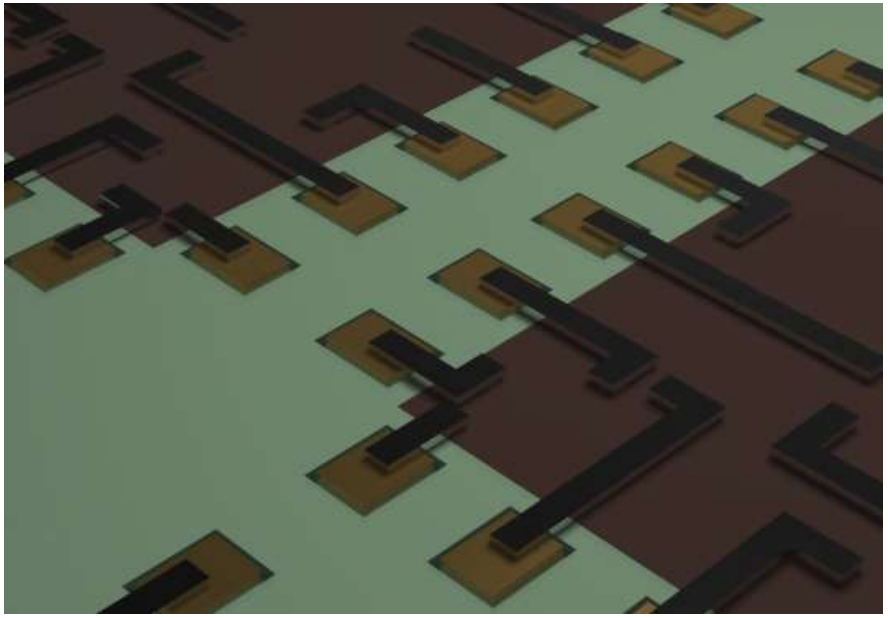
QP Fabrication-Nodule Definition





QP Fabrication- Nodule Metallization





QP Fabrication-Die Singulation