Novel Technique for Flip Chip Packaging of High power Si, SiC and GaN Devices

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Background

- Electronic Products Designers: under pressure to decrease cost and size
- Semiconductor Devices Become Smaller
- Die Generates more Power
- Higher demands for Packaging
- Packaging becomes a more substantial factor in device and system cost
- Especially true for new high switching speed MOSFETs and eGaN FET Devices

Background (cont.)

- New devices provide new capabilities
  - Low conduction losses
  - High Frequency Operation

- Innovative Packaging Required to Realize devices' advantages
  - Device Terminal structure dictates "Lateral vs. Vertical" Packaging
  - Lateral: leadless chip scale packages
  - Vertical: flipped chip where the inter-digitation of source and drain minimizes dc resistance and parasitic inductance
  - Chip Scale Packaging:
    Hermetic packages/interposers

Packaging Goal: What is Needed?

- **Scope: To design Cost Effective, High Performance Package for high speed switching Devices**
- **Highly conductive, low inductance Connections**
- **Efficient Thermal Management**
- **Small Size Chip Scale Package**
- **Non hermetic and Hermetic Options**

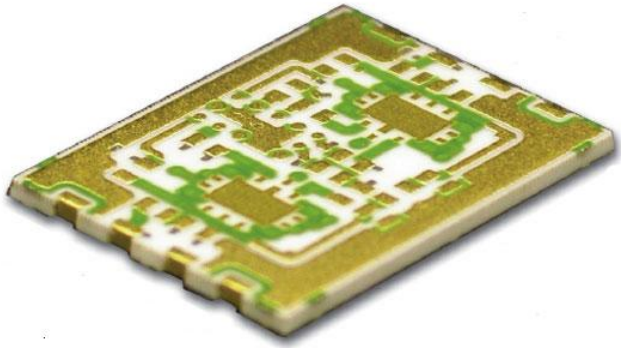
PCTF® Technology

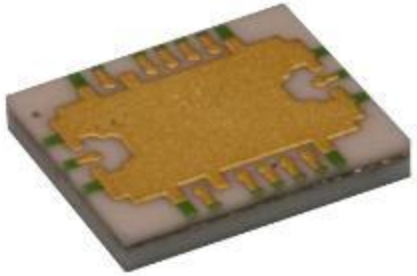
Packaging Solution based on Remtec's PCTF®

Technology: *Plated Copper on Thick Films*

PCTF® Technology

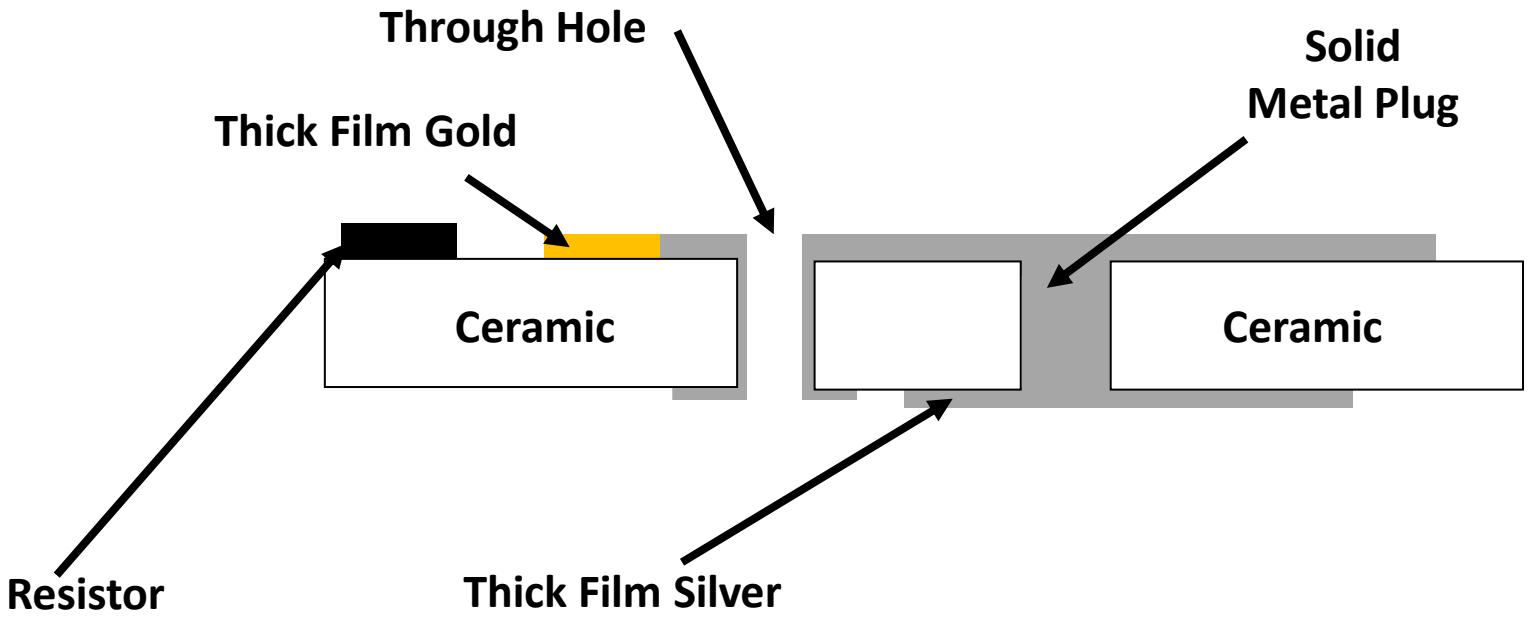
- Plated Copper over Thick Film Silver: .001” -.005” thick
- Cu Plated through-holes, Plugged Vias (hermetic), Wraparounds
- Precision Resistors: mΩ to MΩ
- Ni-Au, Pd, Sn, Ag finish
- Mixing Plated & Unplated Thick Films on the Same Ceramic





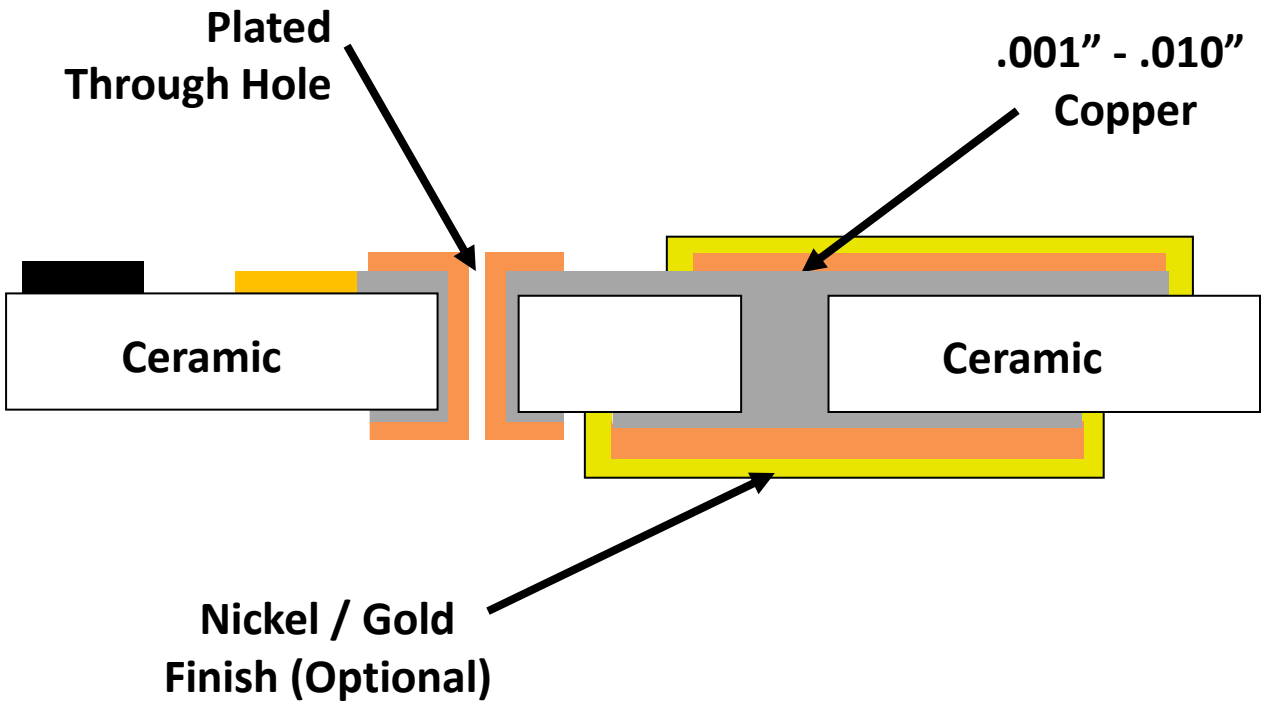
PCTF® Technology Features

Typical Metalized Ceramic Substrate
(Phase One: Thick Films)



PCTF® Technology Features

Typical Metalized Ceramic Substrate
(Phase Two: Copper Plating & Finish)

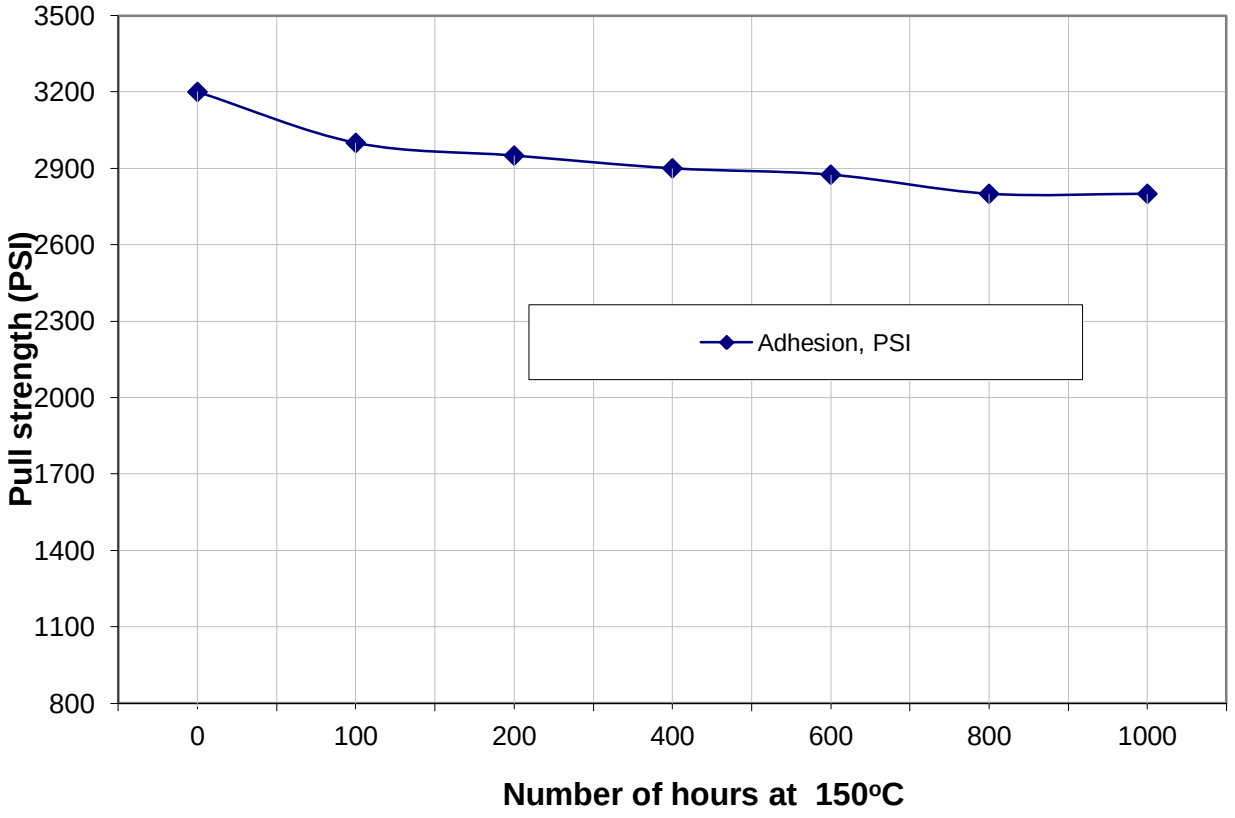


PCTF Adhesion

Adhesion Mechanism

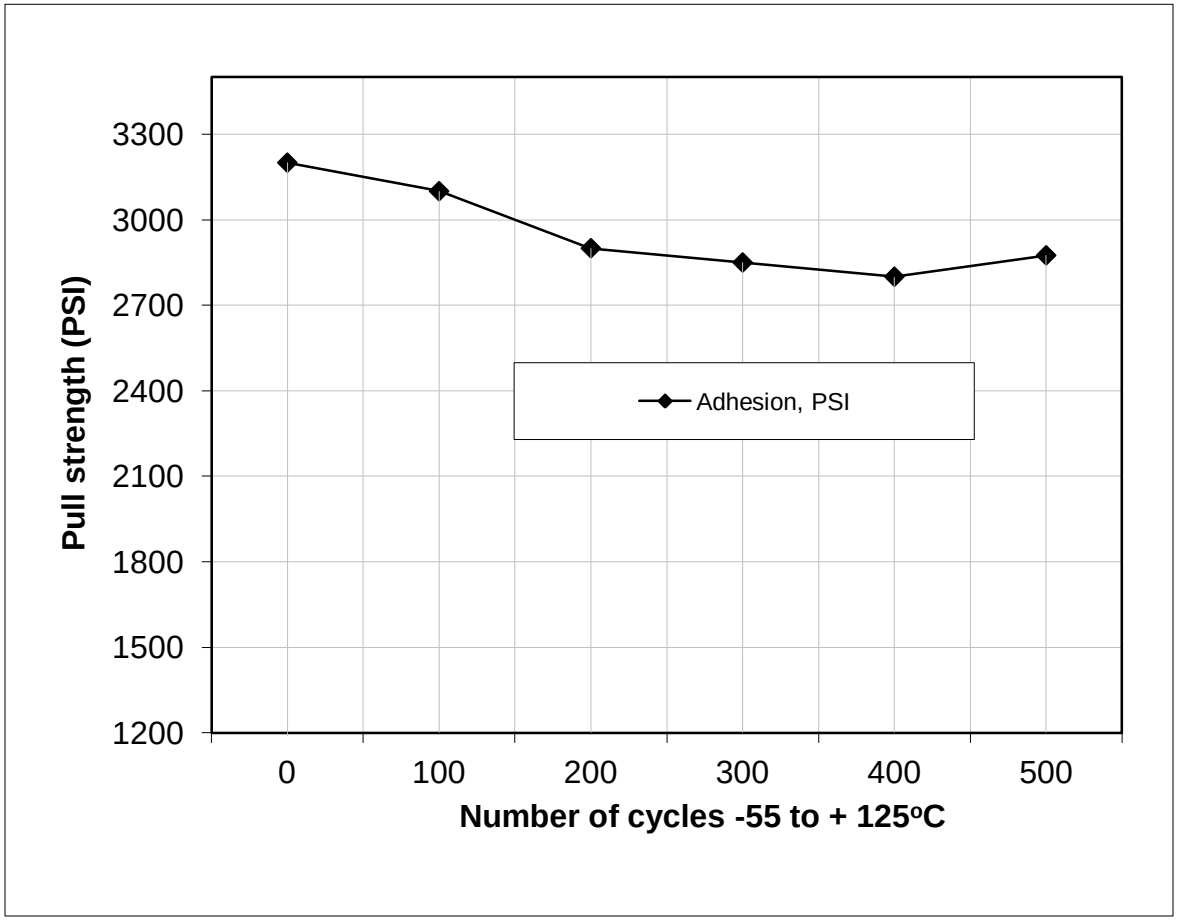
- Thick Film Silver to Alumina Ceramic: Oxide bonded
- Plated Copper to Thick Film: Inter-diffusion

PCTF Adhesion Test Data after Aging



Hours at 150 C	**Adhesion, PSI**
0	3200
100	3000
200	2950
400	2900
600	2875
800	2800
1000	2800

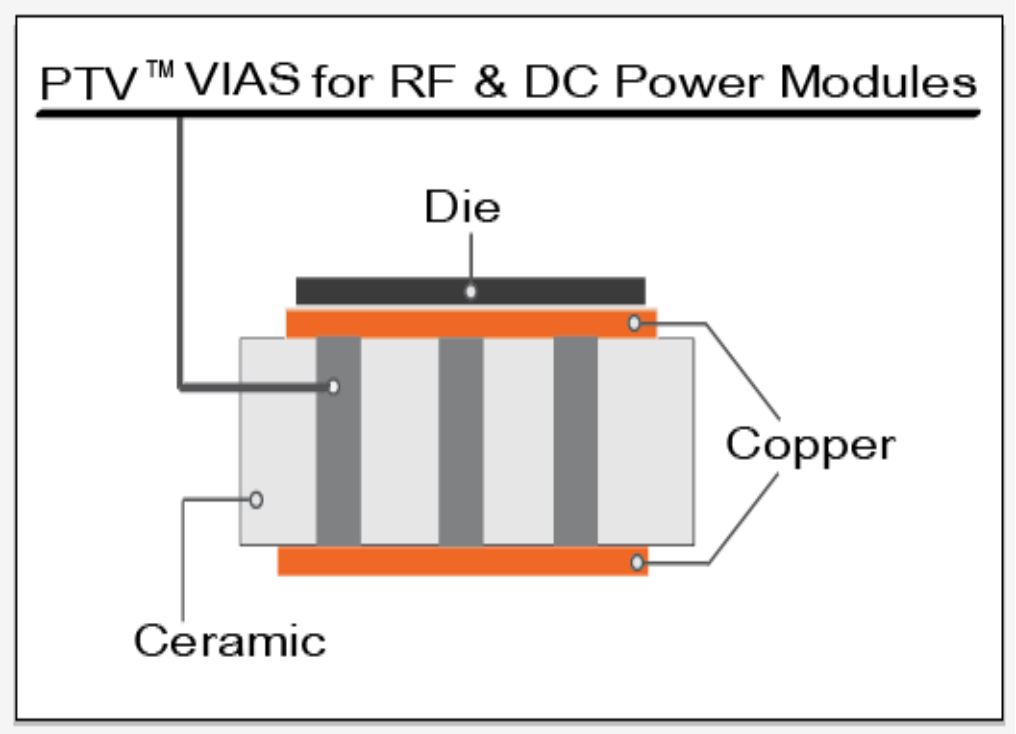
PCTF Adhesion Test Data after Temperature Cycling



Thermal cycles, -55 to + 125 C	Adhesion, PSI
0	3200
100	3100
200	2900
300	2850
400	2800
500	2875

Package Concept: SMT Ceramic Packages with PCTF®

- **Material: Alumina Ceramic – thermally conductive and mechanically rigid**
- **Metallization Material: Copper with Low DC Resistance and Solid Metal Plugged Thermal Vias**

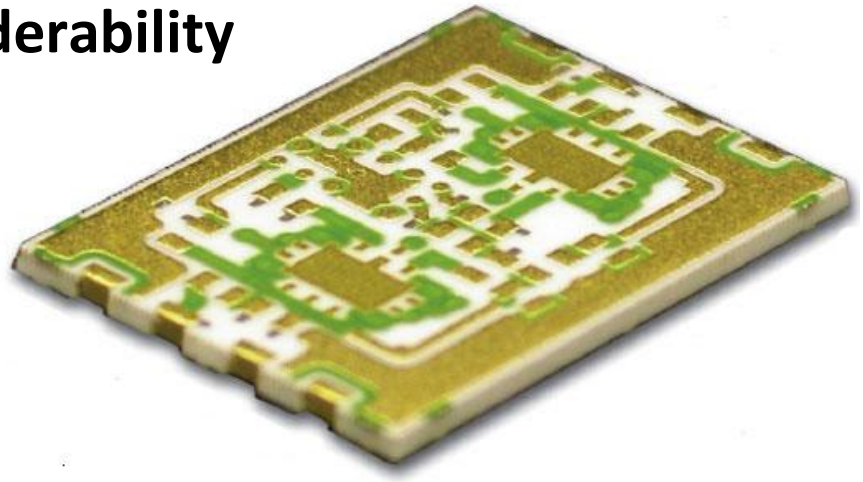


SMT Ceramic Packages with PCTF®: Features

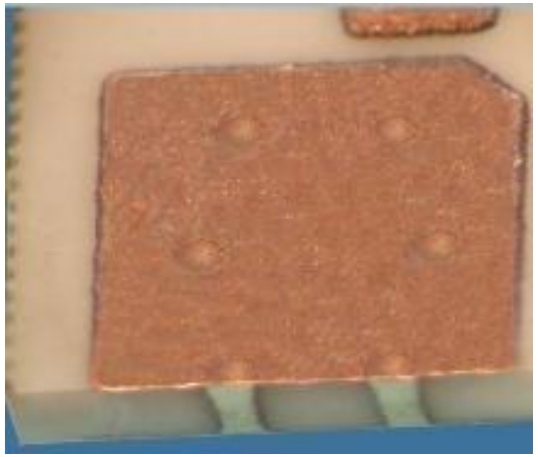
A PCTF® SMT package includes major features:

1. <u>Copper metallization</u>

- Low DC Resistance
- Excellent Heat Spreading Circuit
- Pattern with excellent solderability



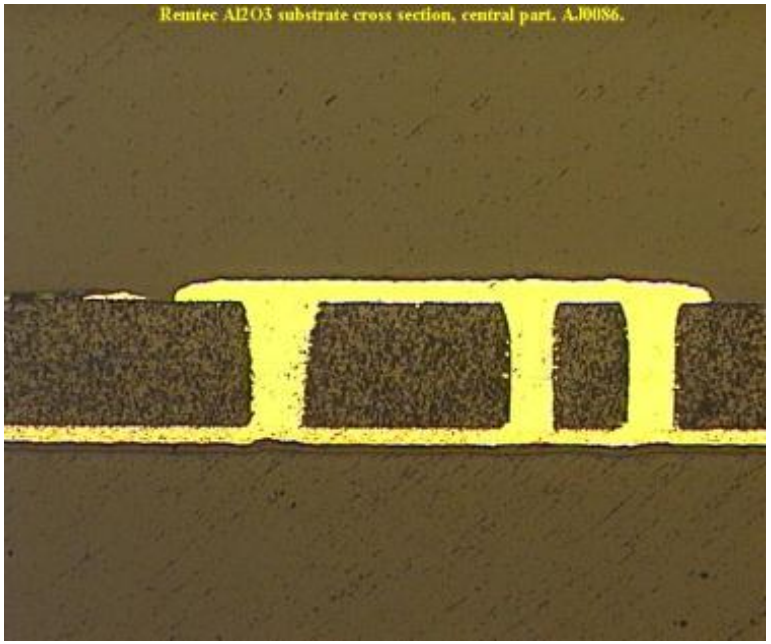
SMT Ceramic Packages with PCTF®: Features



2. Power Transfer Vias – PTV™

- **Copper Plated Solid Plugged Via holes**
- **Thermal Vias with k ≥ 200 W/(MxºC)**
- **Hermetic Filled Vias (10^{-8} atm cc/s)**
- **Electrical Connections with low dc resistance ≤ 1mΩ**
- **Low inductance and capacitance interconnects**
- **Unique Via Material Constructions**

PCTF®: PTV™ Via DC Resistance



Ceramic thickness	Plugged Via Size	Resistance (mΩ)
.010”	.005”	0.50
.015”	.008”	0.42
.020”	.010”	0.38
.025”	.010”	0.47

- Array of 4 vias
- Total Resistance: .1mΩ (10^{-4}Ω)
- @10 amp I^2R losses ~10mW

PTV™- Power Transfer Vias Reliability

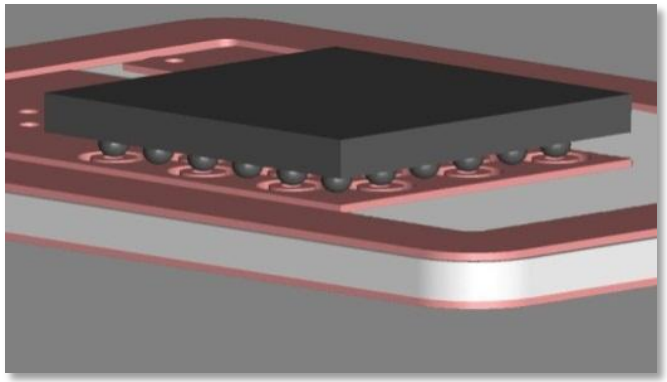
- **Unique Via Construction Ensures High Reliability**
- **Withstands 1,000 T-cycles (-55°C to +150°C) without features degradation and integrity loss**

New Approach for Packaging of High Speed Switching Flip Chipped Devices

Interposers & Hermetic Packages for SiC and GaN FETs

Interposers and Hermetic Packages for SiC and GaN FETs

- Copper Plated PCTF® Metallization with PTV™ Vias
- Near Chip Scale Packaging: Actual package is slightly larger than die
- Die with Flip Chip Interconnects
- .002” Copper Provides for heat spreading and lateral current flow



- Vias Provide Package Interconnects with low DC resistance below 1 mΩ and low lead inductance/capacitance

Why Ceramic for Si, SiC and GaN Interposers

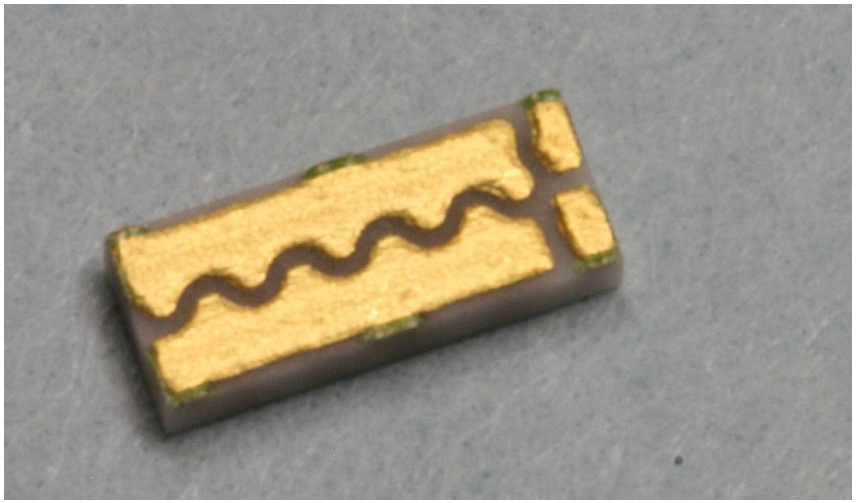
- **Thermally conductive and mechanically rigid**
- **An interface material to compensate for TCE mismatch between semiconductor and PCB**

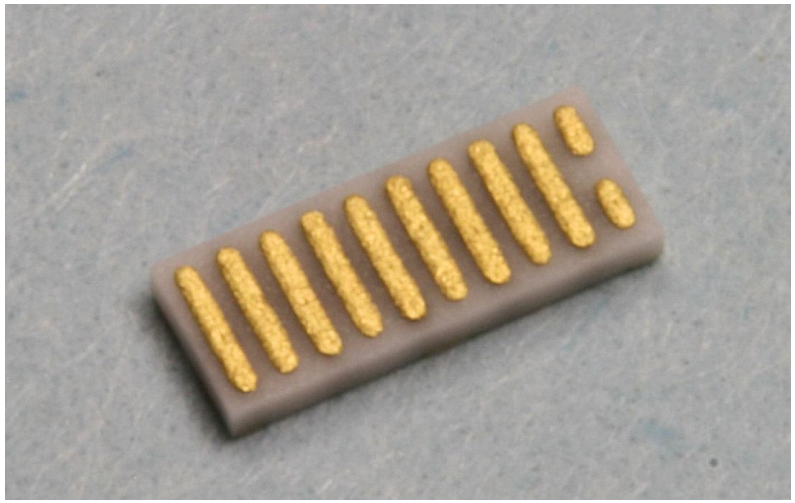
Thermal Properties of Materials

Material	Alumina (Al_2O_3)	PCTF Cu (.002") - Al_2O_3 (.025")	FR-4	Si	SiC	GaN
CTE, ppm/°C	6.6	8.4	15.8	2.6	3.7	6.0
Thermal Conductivity, W/mx°C	25	32	.2	150	270	230

Interposers

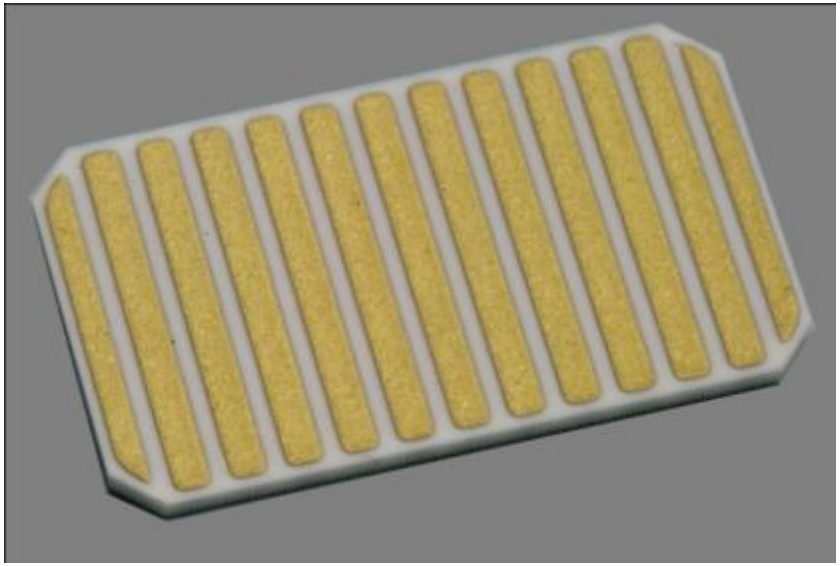
- Interposers Family for GaN MOSFETs
- .002-.003” Copper, Ni-Au Finish
- Flip Chip Die: Connected through Plugged Vias
- Size: .500” x .200” x .050”

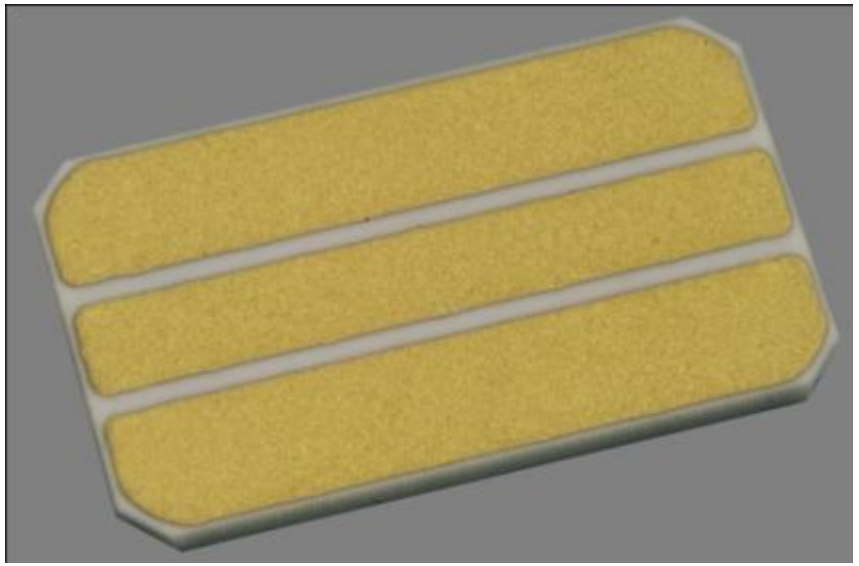




Interposers

- Interposers Family for Si and SiC IC's to 25 AMP
- .002-.003" Copper, Ni-Au Finish
- Flip Chip Die: Connected through Plugged Vias
- Size: .980" x .680" x .050"

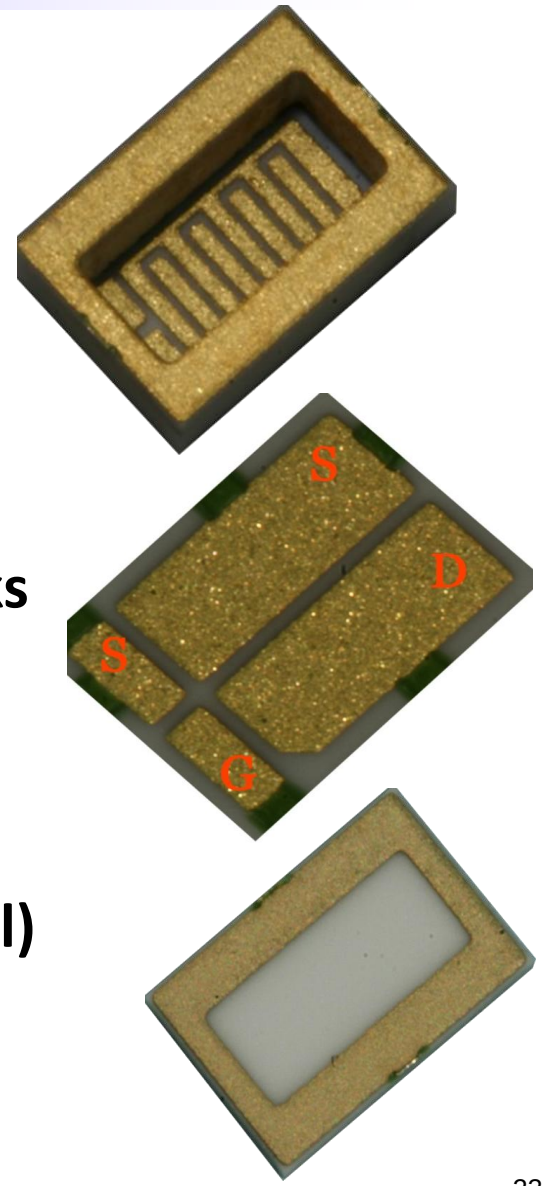




Hermetic Interposer for GaN FET Transistor

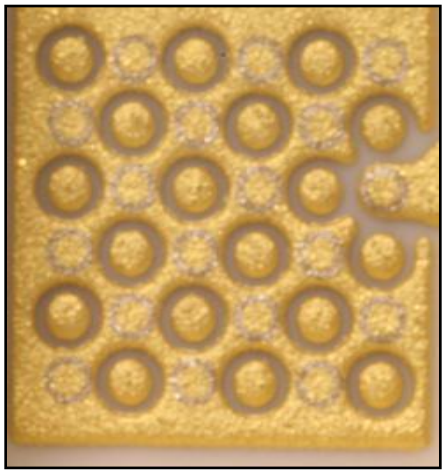
eGaNFET

- New GaN device with High Speed Switching to replace STD MOSFET
- BGA Construction Requires Low DC Resistance/Inductance and Hermetic Connections (Vias)
- Alumina Ceramic with .002” Cu Plated Tracks and Plugged Vias
- Size: .220” x .150” x .050”
- Ceramic Frame Attached with Plated AuSn solder (top metallized for final hermetic seal)
- Flat ceramic Lid with Plated Gold Tin



Leadless Hermetic Package for GaAs MOSFET

High DC Current and High Power Package



- **.002” Copper for heat spreading and lateral current flow (25 AMP)**
- **Size: .400” x .300” x .110”**
- **Vias with Low DC resistance below 1 mΩ and low lead inductance/capacitance**

REMTEC® Ceramic Packaging Solutions for Optimum Performance

New Packages Reliability Testing

Testing was Performed in accordance with MIL-PRF-38534H

Test Conditions per MIL-STD-883

Test	Method	Condition	Notes
Solderability	2003	At 245°C	
Thermal Shock	1011	C	15 C, -65 to +150°C
Mechanical Shock	2002	B, Y1 direction	
Constant Acceleration	2001	3,000 g's Y1 direction	
Hermetic Seal	1014	A4 (open package)	For hermetic packages only
Salt Atmosphere	1009	A	

Conclusions

- **Innovative Packaging Approach Has Been Developed Fully Realizing Capabilities of New High Switching Speed Flip Chip MOSFETs**
  - **Low Conductance Losses**
  - **High Frequency Capability**
- **Developed Leadless Ceramic SMT, Chip-Scale Packages Utilizing GaAs, GaN and SiC Flip Chip Devices**
  - **The Inter-digitation of Source and Drain Minimizes dc Resistance and Parasitic inductance**

Conclusions

- A Variety of Various Cost Effective, High Performance Packages Has Been Developed, Fabricated and Tested
- Small Size Chip Scale Package
- Highly conductive, low inductance Interconnects
- Efficient Thermal Management
- Interposers and Hermetic Packages
- Reliability Testing per MIL-STD-883 Completed

Thank you for your attention!