Manufacture of Nanostructures for Power Electronics Applications

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Outline

• Background
  – Brief intro to carbon nanotubes (CNT)
  – Review of previous work

• Etamota CNT FET (“CTFET”)
  – Motivation
  – Technical challenges
  – Results with vertical and horizontal device geometries

• Research team: Brian Hunt, Eric W. Wong, Chao Li, Rajay Kumar, Mercedes Gomez, Brian Lingg, Mike Bronikowski, Sunghwan Jung, Jim Hartman
Etamota Background

**Tools Business Unit**
- Manufacture and sale of chemical vapor deposition (CVD) systems for production of nanostructures, e.g., CNTs

**Semiconductor Business Unit**
- Commercialize nanostructure-enabled power semiconductor applications:
  - Power FETs
  - Heat spreaders

**WW Semiconductor Market ~$287B**

- Logic 25%
- Analog 17%
- MicroP 23%
- Memory 23%
- Opto 6%
- Discrete 6%
Carbon Nanotube Properties

**Electrical**
- More conductive than copper
- Semiconducting or metallic
- Current density up to $10^9$ A/cm$^2$
- Ballistic transport, mean free path ~1µm
- Radiation tolerant
- Silicon compatible

**Mechanical**
- Strongest known material
- 200 times higher strength/weight than steel

**Thermal**
- Thermal conductivity comparable to diamond
- ~10 times more conductive than copper

**Surface**
- Ideal non-reactive surface (high-k dielectric compatible)

*Carbon nanotubes offer a unique combination of properties that make them ideal for power applications.*
Nanotube structure determines electronic properties

- Typical CNT growth process produces $\approx 2/3$ semiconducting tubes
- Metallic tubes must be removed for semiconductor device applications

(Avouris, IBM)
Burnout of metallic nanotubes

**Burnout process:**

- Originally developed by IBM Research
- *Gate voltage used to “turn off” all semiconducting nanotubes*
- Large S-D voltage drives current through metallic tubes
- Heating in oxygen environment selectively burns metallic tubes
- Voltage increased until most metallic tubes are destroyed
Why make CNT FETs?

**WW Semiconductors**
($287B, 2007$)

- Logic: 25%
- Analog: 17%
- Memory: 23%
- MicroP: 23%
- Discrete: 6%
- Opto: 6%

**Discrete Semiconductors**
($18.1B, 2007$)

- LV FET: 23%
- LV Diode: 9%
- HV Diode: 10%
- SS, other: 22%
- RF, uWave: 9%
- HV Trans: 31%

**Over $5B existing market in low-voltage discrete semiconductors**
# Semiconductor Materials Comparison

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<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>SiC</th>
<th>GaN</th>
<th>CNT</th>
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<tbody>
<tr>
<td>Electron Mobility</td>
<td>1,400</td>
<td>8,000</td>
<td>800</td>
<td>900-2,000</td>
<td>10,000</td>
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<td>(cm$^2$/V·s)</td>
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<tr>
<td>Hole Mobility</td>
<td>500</td>
<td>400</td>
<td>50</td>
<td>50</td>
<td>10,000</td>
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<tr>
<td>(cm$^2$/V·s)</td>
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<td></td>
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<tr>
<td>Band gap (eV)</td>
<td>1.12</td>
<td>1.42</td>
<td>3.25</td>
<td>3.4</td>
<td>0.5-1.0</td>
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<tr>
<td>Thermal Conductivity</td>
<td>150</td>
<td>50</td>
<td>490</td>
<td>130</td>
<td>3,000-6,000</td>
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<tr>
<td>(W/m·K)</td>
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</tbody>
</table>

**CNT Semiconductor Device impact:**

- Greater efficiency ➔ lower loss to heat
- Greater power density ➔ smaller die for same power
Excellent Single-tube CNT FET Performance

- On state current: 3000 µA/µm (Si ~ 200-650)
- R.T. Carrier mobility (p): 10,000-100,000 cm²/V·s (Si ~ 450, AlGaN ~ 2,100)
- Transconductance: 8900 mS/mm, Fuhrer et al., 2004 (SiGe ~ 300)
- Subthreshold swing: ~70 mV/dec (~65 lower limit, room T)
- Ballistic transport shown - mean free path ~ 1µm (E<200mV)
- **20 GHz operation** (Luoam et al., CNRS, APL 6/07)

![Original nanotube device](Tans et al. 1998)

Power devices require many nanotubes in parallel

![Diagram of CNT FET with ALD gate oxide](Gate HfO₂ SiO₂ p++ Si CNT FET with ALD gate oxide H. Dai group at Stanford Javey et al. Nano Letters, 2005)
**CNT power devices: key challenges**

**High on-off ratio** essential to reduce off-state dissipation
- For in situ growth metallic nanotubes must be selectively removed or grow all semiconducting tubes
- Or, nanotubes must be purified before dispersal

**Small $R_{on}$** to reduce off-state dissipation
- High nanotube density required:
  - Low $R_{on}$ per unit area
  - High power density
    - Need many nanotubes in parallel (metallic tubes are an issue)
- CNT-electrode contact resistance must be minimized
  - Essential for low $R_{on}$
  - Pd contacts
  - CNT diameter control
    - minimize Schottky barriers
  - Doping
Power devices with arrays of CNTs

- Infineon work: horizontal CNT array power FET
  - Disordered CNT arrays
  - IBM burnoff technique
  - Currents ~mA with on-off ratio of ~500

- John Roger’s group, Univ. of IL
  - Highly aligned SWNT growth on ST-cut quartz
  - IBM burnoff technique to destroy metallic tubes
  - On-off ratios up to ~$10^4$
  - Currents up to ~1 A
  - See also C. Zhou group: Wang et al. APL 93, 33101 (2008)

Early Etamota CNT FET Platform - Nanotubes in Porous Aluminum Oxide

- Dense **vertical array** of nanotubes provides maximum potential power density
- However, self-supporting vertical SWNT not possible (unless dense-packed)
- **Porous aluminum oxide** (PAO): inexpensive anodized aluminum technology provides dense insulating pore array
- PAO provides mechanical support to enable vertical SWNT and integrated electrodes
- Etamota developed *unique high-yield growth process for SWNT in PAO* (high temp CH$_4$– C$_2$H$_4$)
- Functional vertical CNT FETs
- Manufacturability was an issue...
Si-Based Device Structure: “EVFET”

Edge-Contacted Vertical FET

- Vertical trench geometry
- Builds on standard semiconductor fabrication materials and processes
- *Si-compatible structure will enable logic integration*
- Low-cost starting material commercially available
- *Si compatible structure enables leveraging of semiconductor manufacturing base*
EVFET CNT devices
**CNT EVFET - Data**

- Excellent device uniformity, reproducibility, and scaling
- High yield, very good gate isolation
- Working to improve contact resistance and on-off ratio.

On-off ratio $\sim 10^3$

- Full wafer processing
- Large area devices
Vertical vs Horizontal Geometry

- Source, drain, gate interdigitated electrodes have width minimum set by series resistance constraint.

- *Vertical device structure will give ultimate performance, but horizontal geometry is competitive and more manufacturable.*
Horizontal CNT growth on SiO$_2$/Si and Quartz substrates

- For CNT growth on SiO$_2$, get nonaligned tubes and large variation in lengths,

- The higher voltages required to burn out the longest tubes destroy too many of the semiconducting tubes.

- Aligned CNTs on quartz avoid this issue and give us higher tube densities.
Transferring Aligned Nanotubes from Quartz to Oxide/Silicon

SEM of Aligned NTs on Quartz

SEM of Aligned NTs transferred to Silicon

Reliable, high-yield process
CNT FET Performance

- Horizontal device architecture gives best performance
- Reproducible, high yield CNT process
- Best performance to date $R_{on} A \approx 2 \ \Omega \cdot \text{mm}^2$ with on-off ratio $\approx 10^5$ (same device)
- Scaling to larger devices
- Improvements in burnout process

\[
\begin{align*}
I_d & \text{ vs } V_d \\
I_d & \text{ vs } V_G
\end{align*}
\]
Key Points

- New platform for electronics based on CNT
  - 5x to 10x improvement in key figures of merit
  - Functional devices in hand

- Target market: $5B low voltage components
  - Devices used in almost all electronics

- We have produced high performance CNT FETs in both vertical and horizontal geometries

- Other CNT-based power devices are under development
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