Integrated Inductors in PwrSoC (Today and Tomorrow)

APEC 2010
SP1.4 Power Supply on Chip - PwrSoC

Feb 25th, 2010
Today Ready for Commercialization

- Magnetic Material on Silicon
  - CMOS compatible fabrication process
  - 20 MHz and higher operation
- DC-DC Device With Integrated Inductor
  - Assembly using existing MCM manufacturing process
  - Standard JEDEC qualification & reliability tests
- Targets
  - $V_{IN} < 5V$, $0.8V < V_{OUT} < 3.3V$, $1A < I_{OUT} < 2A$
  - Low profile, small footprint, low cost

Tomorrow In Development

- Continue to Increase Level of Integration
- Magnetic Material and Conductors on Silicon
- Migrate Multiple Die to Monolithic Single Die
Agenda

♦ Market Opportunities For PwrSoC

♦ Dual Chip Approach to Magnetic Integration

♦ Low Cost Approach to Magnetics on Silicon

♦ Technical Improvements

♦ Summary
Power Electronics Market Evolution

Energy Utilization
• Reduction of OpEx
• Global Green Initiatives
• Extension of battery life

New Services and Applications
• Driving additional functions
• Adding more power rails
• Shrinking board size and profile

Higher Capacities
• Data rates increasing
• Growing data storage capacity
• Increased speed, higher noise sensitivity

Industry wide system demands are challenging power designs to deliver

Higher Efficiency  Smaller Size  Lower Noise
All at Lower Cost

Linear Regulator  Lower Cost
DC-DC Switcher  Higher Efficiency
Gen1 DC-DC PwrSoC  Smaller Size

Next Generation PwrSoC
With Wafer Level Magnetics
Power SoC’s Address Market Forces

♦ Integration – increased power density

♦ High frequency operation – very low noise

♦ Wafer level magnetics is a PATH to:
  • Low, silicon-like cost structure for magnetic components
  • Cost-effective DC-DC with switcher-like efficiency solution alternative to LDO
  • Ultra-thin profiles, 0.6mm and below
Power SoC Construction: In Volume Manufacture Today
(Side by Side Vs Stacked Assembly Approach)
Technology Enabling Magnetic Material On Silicon
(Wafer Level Magnetics Approach thru Manufacturing Trials and Qualification)
Wafer Level Inductor Construction
(Fabrication Options [Design Trade-Offs])

- **Magnetic/Conductor Structure**
  - Toroid
  - Shell (sandwiched)
  - Planar Coil with Mirror
  - Meander

- **Magnetic Structure**
  - Multi Layer (Laminated)
  - Single Layer

- **Magnetic Anisotropy**
  - Annealed
  - Geometric
  - None
Construction
(X-Ray Image of Stacked Device)

Inductor Die Magnetic Material

Inductor Windings
Construction
(Cross Section of Stacked Assembly)
Magnetics on Silicon
(Initial DC-DC Device Level Application Implementing Wafer Level Magnetics)
Inductor Level Performance

(Small Signal Characteristics)
Inductor Level Performance
(Large Signal Characteristics)

AC Power Loss 25°C  5 - 10 - 20 MHz

\[ PL = K^* (nVsec)^f \]

- 20 MHz
- 10 MHz
- 5 MHz

\( E \Delta T (nVsec) \)

\( 10 \) \( 100 \)

\( 0.0010 \) \( 0.0100 \) \( 0.1000 \) \( 1.0000 \)

AC Loss (Watts)
Inductor Level Performance

(Inductor Power Losses $V_{IN} = 3.3V_{DC}$ $V_{OUT} = 1.8V_{DC}$ $F_{SWITCH} = 20$ MHz)

$P_{INDUCTOR}/P_{OUT}$

$P_{DC} + P_{AC}$

<table>
<thead>
<tr>
<th>0.2A thru 1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
</tr>
<tr>
<td>0.05</td>
</tr>
<tr>
<td>0.10</td>
</tr>
<tr>
<td>0.15</td>
</tr>
<tr>
<td>0.20</td>
</tr>
</tbody>
</table>

Sum of PIND_ACAutoGenerated

Sum of PIND_DC

ENPIRION
DC-DC Converter Level Performance

(Efficiency – Synchronous Buck 20 MHz)
Inductor Level Performance
(External Magnetic Fields: Same Scale)

Planar Coil Without Magnetic Plate

Planar Coil With Magnetic Plate
Device Level Performance
(Output Ripple / Transient Response $V_{IN} = 3.3 \, V_{DC} \, V_{OUT} = 1.8 \, V_{DC} \, I_{LOAD} 0.6A_{DC}$)

Output Ripple
2 mVp-p

Transient Response
65 mV deviation
Device Level Performance
(Output Voltage CM Noise Spectra $V_{IN} = 3.3\ V_{DC}$ $V_{OUT} = 1.8\ V_{DC}$ $I_{LOAD} 0.6A_{DC}$)
Migration to Monolithic Device
(CMOS Compatible Inductor Fabrication)

Historical: Concept designs
Toroid inductor

Today’s Prototypes
Tomorrow’s Products

Today: Ready for Manufacturing

Magnetic Material on Silicon
Conductors & Magnetic Material on Silicon
Summary and Next Steps

- Wafer level magnetics have been prototyped thru the complete manufacturing process
- Finished devices pass qualification and reliability testing
- Achieved targeted inductor and device performance
- Low cost design construction techniques utilized
- Wafer level magnetic materials ready for commercialization
Wrap Up

Thank You For Your Attention