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Nano-Processing for High Voltage and High Power Devices

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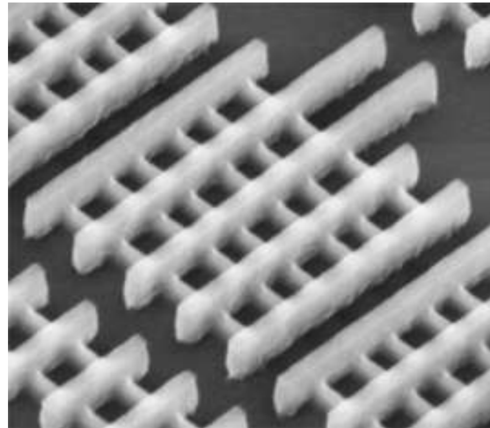
Outline

- Background concepts
- Two “nano” ideas:
  - New high voltage, high power FET device designs
  - Application of “nano-particles” to device assembly processes
- “Front end”- high voltage device configurations
  - Physics of high voltage and high power device fabrication concepts
  - Look at advanced device structures with “nano-scale” dimensions
- “Back end”- Materials for die assembly
  - Optimize the electrical conductivity, remove the waste energy (heat)
  - Maintain “low” process temperatures
  - Create high strength bond lines
  - A new approach to die attachment for high performance packaging
- Summary

High Voltage Devices

Nano-materials and Device Structures

- In the context of “nano”- new devices have critical dimensions in the range of nanometers.
  - Intel – “22nm” FINFET device dimensions- about 50 atomic layers!
  - Suitable structures for low power and low voltages
  - Key point- the electric fields for higher voltage operation will readily exceed the material dielectric limits



Source: Intel, CNET article, May 4, 2011

- For high voltages and high powers, we need to consider:
  - Semiconductor materials properties
  - Physics of the dielectrics
  - Electric fields
  - Device layout and construction
  - Thermal and electrical conductivities

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Nano-materials and Device Structures- 2

- Device dimensions must scale according to the physical constraints:
  - Applies to all materials and structures in the device
  - In silicon, the critical electric field is ~10V-12V per micrometer
    - A ‘high voltage’ device will have dimensions in the range of 25um to 100^{+}um
  - Capacitance effects
    - Speed limitations are proportional to the device size/gate width in FETs, C_{g-s}, C_{g-d}, charge distributions, and C_{b-e}, C_{b-c} in bipolar devices

- “Lateral” device (in the plane of the wafer):
  - The device dimensions are determined by the materials properties
  - Substantial lengths are required to support the impressed electric fields.

- A “trench-type” device distributes the electric fields vertically:
  - Relatively compact devices within the constraints of electric fields, fabrication capabilities, and power density/dissipation.

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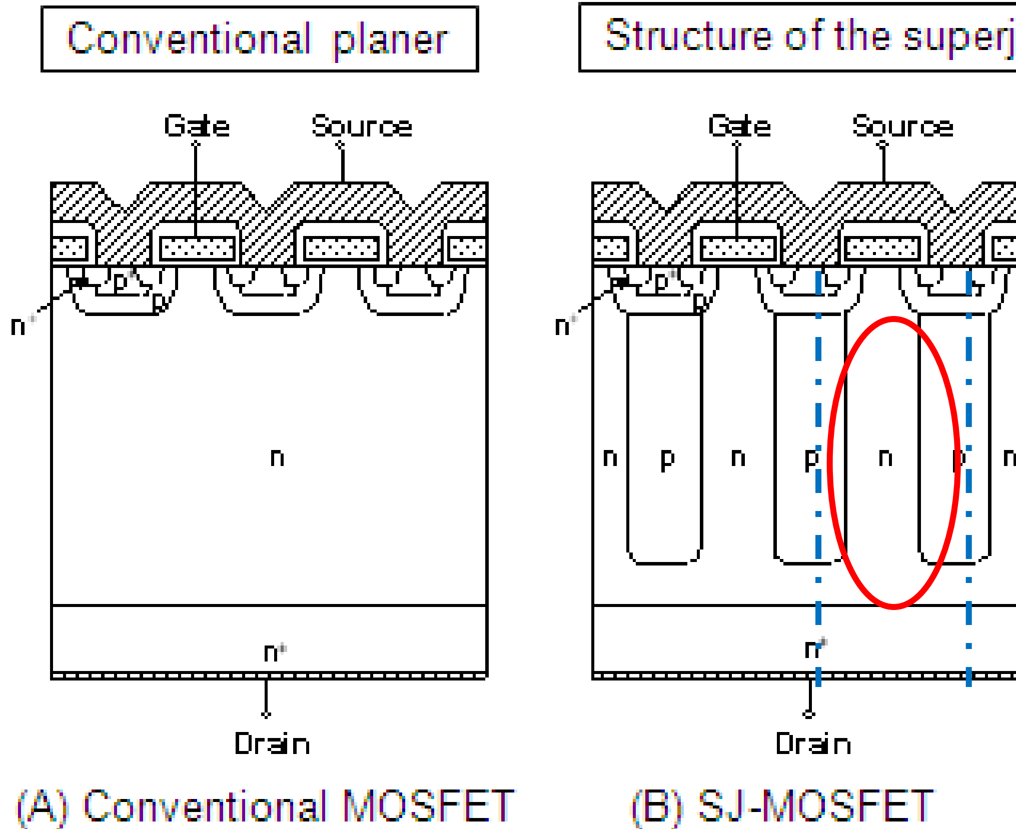
HV Device Topologies

- Vertical “super-junction” structures for high voltage applications:
  - Careful control of the “charge balance” in P-N junctions permits sustaining electric fields that can approach the dielectric limits of the materials
  - Vertical structures optimize the device dimensions and reduce device cost (silicon area)
- Infineon, Fairchild, Fuji Electric, HHNEC, DENSO, Toshiba, and many others have produced this class of devices over the past ~5-7 years using various technologies
- Trench-filled epitaxy approaches- concern for “Lack of charge imbalance margin, Lowering saturated current, Large output capacitance”- DENSO, J. Sakakibara, ISPSD-2008
  - These limitations and issues have been overcome in recent years
- Multiple epitaxy-implant-anneal cycles- relatively heavy loading of tool sets, and somewhat higher fabrication cost. However, billions of these devices have been manufactured (Infineon, 2012)
- Take advantage of “nano” materials physics and advanced processing methods, and epitaxial growth capabilities, to create a new concept

Superjunction Devices

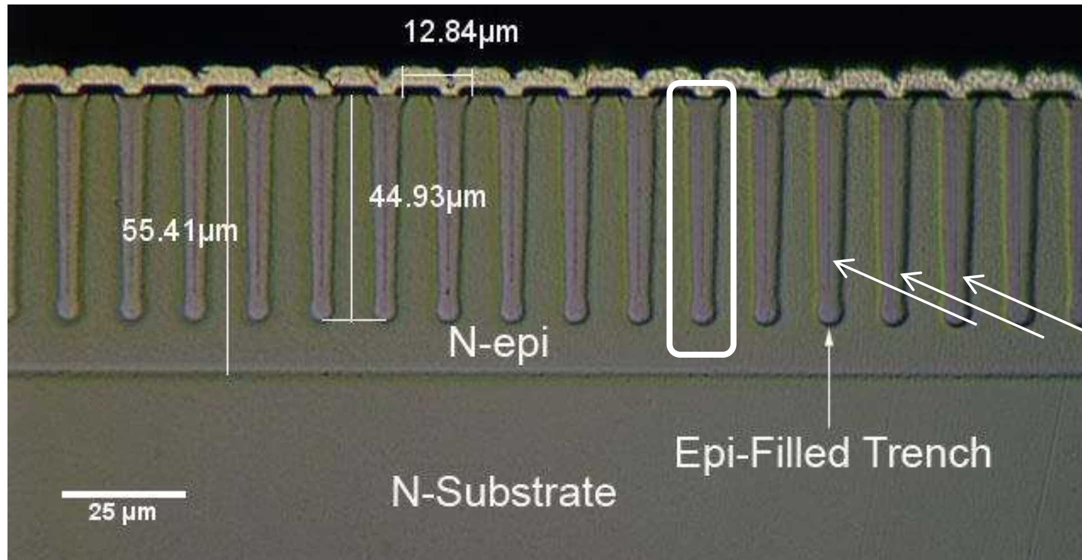


The n-type and p-type charges must be "balanced" for the device to operate correctly.

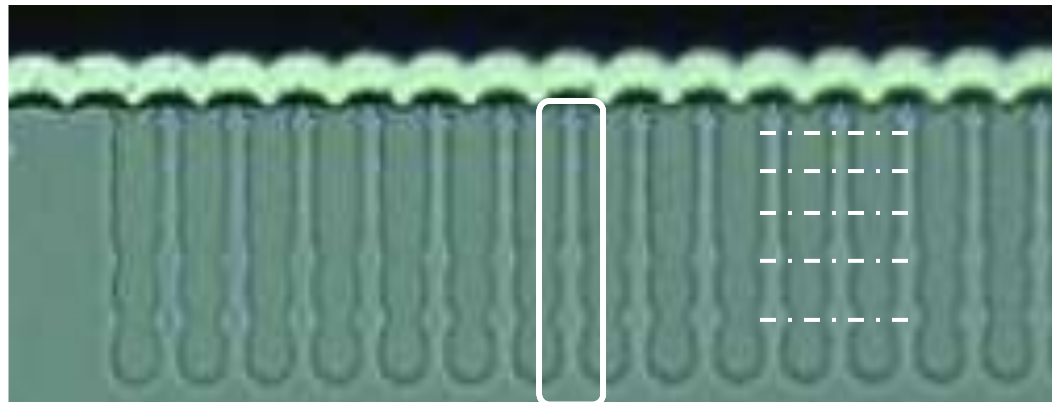
Fuji Electric Co. super junction MOSFET, Mar 28th, 2012 article in *I*-Micronews. "70% reduction in on-resistance, thereby achieving industry-leading performance in low power loss, compared to previous Fuji Electric products. The latest switching loss reduction technology, enabling a 14% reduction in total loss from the device, compared with previous Fuji Electric products."

I-Micronews
FROM CONCEPT TO DEVICES

Commercial Filled-trench HV-FET Devices



One approach employs an epitaxial filled-tapered-trench approach to form the vertical "superjunction" charge-balanced structure. The trench walls are tapered significantly to permit filling of the trenches with the p-type epitaxy. There is a seam in the center of the trenches that forms as the top region closes and seals during the final stages of growth.



A different approach uses a multiple implantation-lightly doped epitaxy-anneal cycle (the 5 cusps in the image) to create the vertical "superjunction" charge-balanced structure. The structure has a "taper" from outdiffusion and photomasking effects. The objective is to provide overall charge balance in the vertical direction. The dashed lines indicate the approximate steps in the formation of the epitaxial materials.

In all cases, the integral of the charge distribution in the vertical direction is ~0, that is, "balanced".

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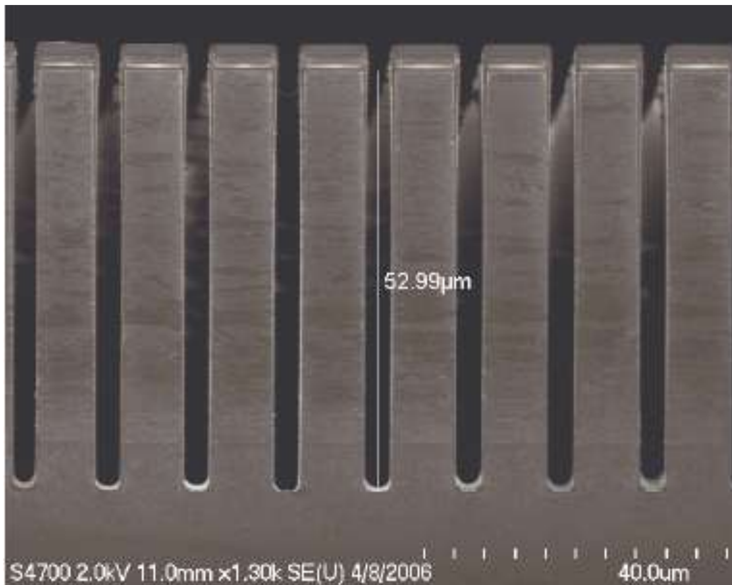
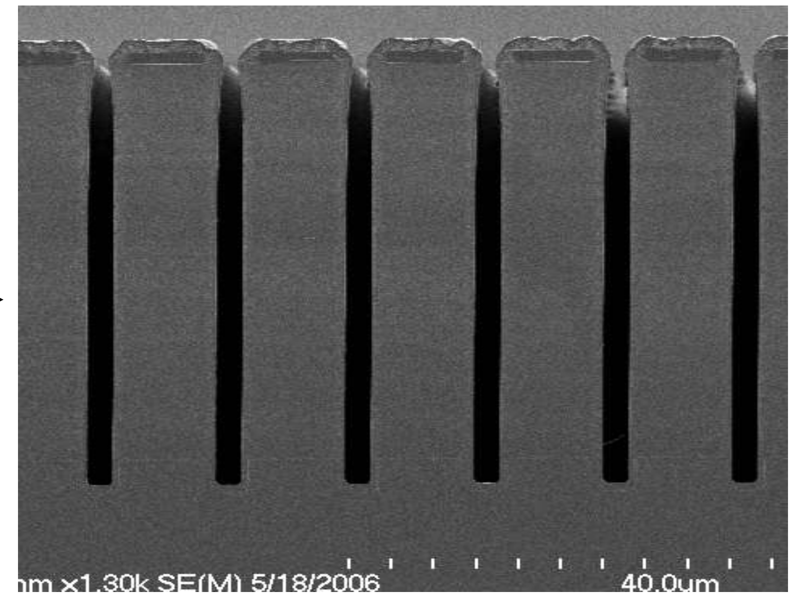
ON Semiconductor HVFET Devices



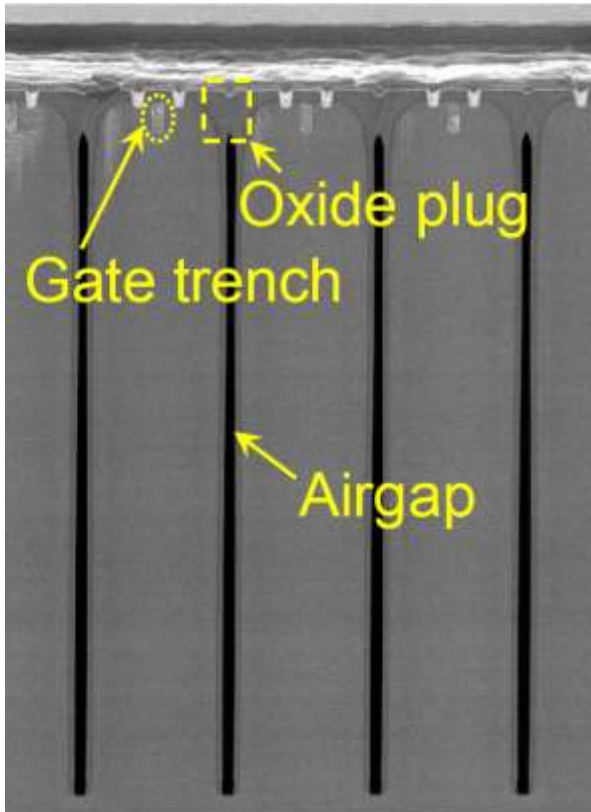
Trench-etched wafer

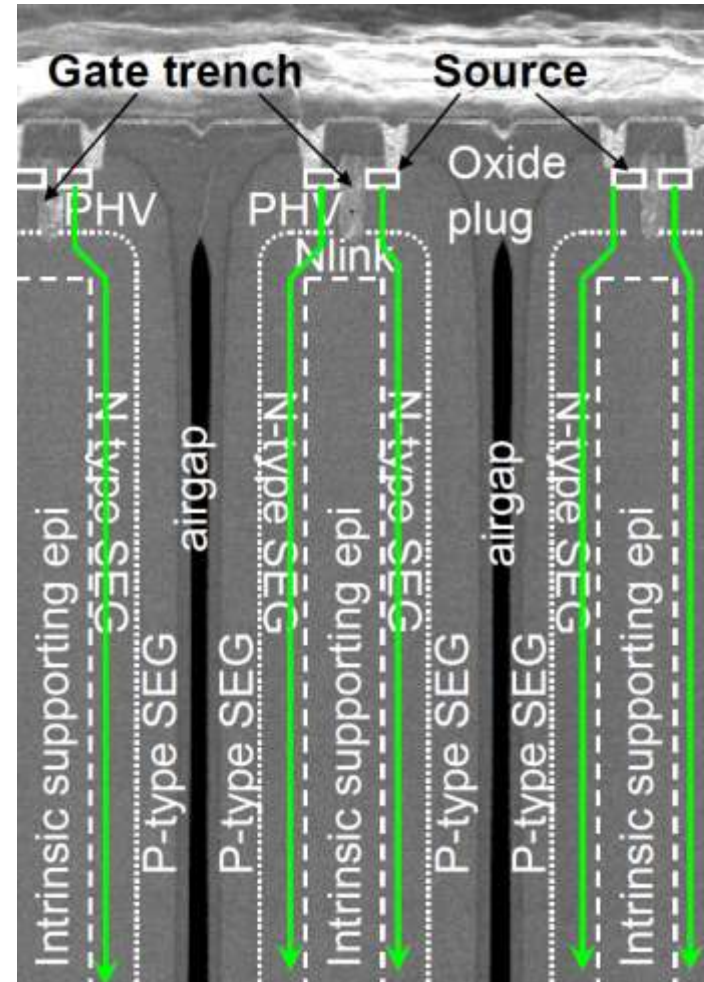


Epitaxy-filled wafer

- In this “nano” construction, deep trenches of ~50-60um depth, and aspect ratios of ~20:1 are etched into the silicon substrate
- Various layers of silicon with appropriate doping are deposited selectively *only* onto the walls of the trenches
- These layers are on the order of only ~200-600 atoms in thickness, but serve to create the charge-balanced structure necessary for device operation
- The epitaxy process also adds two degrees of freedom to tune the charge balance

ON Semiconductor HVFET Device





- "Striped" trench structures-
  - The epitaxial growth process was tailored to "perfectly" fill the trench with single crystal epitaxial layers in the range of ~100nm-400nm thicknesses
  - Charge is balanced to better than 5%
  - The narrow pitch provides a high power density, small device size and low Rdson values
  - The structure is easily scaled for lower or higher voltage applications

From ISPSD 2011, "Best Paper Award", P. Moens et al, ON Semiconductor.

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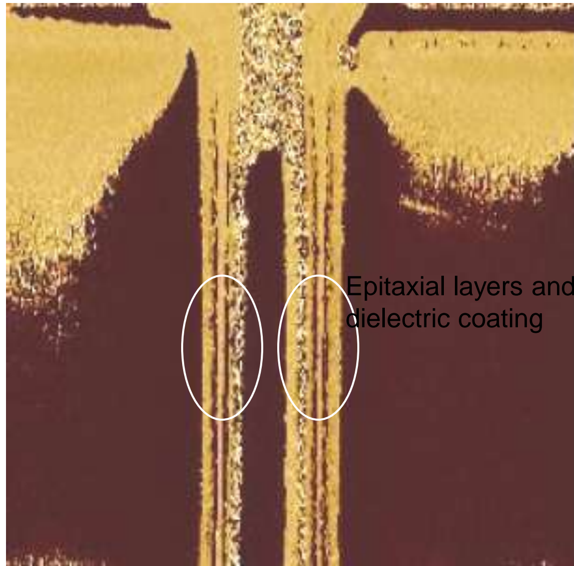
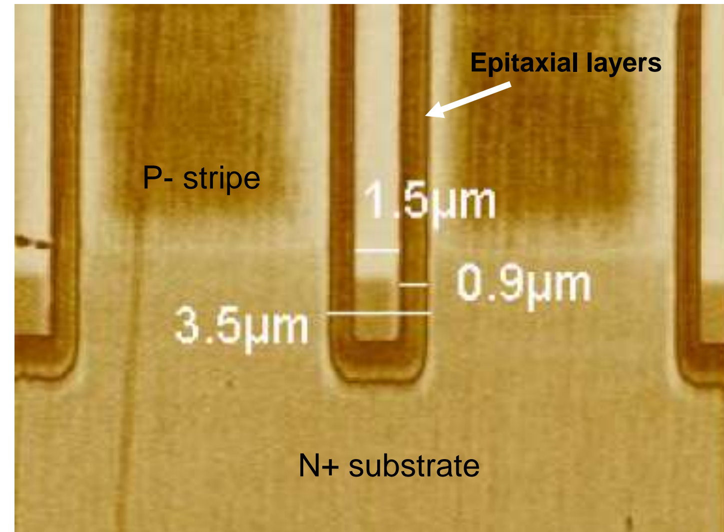
Did We Really Do What We Said?

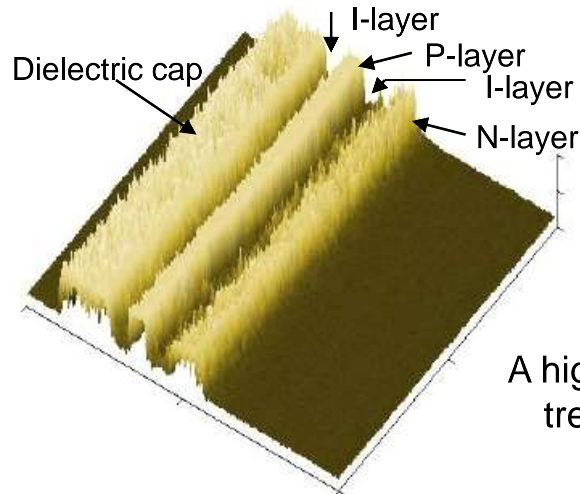
Scanning capacitance (SCM) images of the trench and layer structure



The top region of the trench structure; the various layers are clearly visible



Bottom of the trench showing the layer structure continuity, and the N+/P- junction.



A high resolution SCM image in the middle region of the trench shows the charge separation detail.

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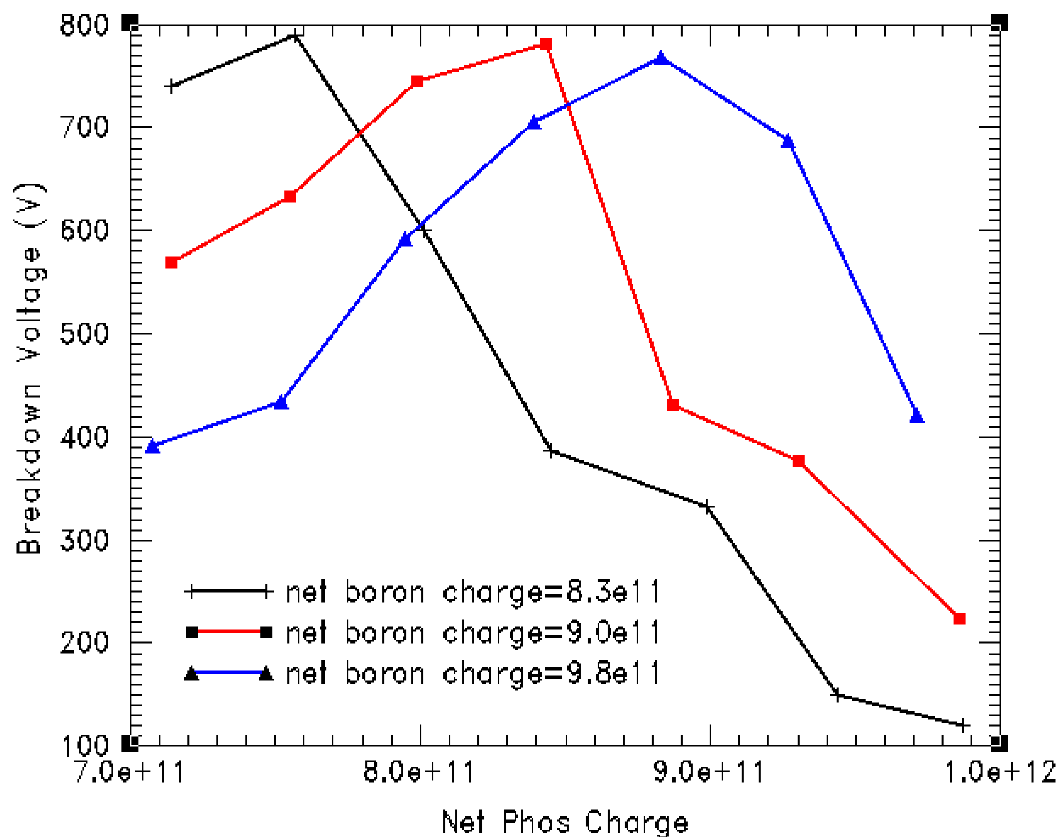
Breakdown Voltage vs. Charge Balance



The device breakdown voltage can be controlled through the charge balance relationships. The ratio of n:p in the trench can be readily controlled to <5%, providing a >30% process window for production.

From ISPSD 2011, “Best Paper Award”, P. Moens et al, ON Semiconductor.

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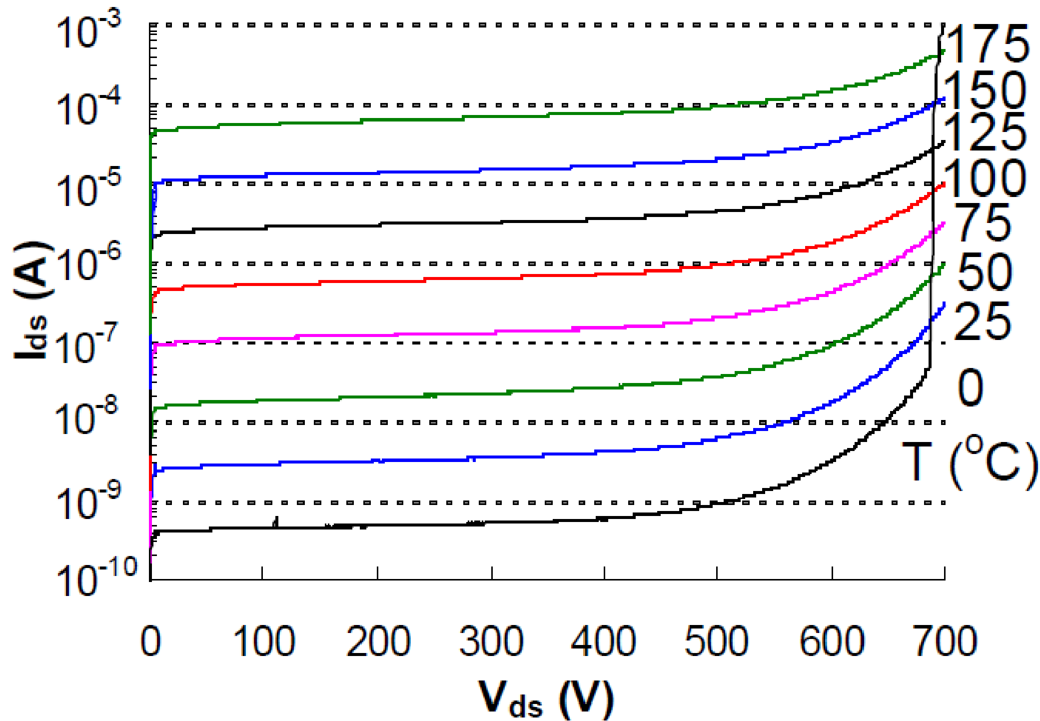
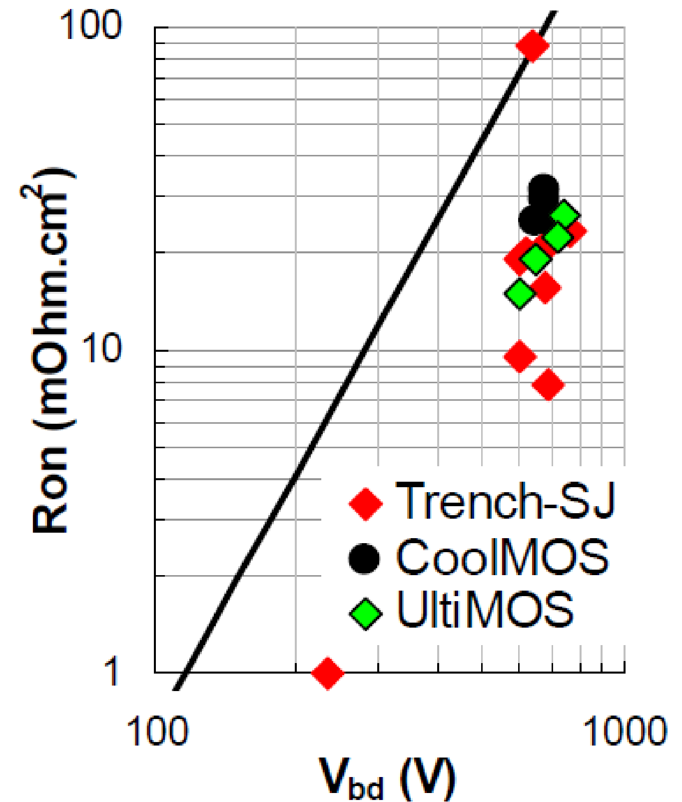
High Voltage Device Performance





Off-state leakage current vs. bias and temperature.
(The test system was limited to 700V)

From ISPSD 2011, “Best Paper Award”,
P. Moens et al, ON Semiconductor.

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Nano-materials for Die Attachment
“The Backend”

Die Attachment/Assembly Considerations

- "Die Attachment"- Bonding the electronic device to a leadframe, or other anchor/support, for packaging and interconnection

- Properties and Dimensions:
  - Provide the highest possible electrical and thermal conductivity to the leadframe, or circuit board
  - Thinnest possible bond line:
    - Minimize any physical impact of the bond line
    - Minimal material- lowest resistance to heat and current flow, cost savings, consistent with a reliable, strong bond structure
    - Overall height of die-bond-leadframe-encapsulant structure
  - Strong bond structure, preferably near the material mechanical limits

Die Attachment/Assembly Considerations- 2

- Materials options:
  - Metals- "solders", preferably re-flowable at modest temperatures, without deleterious phase formation or excessive casting shrinkage (voiding).
  - Limitations in temperatures and compositions (phase diagram relations) to avoid excessive heating of the electrical devices.
  - Pb-Sn solders, various combinations of tin, indium, antimony, gold, silver, and other alloying components have been used over the past >100 years.
  - International legislation limits the use of many "old standards" for die attachment- the RoHS ("non-lead") solders.
  - Newer solders, compounded to avoid the "Pb hazards", have a number of issues related to thermal cycling, Ostwald ripening, and mechanical degradation (c.f., YouTube™ videos on reflowing PS2 motherboards.)
  - Epoxies, typically with filler materials (metals)
    - Compromise thermal and electrical behavior for cost considerations.

- Question: Can we manipulate materials, thermodynamics and kinetics to achieve a low-temperature, low-stress, high conductivity bond, while maintaining high bond integrity, relatively low costs, and RoHS requirements?

"Nano" materials!

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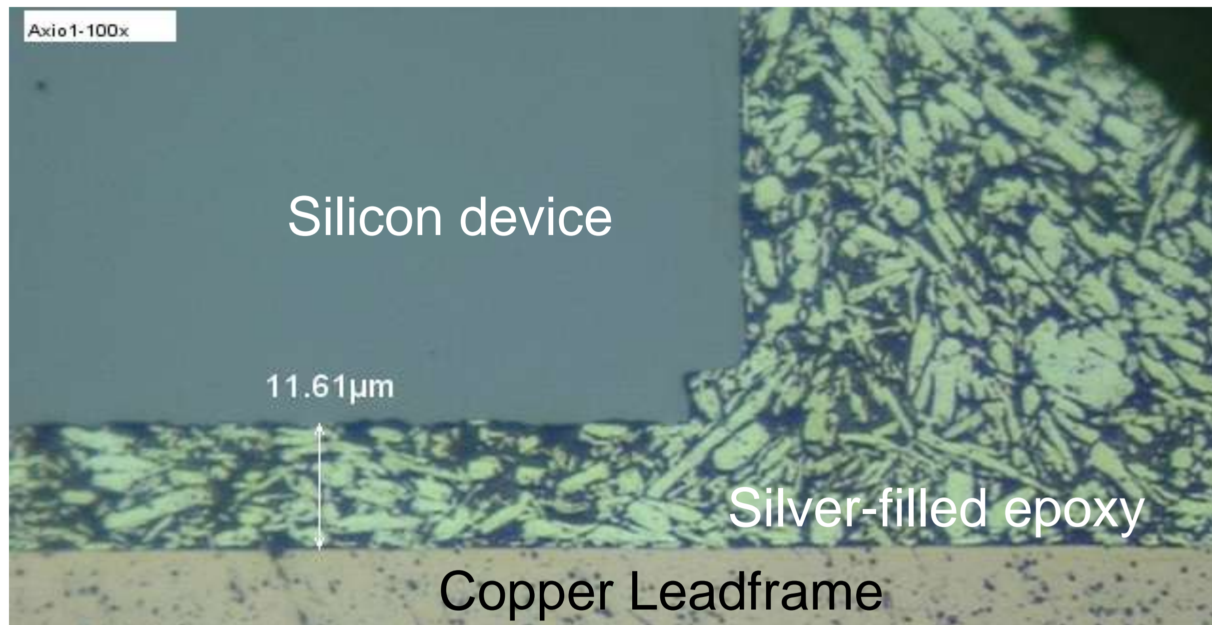
Materials Physics and Die Attachment

- Filled epoxies-
  - Macroscopic pieces of conducting material(s), typically silver or gold, dispersed within the epoxy matrix.
  - Thermal and electrical conductivity is significantly enhanced by the presence of the metal.
- The metal flakes act as thermal shunts to help conduct the heat to the leadframe
- Electrical conductivity occurs by the myriad "connections" between the metal flakes.
- The fill content is critical to both the electrical and thermal behavior of the die attachment.



Optical micrograph of a silicon die affixed to a copper leadframe with silver-filled epoxy.

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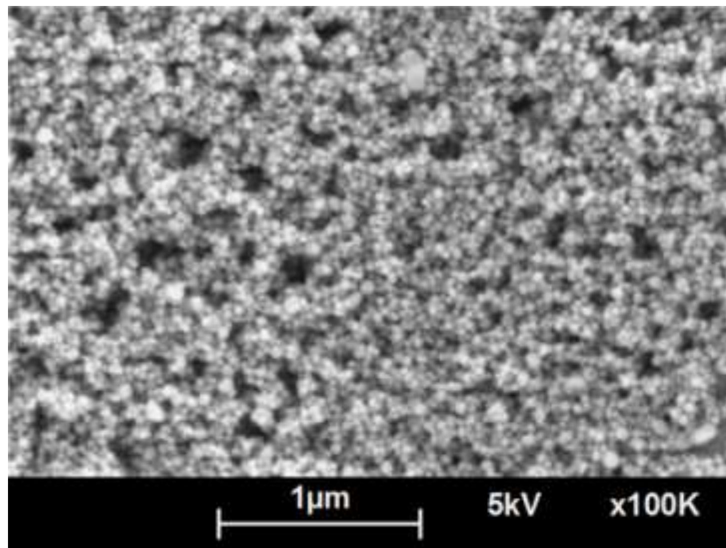
A New Generation of Die Attachment

- Consider "nano-particles" of conducting metals that do not have a strong native oxide: gold, silver, copper, tin, platinum, etc.; *not* materials like aluminum
- Companies such as NBE Tech, Henkel, DOWA, Nihon Handa, and others are investigating this new class of materials

- The basic concept:
  - Gibbs Free Energy- $\Delta G_s = \Delta H_s - T^*\Delta S_s$; if the driving force is negative a reaction *can* "go"
  - Ostwald- described particle growth from a fluid suspension- extend this thinking to fluid-enhanced surface reactions
  - Nano-particles are "all surface"- with a *huge* amount of surface free energy
  - Use the free energy of the nanoparticle surfaces to "melt" the materials ***far*** below their bulk melting point!

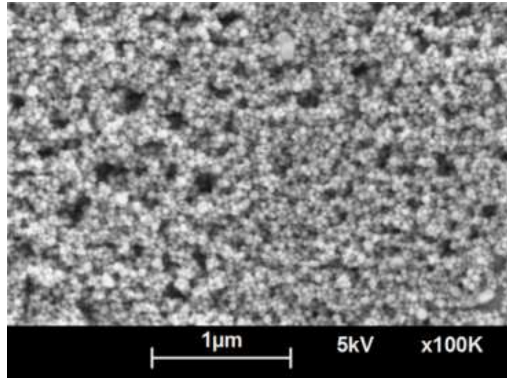
Starting point:



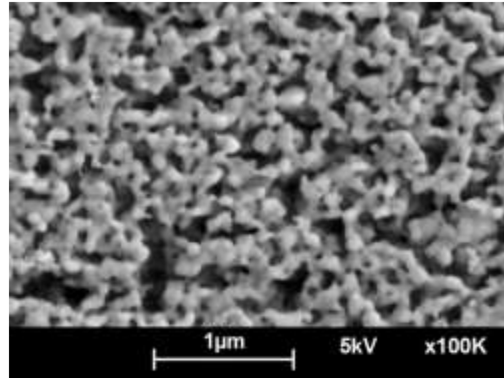
~100A silver particles in a mixed solvent-carrier

Images courtesy of G-Q Lu, NBE Tech

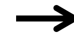
Microstructural Evolution of Sintering nanosilver™

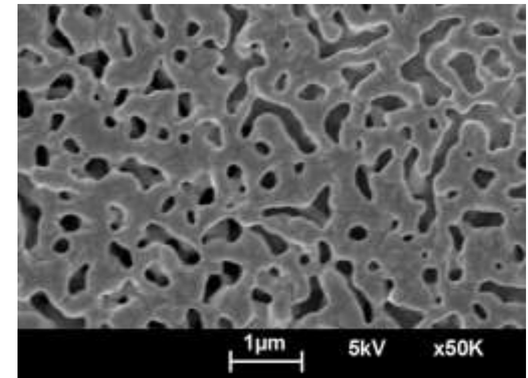


200°C

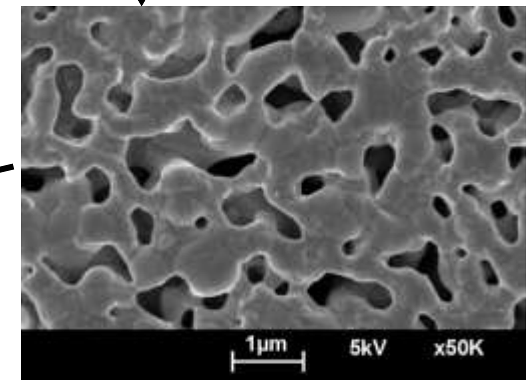


240°C

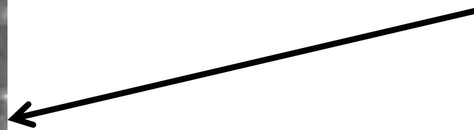


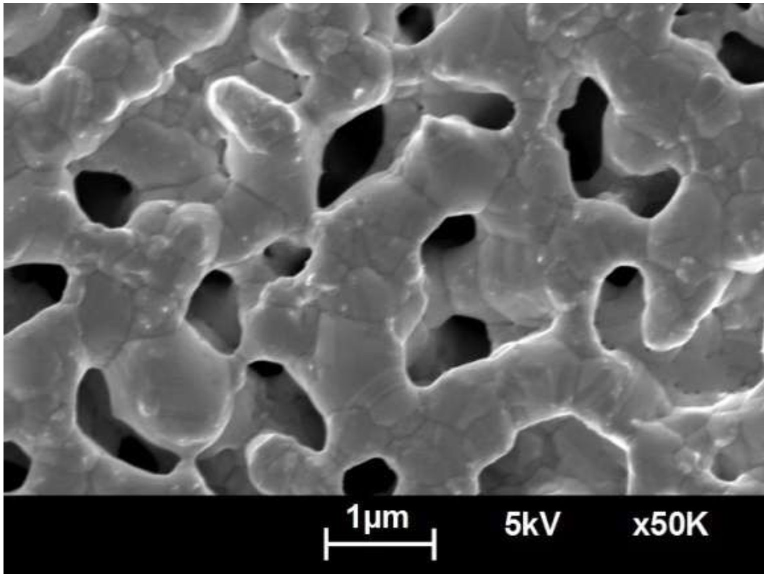


260°C



275°C



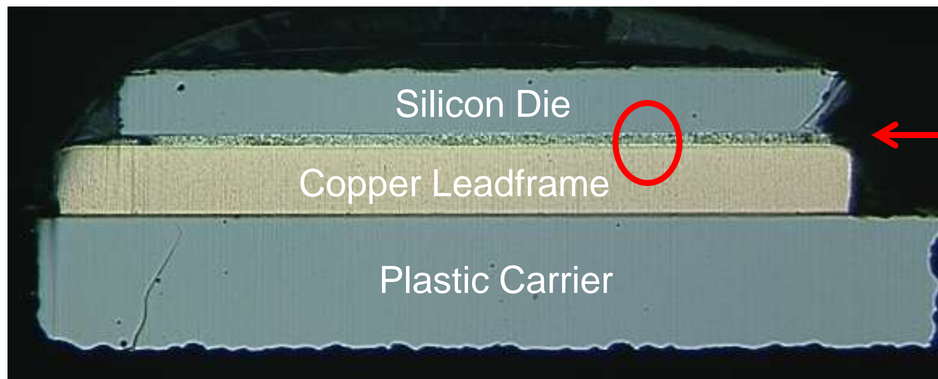


275°C after 10 minutes

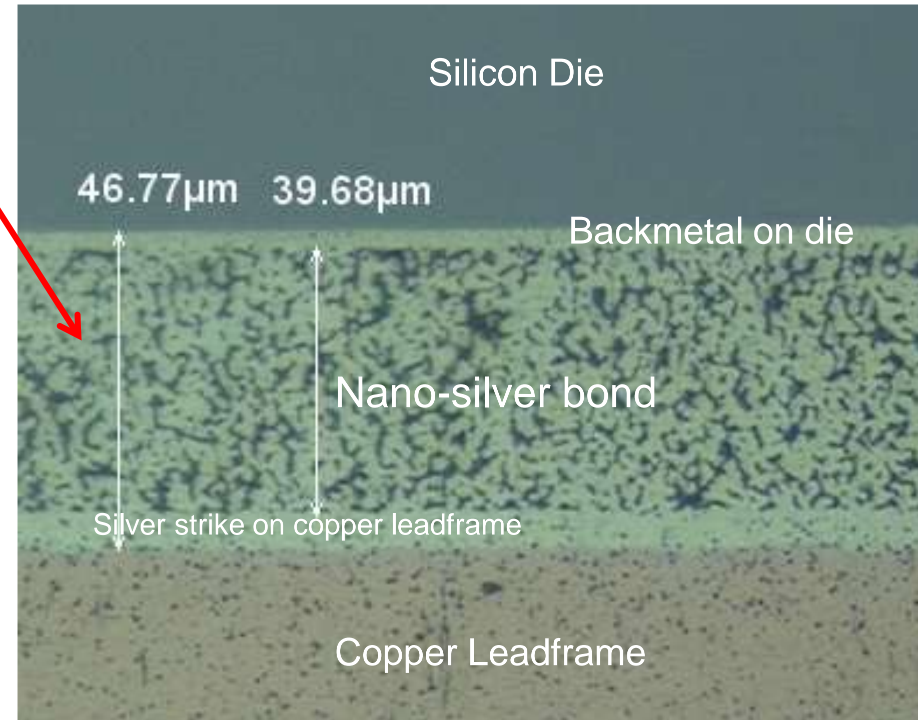
Fusion of the nano-silver particles, grain growth, forming a continuous matrix. Allows for excellent thermal and electrical conduction, accommodates differential thermal expansion, and exhibits extremely high shear loading capabilities.

Images courtesy of G-Q Lu, NBE Tech

Cross-sectional Images of nano-silver^{tm} Die Attachment



Nano-silver bond



- The fused nano-silver matrix forms a high-integrity bond between the die and the leadframe
- Die shear strength of this bond meets or exceeds that of standard Pb-Sn or RoHS solders
- The silver microstructure provides for excellent thermal cycling behavior
- The silver provides a very low resistivity current path to the leadframe

Summary

- Presented concepts for high voltage silicon FET designs that incorporate “nano” dimensions in their fabrication, with extremely high levels of performance.

- Showed a new approach to high voltage devices that relies on “nano-scale” control of epitaxial growth for performance advantages.

- Demonstrated a new paradigm for die attachment that employs thermo-physical interactions, rather than “brute-force” melting and solidification in the assembly process.