Power Magnetics @ High Frequency
State-of-the-Art and Future Prospects

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Swiss Federal Institute of Technology (ETH) Zurich
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“Transforming Magnetics ‘Black Magic’ into Engineering”
A Workshop prior to APEC 2017
Sponsored by the PSMA Magnetics Committee
And
IEEE Power Electronics Society (PELS)

Saturday, March 25th, 2017
7:00 am – 6:00 pm

Sessions

- AC Power Loss Measurements
- Technology Demonstration
- Technical Issues
- AC Power Loss Modeling
Outline

► Impact of Magnetics on Conv. Performance
► Losses Due to Stresses in Ferrite Surfaces
► The Ideal Switch is NOT Enough!
► Challenges in MV/MF Power Conversion
► Future Prospects
Introduction

Converter Performance Indicators
Design Space / Performance Space
Power Electronics Converter Performance Indicators

- Power Density \([\text{MW/dm}^3]\)
- Power per Unit Weight \([\text{MW/kg}]\)
- Relative Costs \([\text{MW/$}]\)
- Relative Losses \([\%]\)
- Failure Rate \([\text{h}^{-1}]\)

Environmental Impact... \[
\begin{align*}
\text{kg}_{\text{Fe}} / \text{kW} \\
\text{kg}_{\text{Cu}} / \text{kW} \\
\text{kg}_{\text{Al}} / \text{kW} \\
\text{cm}^2_{\text{Si}} / \text{kW}
\end{align*}
\]

State-of-the-Art

Future

Time-to-Market

Costs

Losses

Weight

Volume

Failure Rate
Performance Limits (1)

- Example of Highly-Compact 1-Φ PFC Rectifier
- Two Interleaved 1.6kW Systems

\[ P_0 = 3.2kW \]
\[ U_N = 230V \pm 10\% \]
\[ U_0 = 400V \]

\[ f_p = 450kHz \pm 50kHz \]

\[ \eta = 95.8\% \text{ @ } \rho = 5.5 \text{ kW/dm}^3 \]

CoolMOS
SiC Diodes

High Power Density @ Low Efficiency
Trade-Off Between Power Density and Efficiency
Performance Limits (2)

- Example of Highly-Efficient 1-Φ PFC Rectifier
- Two Interleaved 1.6kW Systems

\[ P_0 = 3.2kW \]
\[ U_N = 230V \pm 10\% \]
\[ U_0 = 365V \]

\[ f_P = 33kHz \pm 3kHz \]

★ \[ \eta = 99.2\% \ @ \ \rho = 1.1 \ kW/dm^3 \]

→ High Efficiency  @ Low Power Density  
→ Trade-Off Between Power Density and Efficiency
Abstraction of Power Converter Design

Performance Space

- Efficiency
- Power Density
- Costs
- Reliability
- etc.

System
- Phase-Shift DC/DC Conv.
- Resonant DC/DC Conv.
- DC Link AC/AC Conv.
- Matrix AC/AC Conv.
- etc.

Components
- Power Semiconductor
- Interconnections
- Inductors, Transf.
- Capacitors
- Control Circuit
- etc.

Materials
- Semiconductor Mat.
- Conductor Mat.
- Magnetic Mat.
- Dielectric Mat.
- etc.

Design Space

- Evaluation Formulas
- Lifetime Models
- Cost Models
- etc.

- Specifications
- Operation Limits
- Converter Topology
- Modulation Scheme
- Control Concept
- Operation Mode
- Operating Freq.
- etc.

- Doping Profiles
- Geometric Properties
- Winding Arrangements
- Magnetic Core Geometries
- etc.

→ Mapping of “Design Space” into “Performance Space”
Derivation of $\eta$-$\rho$-Performance Limit of Converter Systems

Component $\eta$-$\rho$-Characteristics
Converter $\eta$-$\rho$-Pareto Front
Derivation of the $\eta$-$\rho$-Performance Limit

- Example of DC/AC Converter System

- Key Components
  - Storage Capacitor
  - Semiconductors & Heatsink
  - Output Inductor
  - Auxiliary Supply

→ Construct $\eta$-$\rho$-Characteristics of Key Components
→ Determine Feasible System Performance Space
**η-ρ-Characteristic of Power Semiconductors / Heatsink**

- Semiconductor Losses are Translating into Heat Sink Volume
- Heatsink Characterized by *Cooling System Performance Index* (CSPI)
- Volume of Semiconductors Neglected

\[
P_H = (1 - \eta_H) P_I = (1 - \eta_H) \frac{P_O}{\eta_H}
\]

\[
P_H = \frac{\Delta T_{s-a}}{R_{th}} = \Delta T_{s-a} \frac{G_{th}}{\dot{g}_{th}} = \Delta T_{s-a} \frac{CSPI \cdot V_H}{\dot{g}_{th}}
\]

\[
\frac{(1 - \eta_H)}{\eta_H} P_O = \frac{\alpha_H}{\Delta T_{s-a}} CSPI \cdot V_H
\]

\[
\rho_H = \frac{P_O}{V_H} = \alpha_H \cdot \frac{\eta_H}{(1 - \eta_H)}
\]

⇒ Heatsink Defines a Converter Limit \( \rho \leq \rho_H \)

\[
CSPI = \frac{G_{th}}{V_H} \left[ \frac{W}{dm^3K} \right]
\]
**η-ρ-Characteristic of Storage+Heatsink+Auxiliary**

- Overall Power Density Lower than Lowest Individual Power Density
- Total Efficiency Lower than Lowest Individual Efficiency

\[ V = V_C + V_H + V_{aux} \quad \eta = \frac{1}{\rho_0} \]

\[ \rho_i = \frac{P_i}{V_i} \quad P_l = P_0 + \sum P_i = \frac{P_0}{\eta} \]

\[ \rho^{-1} = \rho_C^{-1} + \rho_H^{-1} + \rho_{aux}^{-1} \]

- Example of Heat Sink+Storage (No Losses)

\[ \rho_C = \beta_C \gamma_C \]

\[ \rho_H = \Delta T_{s-a} \frac{CSPI}{\alpha_H} \cdot \frac{\eta_H}{(1 - \eta_H)} \]

\[ \rho_{CH} = \frac{\beta_C \gamma_C}{1 + \left(\frac{1 - \eta_H}{\eta_H}\right) \beta_C \gamma_C \alpha_H^{-1}} \]

\[ \Rightarrow \eta-\rho \text{ Characteristic w/o Magnetics} \]

\[ \Rightarrow \text{Higher Sw. Frequ. Leads to Larger Volume} \]
**η-ρ-Characteristic of Inductor (1)**

- **Inductor Flux Swing Defined by DC Voltage & Sw. Frequ. (& Mod. Index)**

- **“-1”-Order Approx. of Volume-Dependency of Losses**

\[
\Delta \hat{B} = \frac{U_{DC}}{NA_F} \frac{1}{T_P} \propto \frac{U_{DC}}{f_p A_F} \propto \frac{1}{A_F} \propto \frac{1}{l^2} \rightarrow P_E \propto f_p \Delta \hat{B}^\rho V_E \propto \frac{1}{l^3} \propto \frac{1}{l}
\]

\[
P_W = I_{rms}^2 R_W \propto \frac{l}{\kappa A_W} \propto \frac{l}{l^2} \propto \frac{1}{l}
\]

- **„0“-Order Approx. (N_{opt})**

\[
P_L = k \sum \frac{4(2-\beta)}{3} \frac{1}{f_p} \frac{2(\alpha-\beta)}{2+\beta} \frac{2\beta}{t_{rms}} \frac{U_{DC}}{V_L} \frac{2\beta}{l} \left| \begin{array}{c} \alpha = 1 \\ \beta = 2 \end{array} \right| \propto \frac{U_{DC} I_{rms}}{\sqrt{f_p V_L}}
\]

\rightarrow \text{Losses are Decreasing with Increasing Linear Dimensions & Sw. Frequency}
η-ρ-Characteristic of Inductor (2)

- Minimization of the Losses of an Inductor of a 3 kW Step-Down DC/DC Converter
  - $U_1 = 400\text{V} / U_2 = 200\text{V}$
  - N87 Magnetic Cores
  - 71um Litz Wire Strand Diameter (35% Fill Factor)
  - Consideration of HF Winding and Core Losses
  - Thermal Limit Acc. to Natural Convection (0.1W/cm$^2$, 14W Total)

Calc. of Opt. # of Turns in Limits: $N \geq 1, N_{\text{min}}$ Avoiding Sat. (incl. DC Curr.), $N_{\text{max}}$ as for Air Core

HF Wdg. Losses: 2D Analy. Approx. / HF Core Losses: $iGSE$ (DC Premagnetization Not Consid.)
- **η-ρ-Characteristic of Inductor (3)**

  - Loss Minimiz. by Calculation of Opt. # of Turns
  - Consideration of HF Winding and Core Losses
  - Thermal Limit Acc. To Natural Convection
  - Assumption: Given Magnetic Core

  ➔ Higher Sw. Freq. – Lower Min. Ind. Losses – Overall Loss Red. Limited by Semicond. Sw. Losses
**η-ρ-Characteristic of Inductor (3)**

- Overall Power Density Lower than Lowest Individual Power Density
- Total Efficiency Lower than Individual Efficiency

\[
P_L \propto \frac{U_{DC} I_{rms}}{\sqrt{f_P V_L}} \propto \frac{P_o}{\sqrt{f_P V_L}} \quad (= k_{L,\text{max}} V_L^2)
\]

\[
P_L = (1 - \eta_L) P_I = (1 - \eta_L) \frac{P_o}{\eta_L}
\]

\[
\rho_L = \frac{P_o}{V_L} \propto P_o f_P^3 \frac{(1 - \eta_L)^3}{\eta_L^3}
\]

- Natural Convection

\[\rho_{L,\text{max}} \propto \sqrt{f_P}\]

→ η-ρ Characteristic of Inductors
→ Higher Sw. Freq. Leads to Lower Vol.
→ Allowed Losses Defined by Cooling
Remark - Natural Conv. Thermal Limit (1)

- Example of Highly-Compact 3-Φ PFC Rectifier
- Nat. Conv. Cooling of Inductors and EMI Filter
- Semiconductors Mounted on Cold Plate

\[ P_p = 10 \text{ kW} \]
\[ U_N = 230V_{AC} \pm 10\% \]
\[ f_N = 50\text{Hz} \text{ or } 360\ldots800\text{Hz} \]
\[ U_o = 800V_{DC} \]
\[ f_p = 250\text{kHz} \]

\[ \rho = 10 \text{ kW/dm}^3 \quad @ \quad \eta = 96.2\% \]

- Systems with \( f_p = 72/250/500/1000\text{kHz} \)
- Factor 10 in \( f_p \) - Factor 2 in Power Density
**Remark - Natural Conv. Thermal Limit (2)**

- Example of Highly-Compact 3-Φ PFC Rectifier
- Nat. Conv. Cooling of Inductors and EMI Filter
- Semiconductors Mounted on Cold Plate

\[
P_P = 10 \text{ kW} \\
U_N = 230V_{AC} \pm 10\% \\
f_N = 50\text{Hz} \text{ or } 360...800\text{Hz} \\
U_0 = 800V_{DC} \\
f_P = 250\text{kHz}
\]

\[\rho = 10 \text{ kW/dm}^3 \quad @ \quad \eta = 96.2\%\]

- Systems with \(f_P = 72/250/500/1000\text{kHz}\)
- Factor 10 in \(f_P\) – Factor 2 in Power Density
**η-ρ-Characteristic of Inductor (4)**

- Natural Convection Heat Transfer Seriously Limits Allowed Inductor Losses
- Higher Power Density Through Explicit Inductor Heatsink

**Natural Convection**

\[
P_L = \frac{(1-\eta_L)}{\eta_L} P_o \leq k_{L,\text{max}} V_L^2 = k_{L,\text{max}} \left( \frac{P_o}{\rho L} \right)^{\frac{3}{2}}
\]

\[
\rho_{L,\text{max}} = k_{L,\text{max}} \left( \frac{\eta_L}{1-\eta_L} \right)^{\frac{3}{2}} P_o^{-\frac{1}{2}}
\]

**Explicit Heatsink**

\[
\rho_{LH,\text{max}} \approx \frac{1}{2} \rho_{H,\text{max}} (\eta_L)
\]

**Heat Transfer Coefficients**

- \(k_i\) and \(\alpha_i\) Dependent on Max. Surface Temp. / Heatsink Temp.
- Water Cooling Facilitates Extreme (Local) Power Densities
**Remark – Example for Explicit Heatsink for Magn. Component**

- Phase-Shift Full-Bridge Isolated DC/DC Converter with Current-Doubler Rectifier
- Heat Transfer Component (HTC) & Heatsink for Transformer Cooling
- Magn. Integration of Current-Doubler Inductors

\[
\begin{align*}
P_D &= 5\text{ kW} \\
U_{in} &= 400\text{ V} \\
U_0 &= 48\ldots56\text{ V} (300\text{ mV}_{pp}) \\
T_a &= 45^\circ\text{C}
\end{align*}
\]

\[f_p = 120\text{ kHz}\]

\[9\text{ kW/dm}^3 (148\text{ W/in}^3) @ 94.5\%\]
Remark – Example for Explicit Heatsink for Magn. Component

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\[ T_a = 45\degree \text{C} \]

\[ f_P = 120\text{kHz} \]

★ 9\text{ kW/dm}^3 (148 \text{W/in}^3) @ 94.5\%
**Overall Converter η-ρ-Characteristics**

- **Low Semiconductor Sw. Losses**
  - **High Sw. Losses** / **Low Sw. Frequ.** / **Small Heatsink** / **Small Ind.** / **High Total Power Density**
  - **High Sw. Losses** / **Low Sw. Frequ.** / **Large Heatsink** / **Large Ind.** / **Low Total Power Density**
Reduction of Inductor Requirement

→ Parallel Interleaving
→ Series Interleaving
**Inductor Volt-Seconds / Size**

- Inductor Volt-Seconds are Determining the Local Flux Density Ampl.
- Output Inductor has to be Considered Part of the EMI Filter
- Multi-Level Converters Allow to Decrease Volt-Seconds by Factor of $N^2$
- Calculation of Equivalent Noise Voltage @ Sw. Frequency (2$^{nd}$ Bridge Leg w. Fund. Frequ.)

\[ \Delta \hat{B} \propto \frac{T_p U_{DC}}{A_E} \propto \frac{U_{DC}}{f_p A_E} \]

\[ M = \frac{\hat{U}_o}{U_{DC}} \]

\[ U_{f_p, eq, rms} = U_{AC, rms} - U_{O, rms}^2 \]

\[ U_{f_p, eq, rms} = \sqrt{M \left( \frac{2}{\pi} - \frac{M}{2} \right) U_{DC}} \]

→ EMI Filter Design Can be Based on Equiv. Noise Voltage
Reduction of Inductor Volt-Seconds / Size

- Multi-Level Characteristic through Series-Interleaving
- Multi-Level Characteristic through Parallel Interleaving

\[ \Delta \hat{B} \propto \frac{T_p \cdot U_{DC}}{N} \cdot \frac{N}{A_E} \]

- Identical Spectral Properties for Both Concepts
- Series Interleaving Avoids Coupling Inductor of Parallel Interleaving!
**Multi-Level Converter Approach**

- Multi-Level PWM Output Voltage – Minimizes Ind. Volume
- Flying Cap. Conv. – No Splitting of DC Inp. Voltage Required
- Low-Voltage GaN or Si Power Semiconductors

**FIG. 1**

**FIG. 4**

Transformers

Optimal Operating Frequency
Example of MF/MV Transformer
Future Direct MV Supply of 400V DC Distribution of Datacenters

- Reduces Losses & Footprint / Improves Reliability & Power Quality
- Unidirectional Multi-Cell Solid-State Transformer (SST)
- AC/DC and DC/DC Stage per Cell, Cells in Input Series / Output Parallel Arrangement

— Conventional US 480V\textsubscript{AC} Distribution

— Facility-Level 400 V\textsubscript{DC} Distribution

→ Unidirectional SST / Direct 6.6kV AC → 400V DC Conversion
Example of a 166kW/20kHz SST DC/DC Converter Cell

- Half-Cycle DCM Series Resonant DC-DC Converter

- Medium-Voltage Side 2kV
- Low-Voltage Side 400V
MF Transformer Design

- DoF – Electric (# of Turns & Op. Frequ.) / Geometric / Material (Core & Wdg) Parameters
- Cooling / Therm. Mod. of Key Importance / Anisotr. Behavior of Litz Wire / Mag. Tape
- 20kHz Operation Defined by IGBT Sw. Losses / Fixed Geometry

→ Region I: Sat. Limited / Min. Loss @ $P_c/P_w = 2/\beta$ ($R_{AC}/R_{DC} = \beta/\alpha$) / Region III: Prox. Loss Domin.
→ Heat Conducting Plates between Cores and on Wdg. Surface / Top/Bottom H₂O-Cooled Cold Plates
**MF Transformer Prototype**

- **Power Rating**: 166 kW
- **Efficiency**: 99.5%
- **Power Density**: 44 kW/dm³

- **Nanocrystalline Cores** with 0.1mm Airgaps between Parallel Cores for Equal Flux Partitioning

- **Litz Wire** (10 Bundles, 950 x 71μm Each) with CM Chokes for Equal Current Partitioning
Calculation of Converter $\eta$-$\rho$-Performance Limits
Selected Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

→ ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
→ Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure
High Frequency Inductors (1)

- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- \( L = 10.5 \mu H \)
- 2 x 8 Turns
- 24 x 80\( \mu m \) Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 \( \mu m \) Copper Foil / 4 in Parallel
- 7 \( \mu m \) Kapton Layer Isolation
- 20\( m\Omega \) Winding Resistance / \( Q \approx 600 \)
- Terminals in No-Leakage Flux Area

\( \Rightarrow \) Dimensions - 14.5 x 14.5 x 22mm\(^3\)
Multi-Airgap Inductor Core Loss Measurements (1)

- Investigated Materials – DMR51, N87, N59
- 30 µm PET Foil with Double Sided Adhesive Between the Plates
- Varying Number $N$ of Air Gaps Assembled from Thin Ferrite Plates
- Number of Air Gaps:
  - Solid $N=6$
  - $N=20$

$\Rightarrow$ Sinusoidal Excitation with Frequencies in the Range of 250 kHz ...1MHz
Multi-Airgap Inductor Core Loss Measurements (3)

- Losses in Sample – Increasing Temperature
- Excitation with 100 mT @ 750 kHz
- Start @ T=35°C
- Excitation Time = 90 s

Solid, $\Delta T = 27.7^\circ C$

$N=20$, $\Delta T = 73.5^\circ C$
Multi-Airgap Inductor Core Loss Approximation (2)

- Total Core Loss in Sample with Varying Air Gaps and Test Fixture
- Excitation @ 500 kHz

\[ P_{\text{loss}} (\text{Watt}) \]

\[
\begin{align*}
\# \text{Air Gaps} & \quad \# \text{Air Gaps} & \quad \# \text{Air Gaps} \\
\end{align*}
\]

- Linear Fit of Measurements
- Analytical Approximation of \( P_{\text{loss}} (N) \)

\[ \Rightarrow \text{Ext. of Steinmetz Eq.} \quad P_V = k_0 f^\alpha \hat{B}^\beta \left( V_C \left( \frac{A_S}{A_C} \right)^\beta + V_S \right) + k_S f^{\alpha_S} \hat{B}^{\beta_S} \cdot N \cdot A_S \quad \text{Sufficiently Accurate} \]
DMR 51 Untreated – FIB Preparation (1)
DMR 51 ETCHED – FIB Preparation (2)
Little-Box 1.0 Prototype

- **Performance**
  - 8.2 kW/dm³
  - 96.3% Efficiency @ 2kW
  - $T_c=58{}^\circ C$ @ 2kW

- **Design Details**
  - 600V IFX Normally-Off GaN GIT
  - Antiparallel SiC Schottky Diodes
  - Multi-Airgap Ind. w. Multi-Layer Foil Wdg
  - Triangular Curr. Mode ZVS Operation
  - CeraLink Power Pulsation Buffer

→ Analysis of Potential Performance Improvement for “Ideal Switches”
Little-Box 1.0 Prototype

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→ Analysis of Potential Performance Improvement for “Ideal Switches”

★ 135 W/in³
Little Box 1.0 @ Ideal Switches (TCM)

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_C = 0$ (Zero Cond. Losses); $k_S = 0$ (Zero Sw. Losses)

Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density

The Ideal Switch is NOT Enough (!)
Future Prospects of Power Electronics

MV / MF Power Electronics

Smart Microgrids, DC Distribution

100 kW

Standard / Integrated Solutions

10 W

System Applications

Micro Power Electronics

Microelectronics Technology, Power Supply on Chip

Future Extension of Power Electronics Application Area
Future Prospects of Magnetics

■ Side Conditions
- Magnetics are Basic Functional Elements (Filtering of Sw. Frequ. Power, Transformers)
- Non-Ideal Material Properties (Wdg. & Core) Result in Finite Magnetics Volume (Scaling Laws)
- Manufacturing Limits Performance (Strand & Tape Thickness etc.) @ Limited Costs

■ Option #1: Improve Modeling / Optimize Design
- Core Loss Modeling / Measurement Techniques (Cores and Complete Ind. / Transformer)
- Multi-Obj. Optimiz. Considering Full System
- Design for Manufacturing

■ Option #2: Improve Material Properties / Manufacturing
- Integrated Cooling
- PCB-Based Magnetics with High Filling Factor (e.g. VICOR)
- Advanced Locally Adapted Litz Wire / Low-μ Material (Distributed Gap) / Low HF-Loss Material

■ Option #3: Minimize Requirement
- Multi-Level Converters
- Magnetic Integration
- Hybrid (Cap./Ind.) Converters

→ Magnetics/Passives-Centric Power Electronics Research Approach!
Thank You!