TEXAS INSTRUMENTS

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Whisker Evaluation of Tin-Plated Logic Component Leads

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Logic Packaging

ABSTRACT

Integrated circuits (ICs) with matte tin (Sn) finished leads for logic products were tested for Sn-whisker-growth susceptibility. The ICs were obtained from several assembly-test subcontractors (subcons). The conditions used to promote Sn-whisker growth are typical for the industry: 51°C and 51°C + 85% RH. In addition, the same conditions were imposed on board-mounted ICs that had a 5-V bias applied to adjacent leads. Biasing of leads in a Sn-whisker test is not typical in the industry, but we believe it represents an in-use condition.

The results of these tests were not as expected. Conventionally, the matte Sn finish is thought to be less prone to whiskers. We found whiskers on some matte-Sn-finished components and no whiskers on other matte-Sn-finished components. We found whiskers on some larger Sn-grain deposits and no whiskers on some finer Sn-grain deposits. This is contrary to much of the literature. Also, we found whiskers quite consistently on the biased samples, but not on the parallel run of parts with no bias. Also, we saw whiskers grow on some units that were in shelf storage for several months, with no exposure to the whisker-test conditions.

This paper highlights the risks associated with Sn-plated leads and the potential for Sn whiskers. The propensity of a Sn finish to develop Sn whiskers is not easy to predict. Results lend credence to the notion that there are likely a multiplicity of mechanisms for Sn-whisker growth.

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Introduction

Many integrated circuit (IC) manufacturers are qualifying, or planning to qualify, matte tin (Sn) finish as a lead (Pb)-free replacement for tin-lead (SnPb) on component leads.[1,2] The target packages for a Sn finish are peripherally leaded surface-mount packages, exclusive of ball grid arrays. Sn-whisker growth is a concern with Sn-plated components. Whiskers are spontaneous filamentous or needlelike growths from the Sn surface.[3–6] The whiskers have the potential to short adjacent leads or break off and short or cause mechanical problems in other regions (such as in a disk drive) of an electronic assembly.

Whiskers can take various forms, from needlelike, to hillocks, to columns, to flowerlike projections. Of most concern are the columnar or needlelike whiskers because they are most likely to create an electrical short.[7]

There are several theories about what causes Sn whiskers. Some of the more compelling ones are:

- Surface oxidation of the Sn causes screw dislocations in the bulk Sn to move up, but whiskers grow in a vacuum.[8]
- Co-deposited hydrogen during electroplating induces stresses that produce whiskers, but whiskers grow on vapor-deposited Sn.[9]
- Intermetallic formation, particularly SnCu after grain-boundary diffusion of Cu into the Sn, induces compressive stress in the Sn, but whiskers grow if Sn has no contact with Cu.[10]
- Mismatch in the coefficient of thermal expansion induces stresses in the Sn. This would apply to Sn on Fe-Ni alloys or other substrates with a low coefficient of thermal expansion.[11]

None of these theories has been shown to adequately account for all reported occurrences of Sn whiskers. It is likely that several factors can contribute to Sn-whisker growth, and these can act singly or in combination. A National Electronic Manufacturing Initiative (NEMI) working group is trying to determine the mechanism of whisker growth. This work should point to the underlying cause(s) and allow a coherent theory to be developed.

At the time of this writing, there is no industry standard for whisker-growth testing of Sn-finished units. A number of industry organizations are working on development of whisker-test methods: NEMI in North America,[12] The Japan Electronics and Information Technology Industries Association (JEITA), and the International Tin Research Institute (ITRI) in Europe.[13] Periodic updates by these organizations typically are presented at industry conferences.[14,15] There are two key issues in development of a standard whisker test. First, trying to prove a negative—that no whiskers will grow on a sample—inherently is a challenge. (What if the sample were allowed to age another day, 20 days, or a year—will a whisker show up?) Second, a common theme of the theories being put forth is that there is some stress in the Sn deposit, and the stress is relaxed by Sn-whisker growth. To develop any accelerated test for electronic components, energy—either thermal or mechanical—normally is pumped into the system to accelerate the desired reaction. In the case of Sn whiskers, too much thermal energy may anneal the Sn and take the stresses out, so there is an upper limit to how much heat a sample can withstand in an accelerated Sn-whisker test.

Complicating the development of a standard Sn-whisker-growth test are no accepted definitions of (1) what is a Sn whisker, (2) what is a rejectable Sn whisker, and (3) how should an Sn whisker sample be inspected (sampling and magnification). The good news is that these are all arbitrary, but can be defined in a straightforward manner. NEMI is addressing whisker definition and inspection protocol. As noted previously, the bigger issue (or bad news) is how to develop and define conditions that accelerate Sn-whisker growth and that ensure Sn-whisker growth in Sn deposits that, over time, will show Sn whiskers in the field.

TI defined four sets of parameters for in-house Sn-whisker-growth tests, based partially on work done at NEMI. The components tested had matte-Sn or tin-bismuth (SnBi)-plated leads and were built by IC package-assembly subcontractors (subcons).

Components Evaluated

Several IC packages procured from various IC assembly subcons were chosen for this evaluation. Key details of each package/finish option evaluated are shown in Table 1.

Table 1. Source and Plating Details for Each Package Evaluated

Subcon	Package	Finish	Type of Plating	Thickness (quoted) (microinch)	Average Thickness (measured) (microinch)	Nickel Layer	Additives	Carbon Content	Grain Size (measured) (µm)
A	SOIC	Sn	Matte	300–800	436	No	Yes	Not known	4.6–7.5
B	SOT	Sn	Matte	300–800	274	No	Yes	Not known	2.7–7.0
C	TO-220	Sn	Matte	300–800	357	No	Yes	0.003 %	3.3–9.4
D	SOT	Sn	Matte	200–1000	246	No	Yes	<200 ppm	4.6–7.8
E	QFN	Sn	Matte	300–1000	422	No	Yes	160 ppm	2.3–7.1
F	SOT	SnBi	NA	160–1000	195	No	Yes	NA	3.1–8.0

The left three columns indicate the IC package assembly subcon (coded), package style, and component finish. All Sn-finished components were classified by the subcon as matte finish. NEMI has defined matte and bright Sn finishes as shown in Table 2.[15]

Table 2. NEMI Definitions of Matte and Bright Sn Finishes

Parameter	Matte Sn	Bright Sn
Carbon content	0.005%–0.50%	0.2%–0.4%
Grain size	1 µm–5 µm	0.5 µm–0.8 µm

In their definition of bright Sn finishes, NEMI indicated that bright Sn essentially is featureless, by scanning electron microscope (SEM) inspection, is less ductile, and can be slightly harder than matte Sn. Table 1 indicates the plating-thickness range provided by the assembly subcon and the average plating thickness, which was measured by TI using X-ray fluorescence. Use of a nickel barrier layer is an option that is believed to affect whisker growth. None of the units tested had a nickel layer between the base metal and the Sn plate. All subcons used proprietary additives in the Sn plating baths. The carbon content of the plating assembly subcon also is given in Table 1. It is not known if this is by analysis or is quoted as typical by the plating-bath subcon. Grain size for each sample, measured by using a scanning electron microscope (SEM), is shown in Table 1.

Two factors are believed to minimize whisker formation: Sn-deposit thickness >8 μm or <0.5 μm and large (3 μm–8 μm diameter) well-polygonized grains.[16]

Figures 1–4 show isometric views of the various package types evaluated.

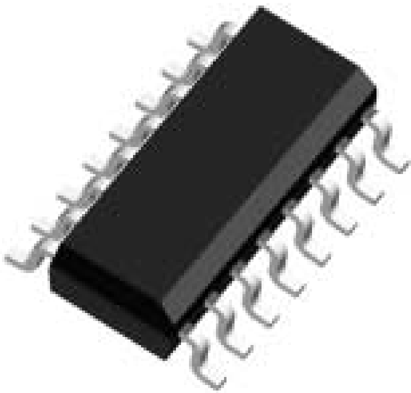

Figure 1. Isometric View of SOIC Gull-Wing Package

Figure 2. Isometric View of SOT Gull-Wing Package

Figure 3. Isometric View of TO-220 Through-Hole Package

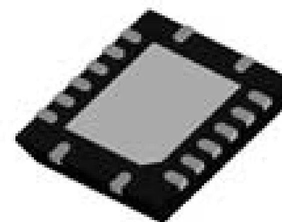

Figure 4. Isometric View of QFN Surface-Mount Package

Grain-Size Measurements

Grain size was measured for the components tested to classify the finish per NEMI recommendations. Examples of the grain structure seen on units from each subcon are shown in Figures 5–10.

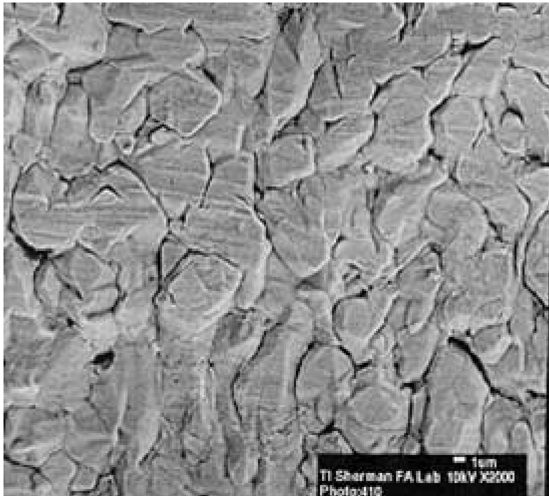

Figure 5. Grain Structure on Subcon A Tin-Plated SOIC Units, 2000X Magnification

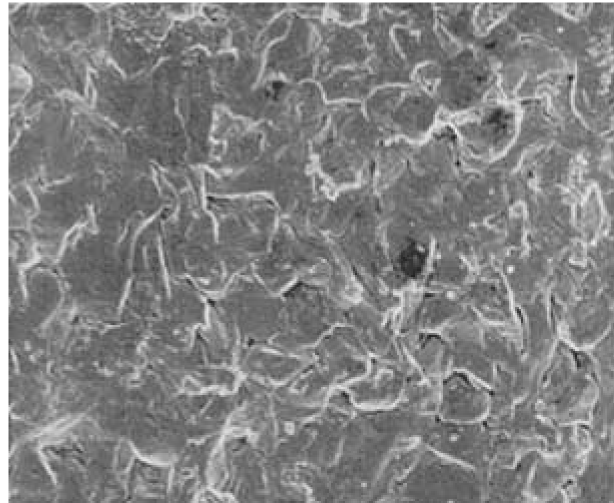

Figure 6. Grain Structure on Subcon B Tin-Plated SOT Units, 2000X Magnification

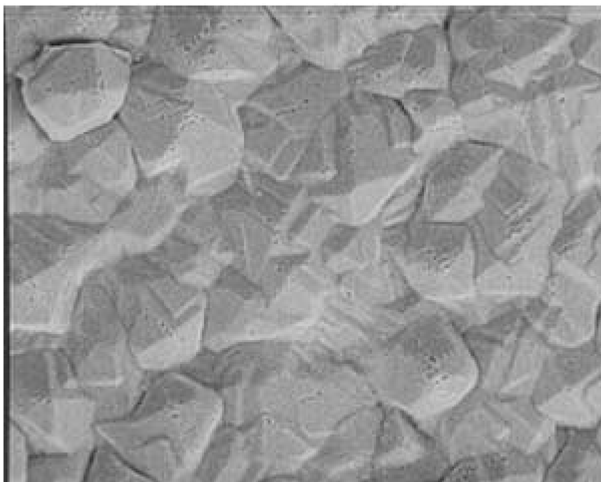

Figure 7. Grain Structure on Subcon C Tin-Plated TO-220 Units, 2000X Magnification

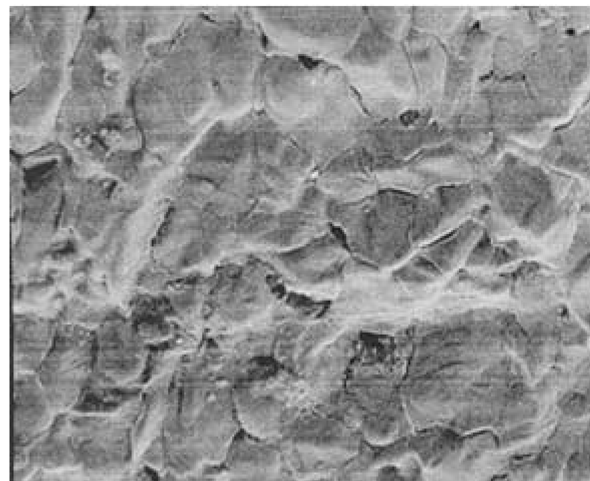

Figure 8. Grain Structure on Subcon D Tin-Plated SOT Units, 2000X Magnification

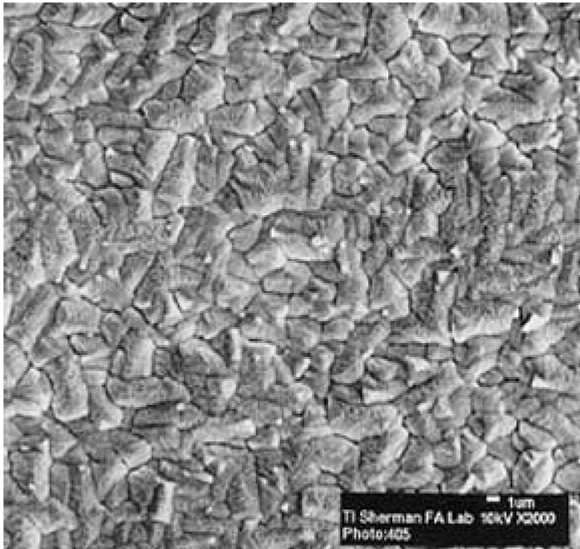

Figure 9. Grain Structure on Subcon E Tin-Plated QFN Units, 2000X Magnification

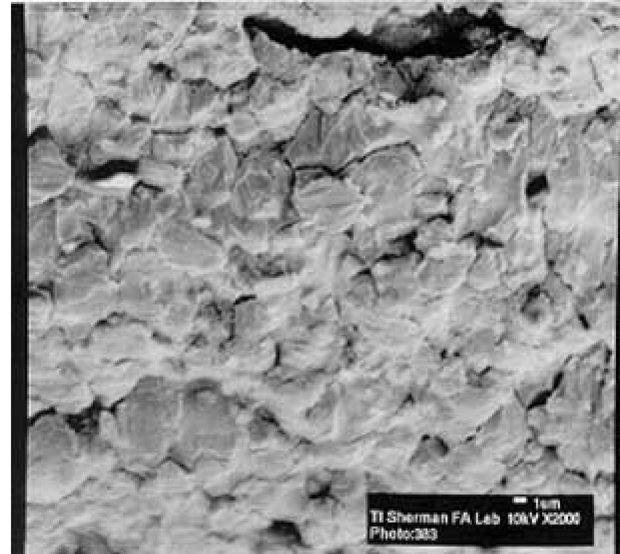

Figure 10. Grain Structure on Subcon F Tin-Bismuth SOT Units, 2000X Magnification

All grain structures noted for subcons A, C, and E units could be classified as large, well-polygonized grains. While grains were distinguishable on units from subcons B, D, and F, they did not appear as sharply defined. Also, plating thickness for all units from subcons A, C, and E were greater than the 8-μm deposit thickness referenced by Schetty.[16]

One theory for large grains suppressing whiskers is that stress, inherent or induced, in the Sn plate is distributed over a larger volume in coarse-grain deposits. This gives a lower stress per unit volume. Similarly, thicker Sn deposits spread the stress over a larger volume, particularly if the stress is associated with SnCu intermetallics close to the Sn/Cu interface and are not generally distributed in the Sn layer. As shown in the following discussion, the work presented here does not support these contentions. We saw whiskers on parts with Sn plating thickness >8 μm and on Sn deposits with large grains. These results point to the complexity of the Sn-whisker phenomenon and suggest that factors such as high internal stress can overcome the cited means to minimize the propensity to form whiskers.

Test Method

Sn-finished SOIC units from subcon A were chosen as the test vehicle for board mount and exposure to all four sets of conditions in Table 3.

Table 3. Whisker-Test Matrix for Subcon A

Run	Precondition (–40°C/+55°C, 24 hours)	Bias + Relative Humidity (RH)	Board Mounted	Bake Temp
1	Yes	No bias, 51°C bake only	No	51°C
2	Yes	Bias + 51°C/85% RH	Yes	51°C
3	No	No bias, 51°C bake only	No	51°C
4	No	Bias + 51°C/85% RH	Yes	51°C

The 51°C bake condition has been determined empirically by several researchers to favor Sn-whisker growth. The relative humidity, at 85%, is thought to favor whisker growth by facilitating the growth of Sn oxide on the surface of the Sn. TI included two cells with bias because this is an in-use condition. The applied bias was ~5 volts. Bias is not typically or widely used in whisker testing. In the test matrix shown in Table 3, the bias and RH parameters are linked.

The preconditioning for 24 hours was intended to drive Cu diffusion from the base metal into Sn-grain boundaries and promote formation of SnCu intermetallics. SnCu intermetallics are thought to cause Sn-whisker growth by creating compressive stresses in the Sn grains.

Board mounting allowed biasing the parts. The board-mount reflow process may relax internal stresses in the Sn layer that were present before board mount and, thus, reduces the tendency to produce whiskers in these deposits.

Packages from other subcons were not board mounted or biased. Exposure conditions for subcons B–D and subcon F are shown in Table 4 and are more typical of industry-wide test conditions.

Table 4. Whisker-Test Matrix for Subcons B–D and Subcon F

Run	Precondition (–40°C/+55°C, 24 hours)	Chamber Environment	Board Mounted	Bake Temp
1	Yes	51°C bake only	No	51°C
2	Yes	51°C/85% RH	No	51°C
3	No	51°C bake only	No	51°C
4	No	51°C/85% RH	No	51°C

NOTE: Subcon E units were exposed to 51°C bake conditions only.

Sample-Mounting Procedure

Units from subcon A (runs 2 and 4) were board mounted on printed wiring boards (PWBs). The solder paste was SnPb, and the reflow profile was typical for the SnPb soldering process, with peak temperature being ~220°C. One theory is that higher reflow temperatures (>235°C) used with Pb-free (SnAgCu) solder alloys may help relax the stress in the plating and reduce whiskering. Choice of SnPb paste and reflow temperature for this evaluation was based on the desire to exclude any impact of higher-reflow-temperature processes. If component subcons start producing Sn-finished components in volume, there is an undefined length of time when SnPb solders (and associated reflow temperatures) still will be in use by a high percentage of reflow operations. Thus, use of the SnPb solder process with peak temperature of ~220°C as a worst-case condition was justified. The PWBs used for board-mounted SOICs are shown in Figure 11.

Two leads on the 16-pin SOIC units from subcon A were scratched horizontally across the lateral lead surface prior to whisker-test exposure. Surface scratches are stress points in a Sn deposit.

Units from subcon A that were not board mounted (runs 1 and 3) were taped to a SEM inspection pedestal prior to exposure in the chambers. Units were mounted in both the dead-bug (feet up) and live-bug (feet down) positions as shown in Figure 12.

Figure 11. SOIC Unit From Subcon A Soldered to PWB

Figure 12. SOIC Units Glued to SEM Inspection Pedestal Prior to Test-Condition Exposure

Units from subcons B–F were not board mounted or glued to a SEM pedestal, but were placed in stainless-steel baskets and put inside the chambers for exposure.

Inspection Locations and Procedure

The inspection process had two goals, grain-size measurement and whisker detection. Magnification levels of 400X to 750X were adopted for the initial unit inspection, with magnification levels of 1000X to 7000X for grain-size measurement and whisker-site inspection. Additional magnification levels were used as needed, based on surface-finish and/or whisker-site conditions.

On the subcon A SOIC and subcon C TO-220 units, whiskers were detected at the lower levels of magnification during the inspection process. In contrast, whiskers detected on the subcon F SnBi SOT units were visible only at higher-magnification levels.

Units from each group in Table 1 were inspected for whisker growth at 0 hours and at exposure points noted below. Inspection locations for SOIC and SOT package styles are shown in Figures 13 and 14. Inspection points for live-bug samples (see Figure 13) included (1) top edge of lead at the shoulder bend (right or left side), (2) top center of lead at shoulder bend, (3) center of lateral lead-surface scratched area, and (4) bottom-left edge near underside of shoulder bend. Inspection points for dead-bug samples (see Figure 14) included (5) underside of lead foot at the tip and (6) underside of lead at start of shoulder bend.

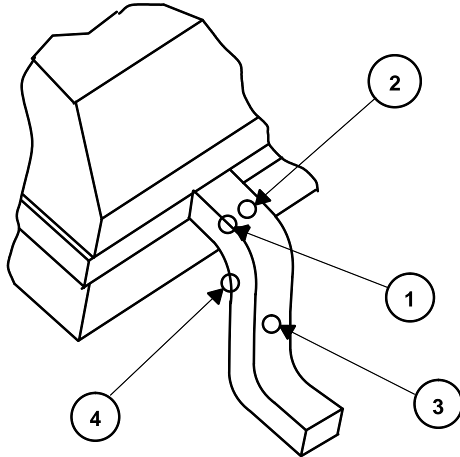

Figure 13. Inspection Locations for Live-Bug Gull-Wing Units

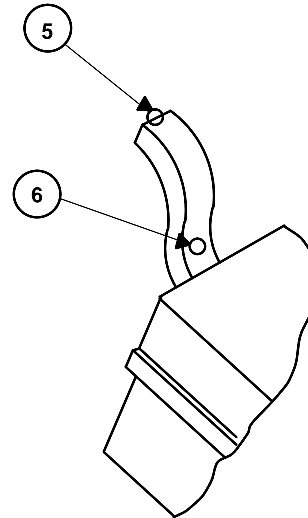

Figure 14. Inspection Locations for Dead-Bug Gull-Wing Units

Inspection locations for TO-220 samples (see Figure 15) included (7) top-left edge and side of lead, (8) top-right edge and side of lead, (9) bottom right edge and side of lead, and (10) bottom left edge and side of lead. For each of the four edges identified, the entire edge was inspected, not just a single point. Inspection locations for QFN packages (see Figure 16) included (11) edges of the exposed pad, (12) edges of left-side lead, and (13) edges of right-side lead.

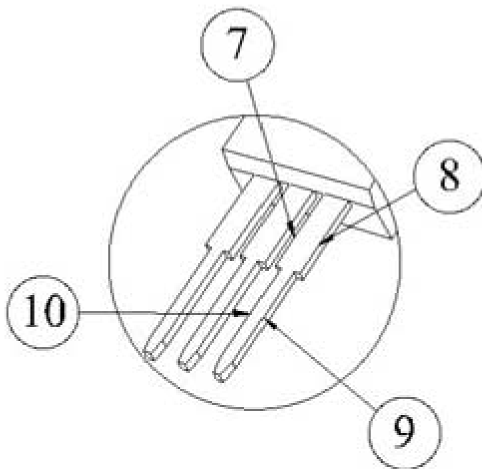

Figure 15. Inspection Locations for TO-220 Units

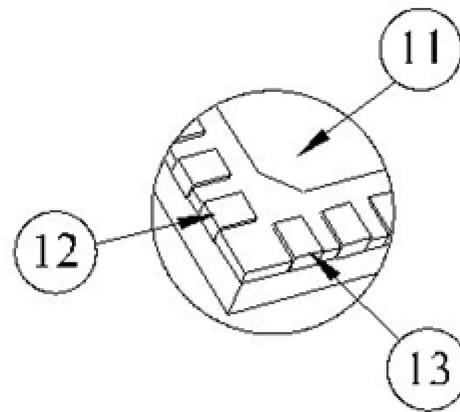

Figure 16. Inspection Locations for QFN Units

Locations identified in Figures 13–16 were the primary (minimum) whisker-inspection locations. Other points on the leads were inspected in some cases.

Inspection Results for Sn-Finished Units

Units were inspected before exposure to the conditions in Table 3 to establish a baseline for comparison. Units from each group then were exposed to the test conditions for extended times. Units from group A were pulled and inspected after 300-, 500-, 1000-, 2000-, and 3000-hours exposure. Table 5 summarizes the results of inspections on the subcon A units. Units from subcons B–D and F in Table 1 were inspected before exposure (0 hours) and after 3634-hours exposure to the stated conditions.

Inspection Results for Subcon A, Sn-Finished Units

Table 5 summarizes the SEM-inspection results for the Sn-finished SOIC units from assembly subcon A. No whiskers were noted on any of the subcon A units (runs 1–4) at inspection points prior to 1000-hours exposure.

Table 5. SEM Inspection Summary for Sn-Finished SOICs, Subcon A

Run	Inspection Point (hours)†					
	0	300	500	1000	2000	3000
1	0	0	0	0	0	0
2	0	0	0	X	X	X
3	0	0	0	0	0	0
4	0	0	0	0	X	X

† 0 = Sample was inspected and no whiskers were noted.
X = Whiskers were noted on a particular sample.

Generally, whiskers were seen on board-mounted units exposed to bias + 51°C/85% RH conditions. Whisker growth was seen after only 1000-hours (41 days) exposure on run-2 units and after 2000-hours (83 days) exposure on run-4 units. SEM photographs of subcon A units after 1000-hours exposure to run-4 conditions did not show any whiskers (see Figures 17 and 18).

Figure 17. Subcon A SOIC Unit at 450X, 1000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4 From Figure 13. No Whiskers Noted.

Figure 18. Subcon A SOIC Unit at 450X, 1000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 1. No Whiskers Noted.

However, when subcon A units were inspected after 2000-hours exposure to run-4 conditions, whiskers were evident (see Figures 19 and 20). The whiskers are noted as white lines or filaments emanating from the lead surface. Whisker lengths were measured in the SEM and are indicated in the photographs by a thin, dark line next to the whisker.

Figure 19. Subcon A SOIC Unit at 3000X, 2000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Whisker Length = 12.4 μm.

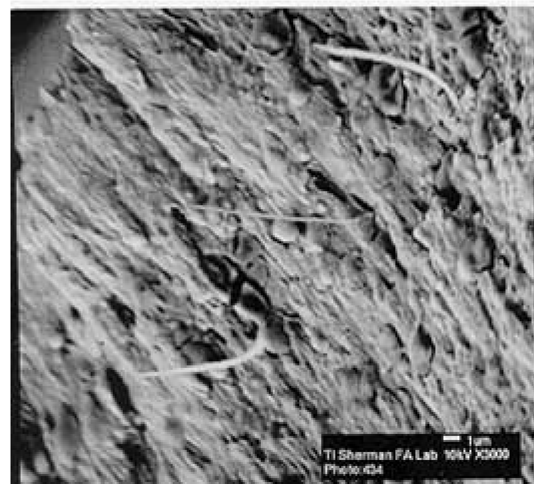

Figure 20. Subcon A SOIC Unit at 3000X, 2000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Multiple Whiskers Noted, With Length = 7.9–9.5 μm.

Multiple whiskers were noted across the lead surfaces of units exposed for 2000 hours. Figure 21 shows a 3000X magnification view of the 2000-hour exposure, with multiple whiskers approximately 1.6 μm long. Figure 22 indicates a whisker formation noted on 2000-hour exposure to run-4 conditions.

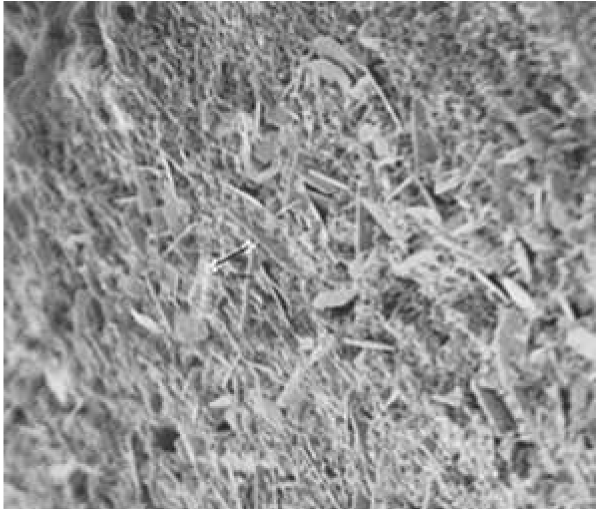

Figure 21. Subcon A SOIC Unit at 3000X, 2000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Multiple Whiskers Noted, Length of Measured Whisker = 1.6 μm.

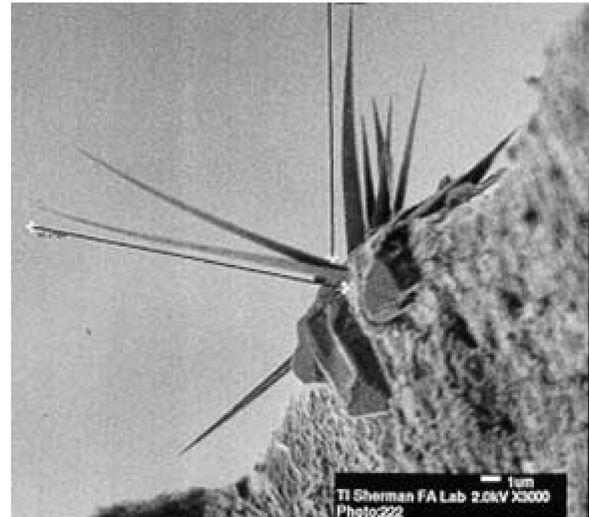

Figure 22. Subcon A SOIC Unit at 3000X, 2000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Whisker Length = 13.9–16.2 μm.

At 3000-hours exposure to run-4 conditions, whiskers again were seen (see Figures 23–26). Figure 23 shows whiskers noted on the side of a component lead. Figure 24 is a higher-magnification view of the whiskers noted in Figure 23. Whisker lengths measured in the range of 8–17.7 μm. Figures 25 and 26 show whiskers noted at 3000-hours exposure. Whisker lengths in these two cases were measured at 13–14 μm and 15–34 μm, respectively.

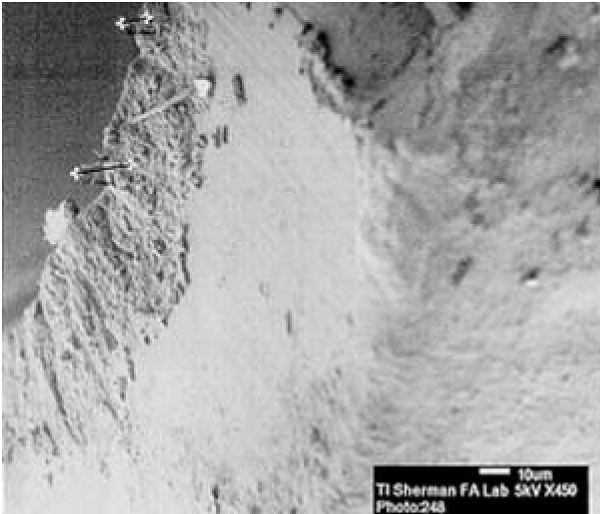

Figure 23. Subcon A SOIC Unit at 450X, 3000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Multiple Whiskers Noted, With Length = 8.0–17.7 µm.

Figure 24. Subcon A SOIC Unit at 1400X, 3000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Multiple Whiskers Noted, With Length = 8.0–17.7 µm.

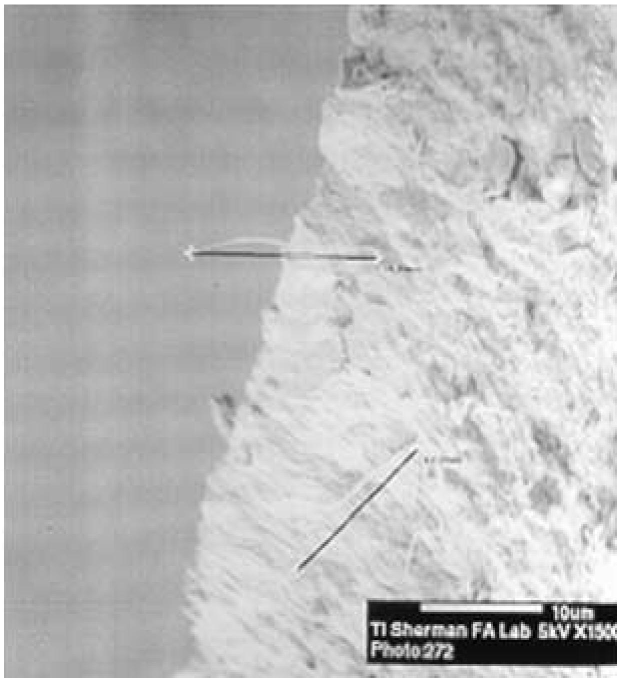

Figure 25. Subcon A SOIC Unit at 1500X, 3000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 4. Multiple Whiskers Noted, With Length = 13–14 µm.

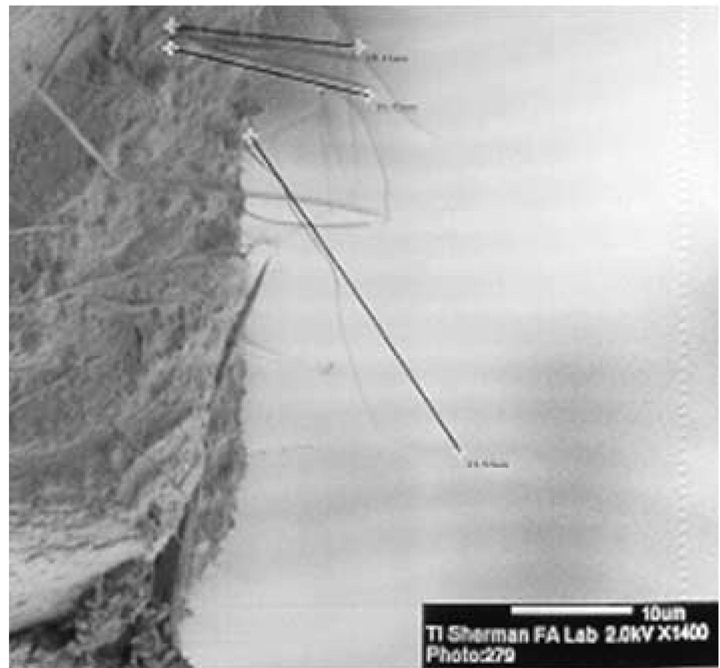

Figure 26. Subcon A SOIC Unit at 1500X, 3000-Hours Exposure to Run-4 Conditions (No Precondition, Bias + 51°C/85% RH). Inspection Location 3, Scratched Surface. Multiple Whiskers Noted, With Length = 15–34 µm.

Inspection Results for Subcons B–D, Sn-Finished Units

Units in subcons B, C, D, and F were inspected at 0-hours exposure and after 3634-hours exposure to conditions shown in Table 4.

Inspection of subcon B units (see Figures 27 and 28) noted no whiskers after 3634-hours exposure to the test conditions. Figure 27 shows lead appearance after exposure to precondition + 51°C/85% RH, with no bias. Figure 28 shows lead appearance after exposure to 51°C/85% RH, no precondition or bias. No whiskers were noted on these units.

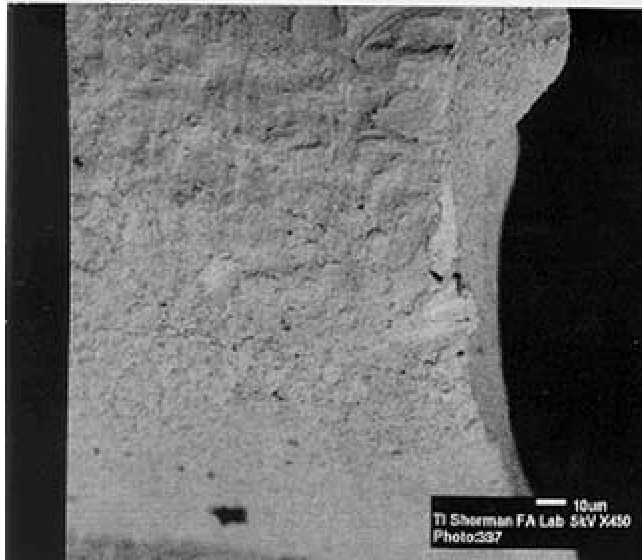

Figure 27. Subcon B SOT Unit at 450X, 3634-Hours Exposure to Precondition + 51°C/85% RH, Unbiased. Inspection Location 1, Right Side. No Whiskers Noted.

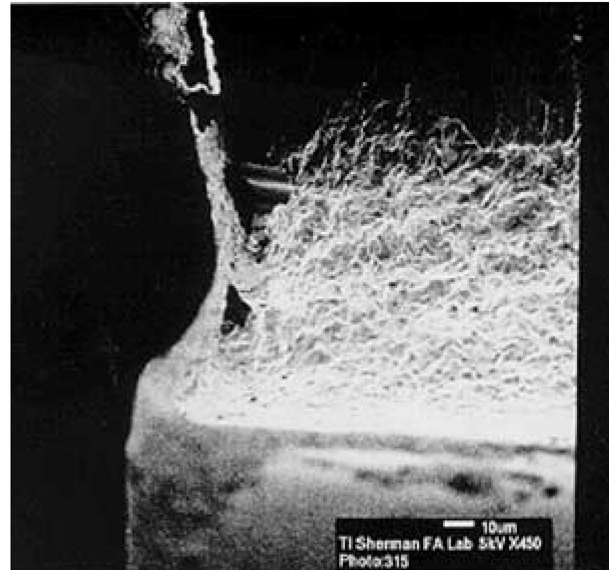

Figure 28. Subcon B SOT Unit at 450X, 3634-Hours Exposure to 51°C/85% RH, No Precondition, Unbiased. Inspection Location 1, Right Side. No Whiskers Noted.

Inspection of subcon C units (see Figures 29–34) after 3634-hours exposure to the test conditions noted whiskers of varying lengths. Figures 29 and 30 show whisker growth on units exposed to precondition + 51°C/85% RH for 3634 hours, with no bias applied.

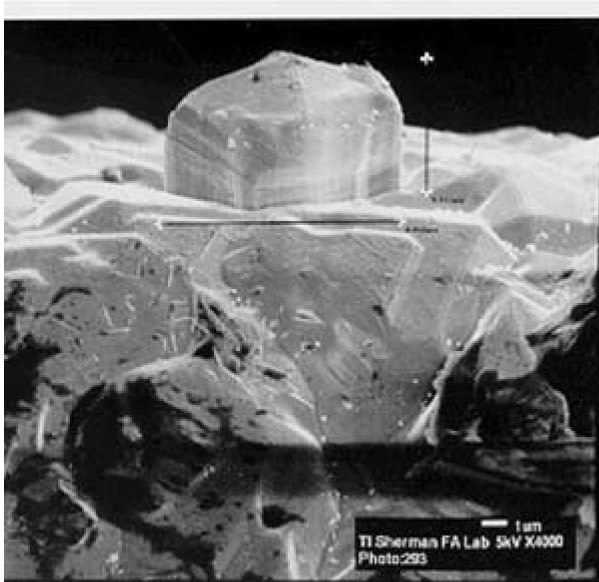

Figure 29. Subcon C TO-220 Unit at 4000X, 3634-Hours Exposure to Precondition + 51°C/85% RH, Unbiased. Inspection Location 8, Figure 15. Whisker Length = 5.1 μm.

Figure 30. Subcon C TO-220 Unit at 7500X, 3634-Hours Exposure to Precondition + 51°C/85% RH, Unbiased. Inspection Location 7, Right Side. Whisker Length = 9.3 μm.

Figures 31–32 show whisker growth on units exposed to 51°C/85% RH for 3624 hours, with no preconditioning and no bias applied.

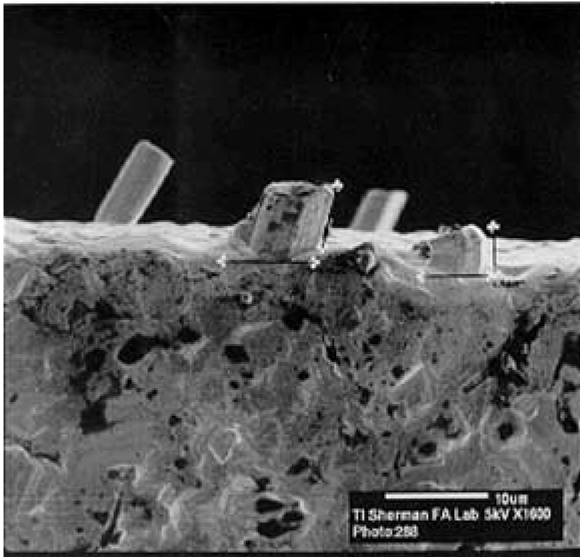

Figure 31. Subcon C TO-220 Unit at 1600X, 3634-Hours Exposure to 51°C/85% RH, No Precondition, Unbiased. Inspection Location 9. Multiple Whiskers Noted, With Length = 4.6–6.2 µm.

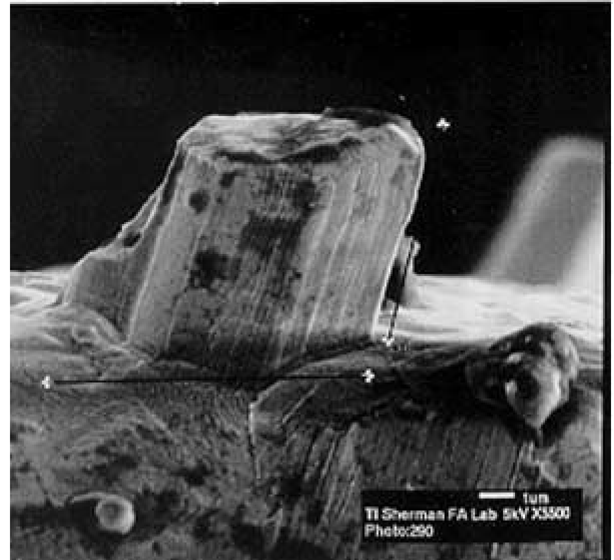

Figure 32. Close-Up of Whisker Noted on Subcon C TO-220 Unit at 1600X, 3634-Hours Exposure to 51°C/85% RH, No Precondition, Unbiased. Inspection Location 9. Whisker Length = 6.2 µm.

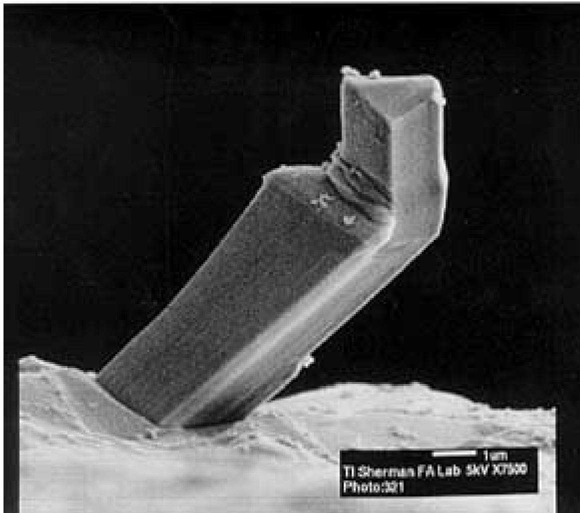

Figure 33. Subcon C TO-220 Unit at 7500X, 3634-Hours Exposure to Precondition + 51°C/85% RH, Unbiased. Inspection Location 9. Whisker Length = 7.7 µm.

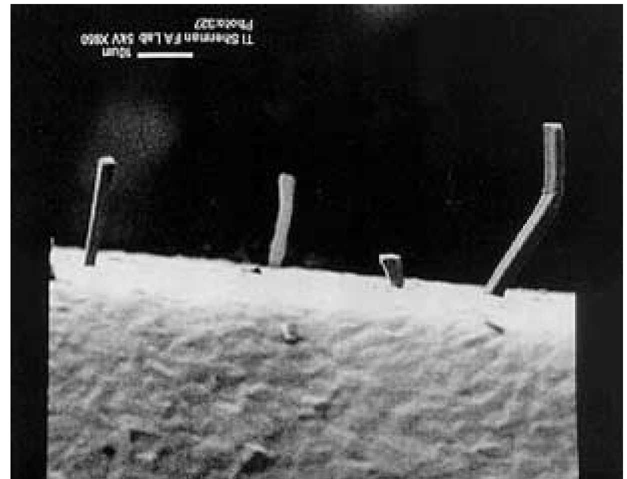

Figure 34. Subcon C TO-220 Unit at 950X, 3634-Hours Exposure to Precondition + 51°C/85% RH, Unbiased. Inspection Location 7. Multiple Whiskers Noted, With Length 6.1–32 µm.

Additionally, units were pulled from the subcon C group that had been stored on a shelf for nine months, with no exposure to whisker-test conditions. Upon inspection, these units showed initiation of whisker growth. This is significant because the units had not been exposed to whisker-test conditions, only shelf storage. Examples of the whisker growth on the shelf-stored units are shown in Figures 35–38.

Figure 35. Subcon C TO-220 Unit at 7500X, After 9-Months Shelf Storage, No Exposure to Whisker-Test Conditions. Inspection Location 8. Whiskers Are 8.8 μm Wide × 6.9 μm Long.

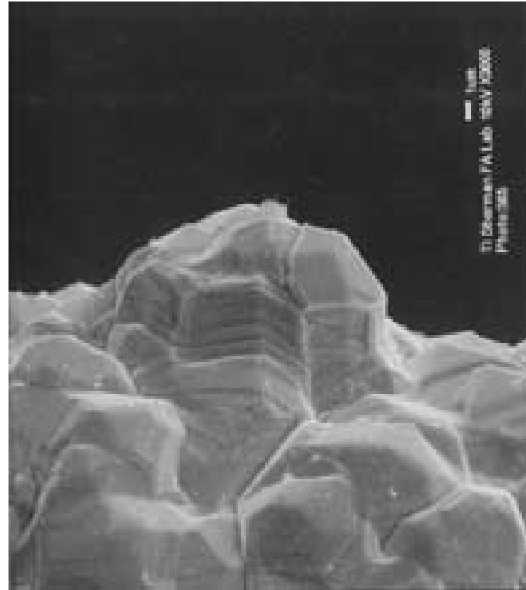

Figure 36. Subcon C TO-220 Unit at 3000X, After 9-Months Shelf Storage, No Exposure to Whisker-Test Conditions. Inspection Location 8. Whiskers Are 14.6 μm Wide × 9.4 μm Long.

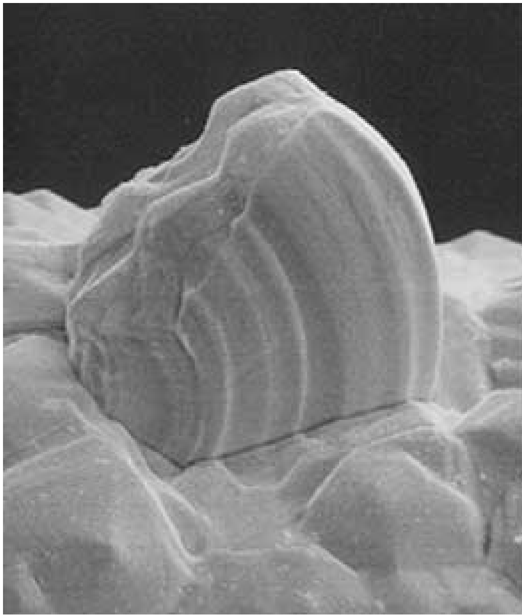

Figure 37. Subcon C TO-220 Unit at 3700X, After 9-Months Shelf Storage, No Exposure to Whisker-Test Conditions. Inspection Location 9. Whiskers Are 14.2 µm Wide × 14.5 µm Long.

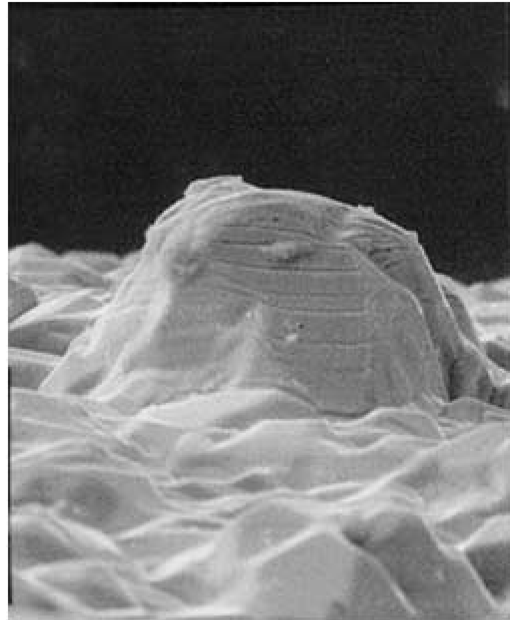

Figure 38. Subcon C TO-220 Unit at 3300X, After 9-Months Shelf Storage, No Exposure to Whisker-Test Conditions. Inspection Location 10. Whiskers Are 20.3 µm Wide × 10.1 µm Long.

Inspection of subcon D units (see Figures 39 and 40) noted no whiskers after 3634-hours exposure to the test conditions. Figure 39 shows lead appearance after exposure to precondition + 51°C/85% RH, with no bias. Figure 40 shows lead appearance after exposure to 51°C/85% RH, with no preconditioning or bias. No whiskers were noted on these units.

Figure 39. Subcon D SOT Unit at 600X, 3634-Hours Exposure to 51°C/85% RH, Unbiased. Inspection Location 4. No Whiskers Noted.

Figure 40. Subcon D SOT Unit at 450X, 3634-Hours Exposure to 51°C/85% RH, Unbiased. Inspection Location 1. No Whiskers Noted.

Units in subcon E were inspected at 0-hours exposure and after 4000-hours exposure to 51°C bake condition. No whiskers were noted on these units.

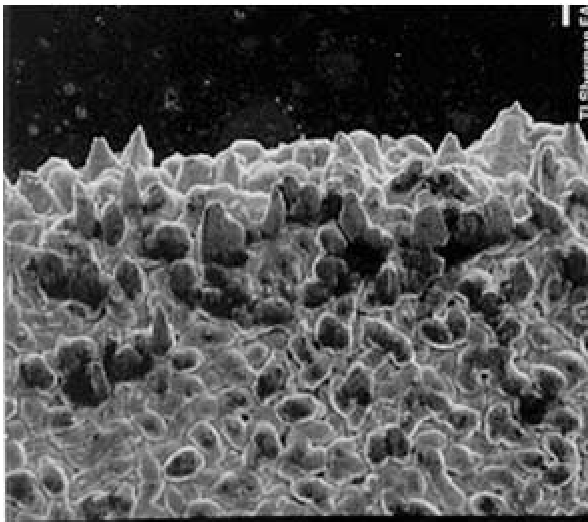

Figure 41. Subcon E QFN Unit at 1000X, 4000-Hours Exposure to 51°C Bake, Unbiased. Inspection Location 13. No Whiskers Noted.

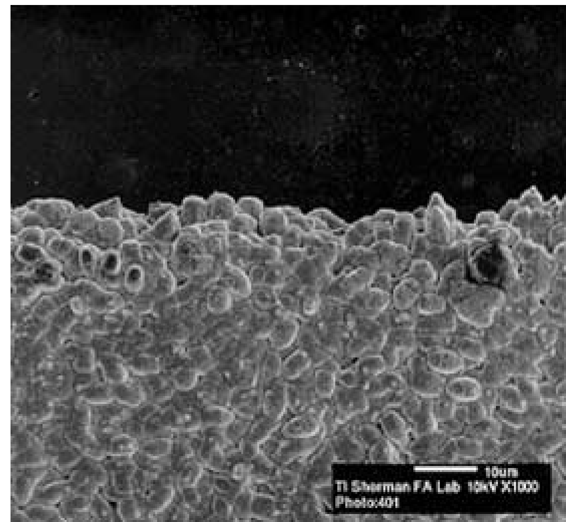

Figure 42. Subcon E QFN Unit at 1000X, 4000 Hours Exposure to 51°C Bake, Unbiased. Inspection Location 12. No Whiskers Noted.

Inspection Results for SnBi-Finished Units

Units from one subcon (subcon F) used a SnBi finish on an SOT package. SnBi-finished SOT units were not board mounted or biased, but were exposed to the conditions in Table 3. Inspection was performed prior to exposure (0 hours) and after 3634-hours exposure to the conditions in Table 4. Units were not pulled at intermediate inspection points. In addition to inspection locations identified in Figures 13 and 14, the SnBi SOT packages also were inspected along the foot area of the lead.

Figure 43. Subcon F SnBi-Finished SOT Package After 3634-Hours Exposure to 51°C/85% RH. Inspection Location 1, Right Side. Whisker Length = 0.4–0.6 μm.

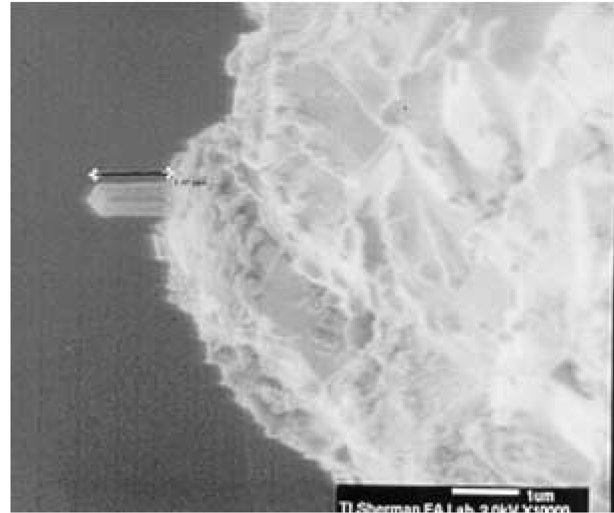

Figure 44. Subcon F SnBi-Finished SOT Package After 3634-Hours Exposure to 51°C/85% RH. Inspection Location 1, Left Side. Whisker Length = 1.1 μm.

Figure 45. Subcon F SnBi-Finished SOT Package After 3634-Hours Exposure to 51°C/85% RH. Inspection Location Left Edge, Foot Area. Multiple Whiskers Noted, Length = 5.7–6.5 μm.

Figure 46. Subcon F SnBi-Finished SOT Package After 3634-Hours Exposure to 51°C/85% RH. Inspection Location Left Edge, Foot Area. Closeup of Whisker, Length = 6.5 μm.

Summary of Results for Subcons B–F

Table 6 summarizes the SEM inspection results for units from subcons B–F.

For the TO-220 units from subcon C, whiskers were noted on units that were shelf stored for nine months, with no exposure to the test conditions.

Table 6. SEM Inspection Summary for Units From Subcons B–F

		Inspection Point†	
Subcon/Package	Condition	0 hours	3634 hours
B/SOT	1	0	–
	2		0
	3		–
	4		0
C/TO-220	1	X	–
	2		X
	3		–
	4		X
D/SOT	1	0	–
	2		–
	3		–
	4		0
E/QFN	51°C bake	0	0 (4000 hrs)
F/SOT	1	0	–
	2		–
	3		–
	4		X

† 0 = No whiskers noted
X = Whiskers noted on a particular sample
– = Sample was not inspected

Observations

There appears to be two distinctly different whisker types: a cylindrical base with tapered extensions that can be very fine, or thicker and more needlelike in shape. This type was evident on subcon A SOIC devices. The second whisker type, observed on subcon C/TO-220 and subcon F SnBi SOT units, was a much more distinctive, crystal-like structure, from the base through the entire whisker length.

In addition, the plated surface on the subcon C/TO-220 units showed the same distinct pattern as the shape of the top of the whisker. When viewing the flat plated surfaces, shapes similar to the lateral surfaces of whiskers also could be seen.

Summary of Results

Whisker-test conditions were defined for this testing after review of industry experimentation in progress (NEMI).[12] Whisker growth was seen on the subcon A Sn-finished, board-mounted SOIC units at 1000 hours, and beyond, after exposure to bias + 51°C/85% RH. Whiskers were noted both with and without exposure to preconditioning (–40°C/+55°C, 24 hours). Whisker length ranged from <2 μm up to 34 μm.

Sn-finished SOT packages from subcon B and subcon D did not exhibit whisker growth when exposed to 51°C bake or 51°C/85% RH conditions, either with or without preconditioning (–40°C/+55°C, 24 hours). These units were not board mounted or biased.

Sn-finished TO-220 packages from subcon C exhibited whisker growth after exposure to 3624 hours of 51°C/85% RH conditions, both with and without preconditioning (–40°C/+55°C, 24 hours). These units were not board mounted or biased. Also, it is significant that the TO-220 leads were not formed during assembly. Forming of the leads induces stress in the bend areas of the leads; therefore, the TO-220 leads did not have any mechanical stress from forming. Whisker length ranged from 4.6 µm to 32 µm. Sn-finished TO-220 units also were pulled from shelf storage after nine months and inspected. Units that had not been exposed to any whisker-test conditions, only shelf storage, also exhibited whisker growth. Maximum whisker length measured was 14.5 µm.

Sn-finished QFN packages from subcon E did not exhibit whisker growth when exposed to 51°C bake for 4000 hours. These units were not board mounted or biased.

SnBi-finished SOT packages from subcon F exhibited whisker growth after 3634-hours exposure to 51°C/85% RH conditions. Multiple whiskers were noted, ranging in length from 0.4 µm to 6.5 µm.

Conclusions

This work shows some of the risks associated with matte Sn as a lead finish—sometimes it produces whiskers and sometimes it does not. Both matte Sn and Sn/Bi finishes grew whiskers on the logic product packages tested. Whiskers were grown on biased and unbiased devices and on formed and unformed leads (unformed leads largely discount mechanically induced stress in the Sn). Whiskers also were seen on units that were shelf stored only. All of the Sn deposits tested would be classified as matte Sn, yet there were some that showed no whiskers, and most showed some whiskers. Matte Sn commonly is thought to be least susceptible to Sn whiskering. What is not taken into account is the level of stress initially in the Sn deposit. We did not measure the stress level in the Sn as deposited. This is a difficult measurement to perform on parts as received. The disparity in performance of these matte Sn deposits points to the risk of using, and the difficulty in controlling, matte Sn.

The work also lends credence to the notion that there are likely a multiplicity of mechanisms operating to form Sn whiskers, and that these mechanisms can work individually or in concert. A multiplicity of mechanisms complicates schemes intended to minimize Sn whiskers.

Finally, what is unique about this work is that it looks at biased units in parallel with units that were unbiased, and both were subjected to temperature/humidity storage conditions. Biasing most closely resembles the in-use condition for ICs. Industry-wide work on Sn-whisker testing has not embraced an electrically biased test condition. The growth mechanism for whiskers grown under bias conditions likely is not the same mechanism as that for classical whiskers grown with no bias. Such Sn whiskers, grown with or without bias, have the potential to pose long-term reliability risks for electronic devices built using ICs with matte Sn-finished leads.

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