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Ultra Low Power Energy Harvesting and Power Management IC (PMIC) Design

APEC 2017 - Energy Harvesting Industry Session

Séamus O'Driscoll, 30th March 2017

APEC

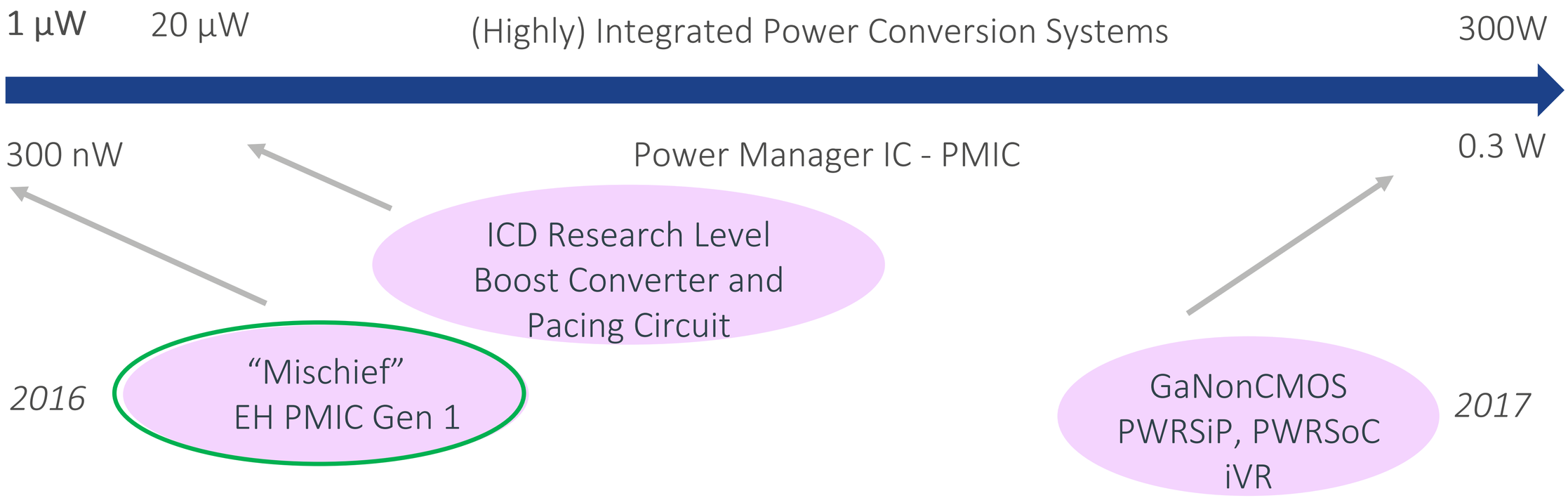
UCC University College Cork, Ireland Coláiste na hOllscoile Corcaigh
Ireland's European Structural and Investment Funds Programmes 2014-2020 Co-funded by the Irish Government and the European Union
European Union European Regional Development Fund

Power Conversion & PMIC at Tyndall:

Smart Sensor Power
Ambient Energy Harvesting
Implantable Power

Edge, Gateway Devices
Smart Phones
AC Adapters

Blade Server Processor
Base Station
UPS, PV Inverter



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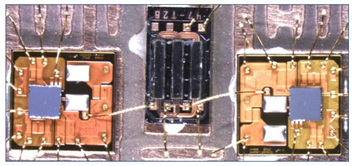
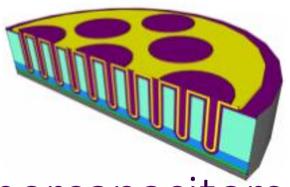
Research Groups contributing to Energy Harvesting & PMIC Development

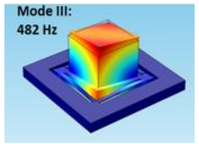
ICT4EE Systems
(Energy Efficiency)

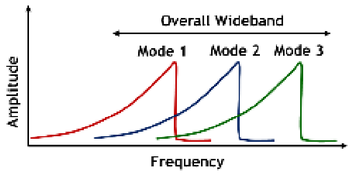


PWRSiP, PWRSoC



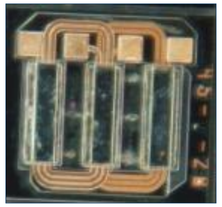
Solid State Supercapacitors





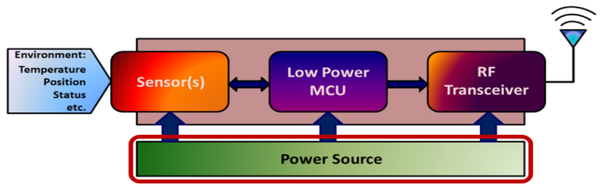
Vibrational Energy Harvester

Materials
Structures
Magnetics on Silicon



Solid State
Energy Cells

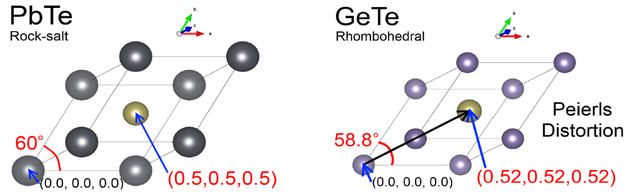
MCCI
Microelectronic Circuits Centre Ireland



WSN

Material Model & Synthesis

Mix materials with slightly different atomic arrangements:



Integrated Power Systems and PMICs

Integrated Systems Design

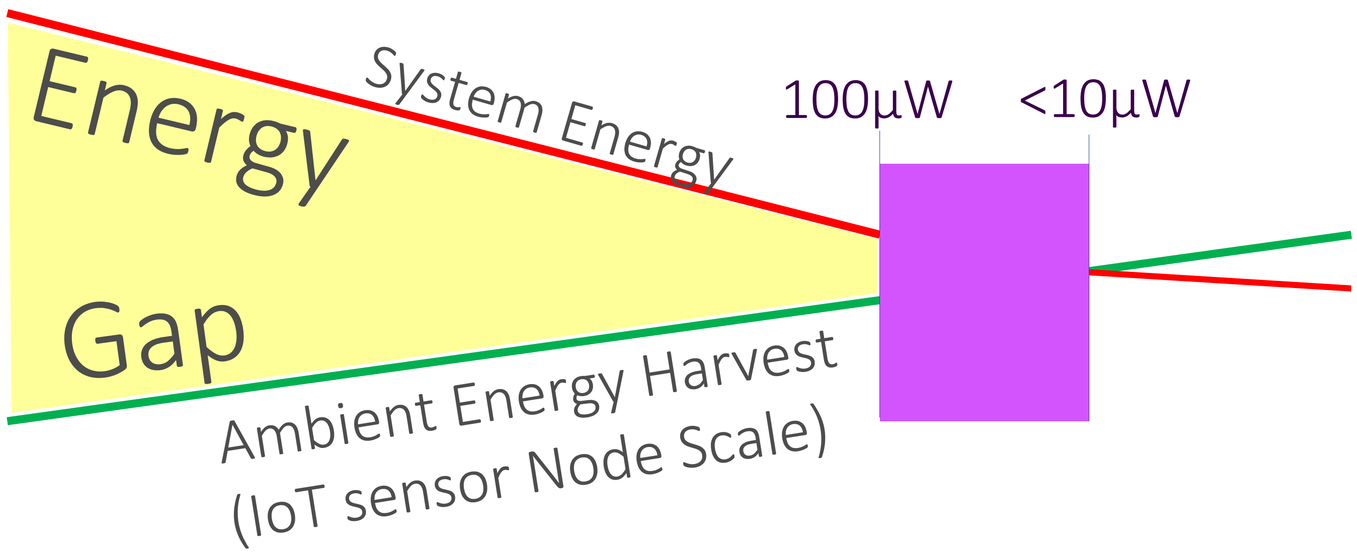
UCC University College Cork, Ireland Coláiste na hOllscoile Corcaigh
Ireland's European Structural and Investment Funds Programmes 2014-2020 Co-funded by the Irish Government and the European Union
European Union
European Regional Development Fund

Ultra Low Power (ULP) PMICs

Low Bandwidth and Low Average Data ***"battery-less"*** (maintenance-free) systems

Or

Battery Life extension to 25+ years



Power and Energy Data points

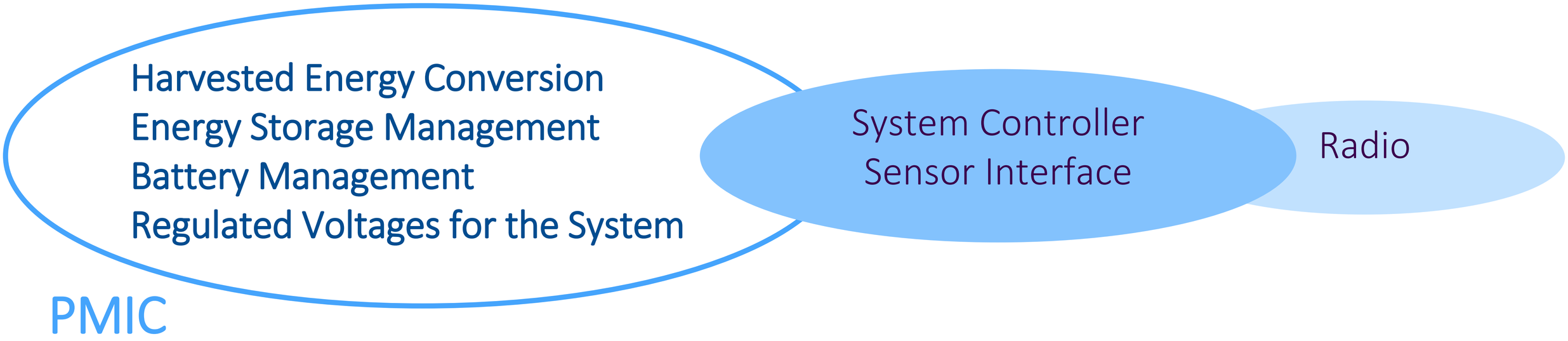
Short-range (BLE) Wireless SoC
Wearables - 1µA Idle with 32kHz & RTC
~2.4uW average for radio for heart rate profile – 4bytes/s for 1h/day

Ocular (retina) implant system @ IDD=50nA

Hearing Aid DSP - <100uA/MIPs

SOA Technology Solid State Storage on 1.5mm X 1.5mm die will provide ~15µW.h (10µm layer)

Control Silicon - ULP Wireless System Node



There are generally two types of PMIC

A. Switch Mode (15uW and η% = 75-90+% (@3V3 Bat)
B. Switched Energy Management ICs (> ~1uW)

“Mischief” is an advanced Next Generation PMIC development program

Ambient Energy Harvesting

- PV **(DC)** and with fractional open circuit voltage **(FOCV)** sensing, the maximum power point (**MPPT)** is generally quite easily achieved.
  - MPPT point a little less than VBAT, boost is very efficient
  - The Switched Energy Manager is a good choice for single voltage, MPPT=VBAT.

- TEG **(DC)** usually generates a low DC voltage.
  - Some PMIC solutions start at 10mV but require a **coupled inductor resonator** with high Q – many examples such as Linear Technologies, Enocean. The wound magnetic (N=1:100) may be a high proportion of PMIC area.
  - Research Level: Fine geometry CMOS Gated Ring Clocks + Tx Coupled Oscillators + Charge Pump Multipliers – 85mV

- Vibration Energy Harvesting (VEH) **(AC)**
  - Random, variable frequency or impact driven mechanical resonators at fixed frequency
  - Piezo/Electret – High Voltage (to 10 - 100VAC), Low Current – Research Level: Active Rectifiers, Low Loss Charge Extraction
  - Electromagnetic Transduction – Lower Voltage, Higher Current – Research Level: Power Factor Improvement

Survey of Commercially Available ULP EH PMICs

(June 2016)

Marketplace EH PMIC	IQ (Regulation) (nA)	SPI/ I2C Interface and digital control benefits	MPPT	Topology	Low Output Voltages	ULP Efficiency (%) (1V-2V, 10uA)	Current Control - Battery Chemistry Charge Current Optimisation	Cold Start Power (uW)
#1	320	No	Yes	Boost	No	82	No	16
#2	41000	No	Yes	Boost	No (3V+)	na	No	
#3	300	No	Yes	Cascade Boost, Buck+LDO	Yes	Low (<20)	No	11
#4	2000	No	Yes	Boost, Buck-Boost, LDO	Yes	Low (<20)	No	
#5	330	No	Yes	Boost	No (2V+)	77	No	15
#6	250	No	No	Step Down Switched Energy	Yes (1.1V+)	Highly sensitive to OP point	No	1.2
#7	100	No	No	Step Down Switched Energy	No (~3V)	na	No	<1
Mischief	160	Yes	Yes	QR Buck, Boost	0.9V	85	Yes	<1

“Mischief” Research Test Chip/Platform
Energy harvesting PMIC Goals

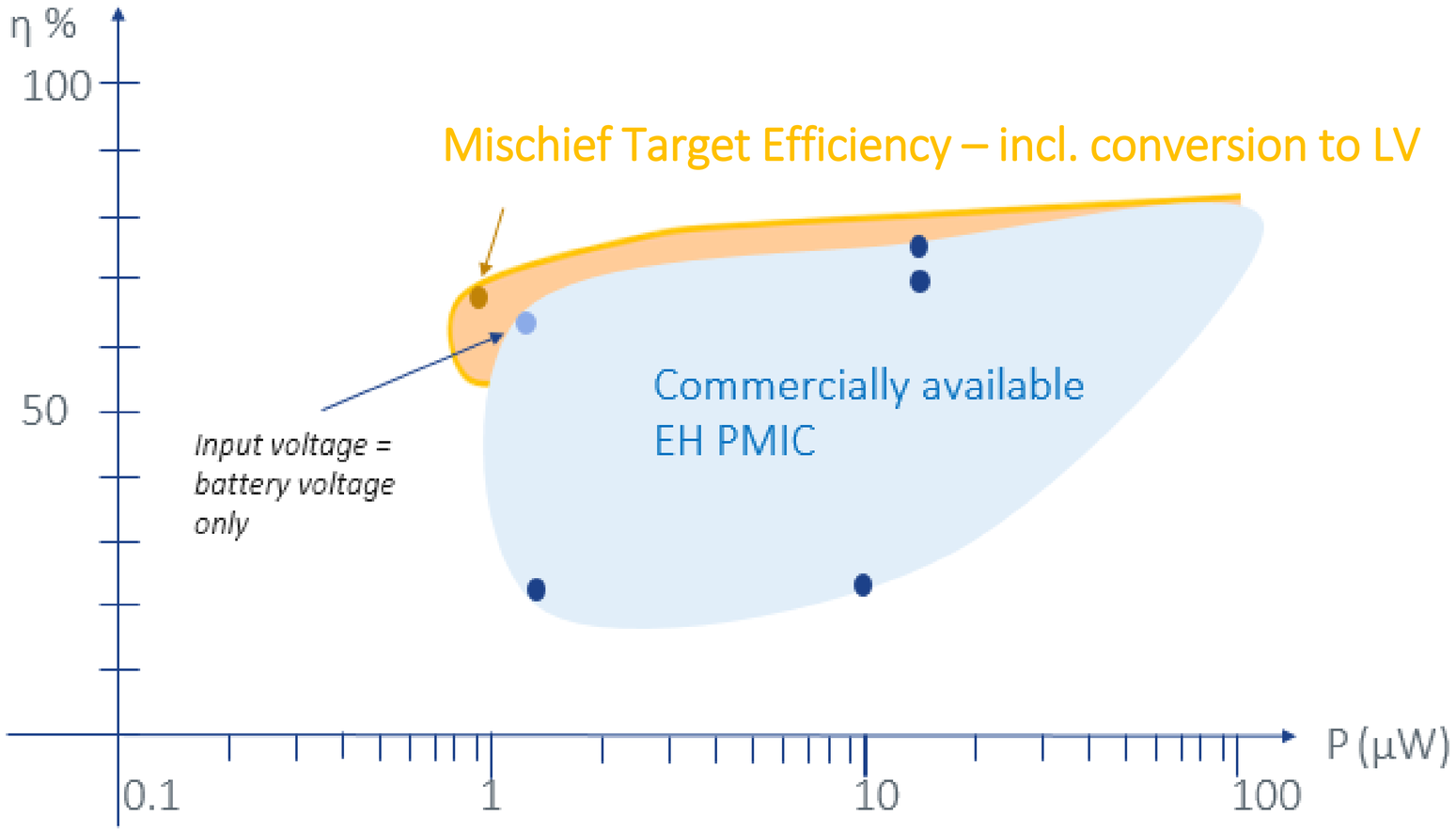
Highest efficiency switch-mode, energy harvesting PMIC, measured @ 10 µW point
Cold-start and operation over ~1µW to 200mW

Lowest quiescent current (I_Q) in low power regulation mode, ~160nA for SMPS

Highest **end-to-end system** efficiency (HV and LV)

Technology Platform for development of:
Next Gen control & features
substantially increased power transfer - VEH

Highest Efficiency & Next Gen Capability



4 Switch
Quasi-Resonant
Buck-Boost topology

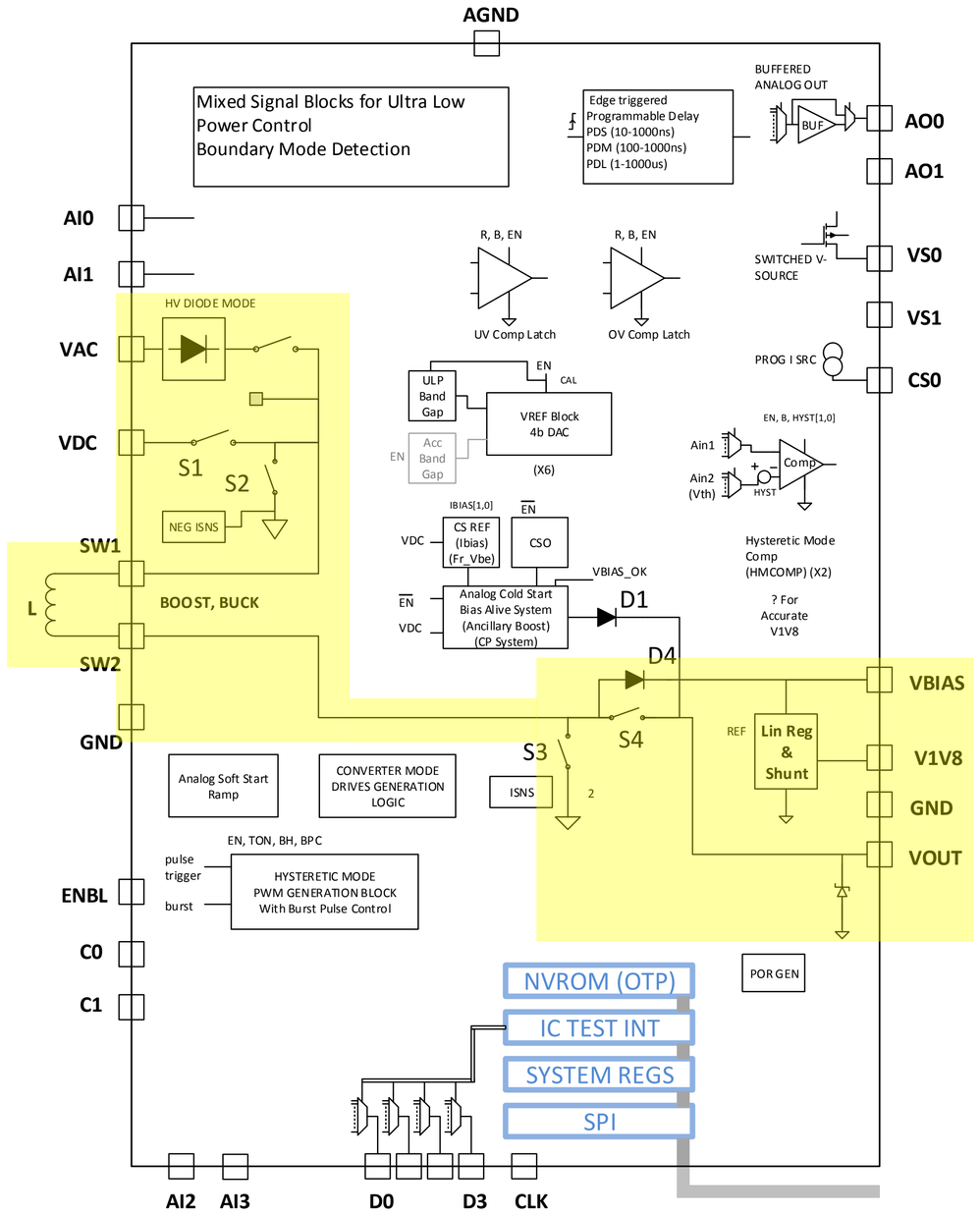
After extensive survey of best available parts

Highest end-end efficiency over 1uW upwards with SMPS

Focus should be on all System Voltages

Static I_Q matters, Low BW Control

Mischief Research Test IC Block Diagram



- 4-S Buck and Boost Power Path for Efficient Energy Storage and Lower System Voltage such as 1V8
- Modular Flexible Mixed Signal blocks
- Asynchronous Digital and Analog
- Dynamic Power/Speed Control
- Fast Start and Stop Blocks – Efficient Duty Cycling

A platform for on-going development – Microprocessor or FPGA

Preliminary Drawing - design is still underway

Requirements - “Datasheet”
helps focus our Targeted Research

Mischief ENERGY HARVESTING PMIC
IC
Short Form Datasheet

UNIQUE FEATURES

- TEG, VEH, PV Energy Source Capability
- Designed primarily for ***battery-less*** *Smart Sensor Nodes*
- Input Operation from 200mV
- Tri-Modal 4 Switch Buck- Boost, with automatic mode transitioning.
  - Buck Mode
  - Buck-Boost Mode
  - Boost Mode
- 90% Efficiency for 10uW to 100mW
- 75% Efficiency for 1uW to 10uW
- 100nA Quiescent Current in Low Power (LP) Regulation Mode
- Supercapacitor Energy Storage Management with E_GOOD status
- I2C Communications Interface
- Output Overload threshold set point
- VEH Synchronous Rectifier (Suitable for Tyndall VEH technologies) and Boost Mode Power Factor Improvement
- Condition Monitoring for Energy Source and Storage
- Burst Mode Control to maximize efficiency with optimised burst energy packet design.
- 1st Valley Quasi Resonant Switching

FEATURES

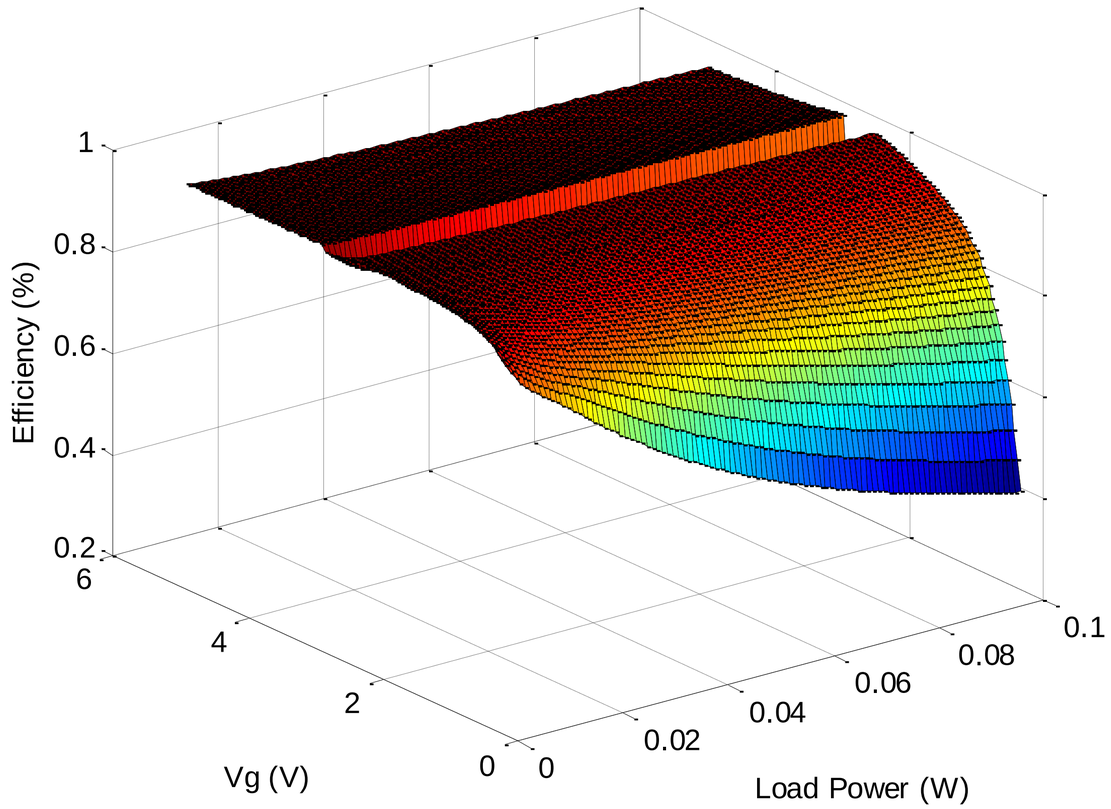
- Programmable Output Voltage Monitor
- Timed Switching Disable for Communications
- Output in Regulation, VOUT_GOOD
- MPPT Set Point Adjust
- IC Energy Management Block automatically disables switching during intervals of inadequate ambient energy

TYPICAL APPLICATIONS

- Battery-less Smart Sensing Wireless Nodes
- Indoor PV cell energy harvesting
- TEG energy harvesting
- VEH energy harvesting
- Portable and wearable devices with energy harvesting
- IP blocks for Implantable Devices

4 Switch Buck-Boost used in Buck or Boost Mode

f=120kHz, V=2.8, L=45uH



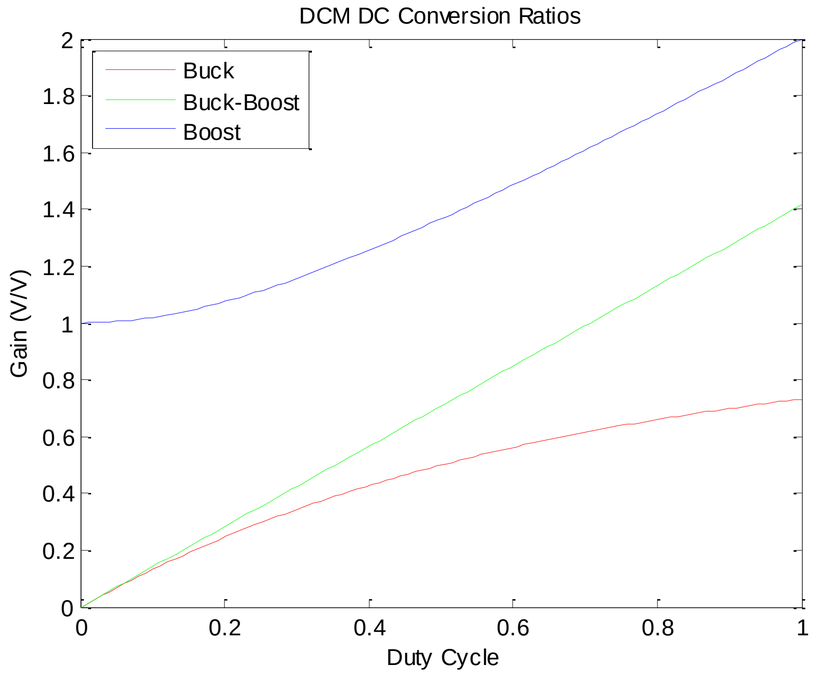
Conduction Loss Plot

Buck Boost Mode may only be used for a narrow band to cater for the Steady State Duty transition between Buck and Boost Modes.

QR mode switching losses are to be included

Steady State Gains

Consider as transition through modes and there are various options.



Silicon Fab Process

0.18 µm Process Family:
> XP018
0.18 Micron CMOS Analog Mixed-Signal Process Technology

X-FAB MIXED-SIGNAL FOUNDRY EXPERTS

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X-FAB 180nm CMOS Process with XP power option

Input and output voltages range to ~4V and are implemented with ne5 and pe5 nmos/pmos

Has 32V HVMOS Asymmetrical low RON MOSFETs – will be suitable for piezo/electret voltages

Appropriate components

Isolation wells, sandwich capacitors, high resistivity poly resistors, thick top metal, qualifications, to 175C

The ideal fab process should offer a migrating path to highly featured MEMs processes

- BEOL on chip magnetic material/high density supercapacitors/electrochemical storage/piezo/MEMs/TEG

Fine geometry CMOS would allow start-up voltages ~100mV. 180nm CMOS come alive circuits are ~375mV, best case

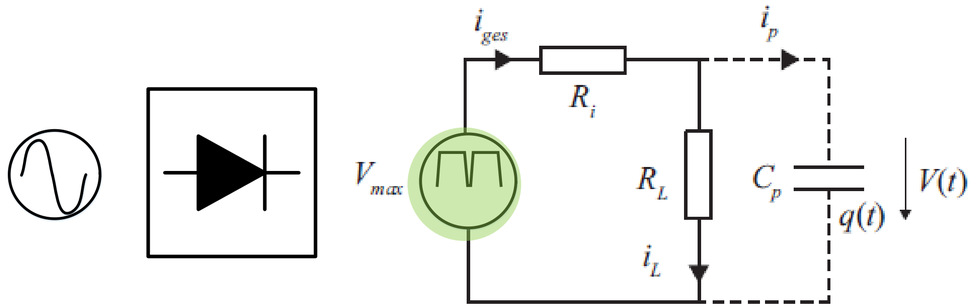
Enabling High Value, Novel, Next Generation Features

Digitised outer loop power/current set points for MPPT will enable features such as **performance monitoring of source and storage**

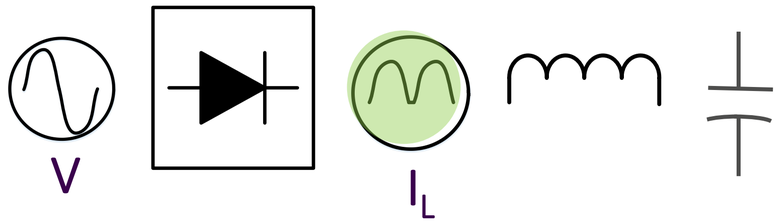
Charge profile tuning to suit **emerging battery chemistries**

VEH is AC and will be by Active Rectifier & DC-DC/Synchronous Charge Extraction or Power Factor Improvement

Piezoelectric, electret devices tend to be current source in nature
Electromagnetic transduction tend to be voltage source in nature



Active Rectifier



Boost to HV "Bulk" Storage Capacitor

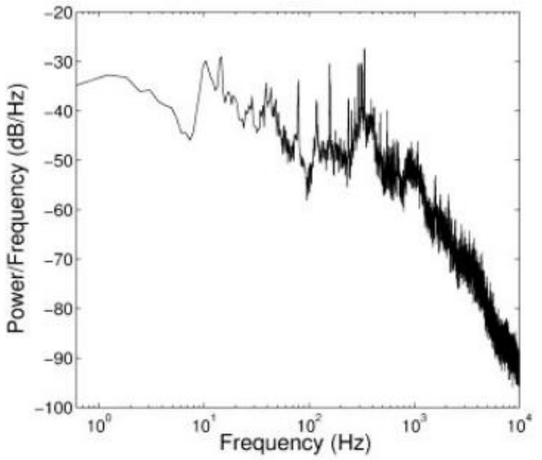
Power Factor Improvement

Non-Linear Stimuli to increase Harvester Utilisation Electromagnetic Transducer (EMT) VEH

AC MPPT involves Resistive and Reactive Impedance Matching

Mischief injection stimuli will increase power transfer across the VEH frequency spectrum

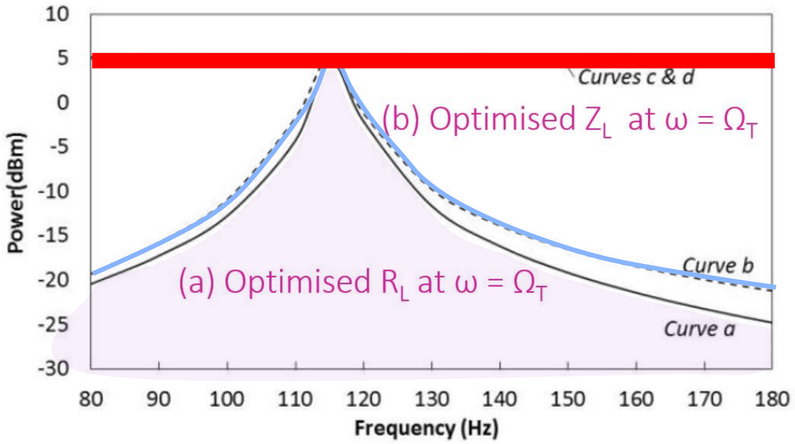
VEH Transducer on Railcar



'Surfing the high energy branch of nonlinear energy harvesters', D. Mallick, S. Roy, Phys. Rev. Lett., week ending 4 NOVEMBER 2016, claim **32 X**

Adjacent research activity[1] on "Bias-Flip" claims **8 X** increase in delivered power away at Ω_M

(c) Optimised R_L and Z_L
(d) Bias Flip alternative technique



[1] Bias-Flip Technique for Frequency Tuning of Piezo-Electric Energy Harvesting Devices,
Journal of Low Power Electronics and Applications, 2013, Zhao, Jianying; Ramadass, Yogesh; Lang, Jeffrey; Ma, Jianguo; Buss, Dennis

Mechanical and Electrical Co-Design VEH

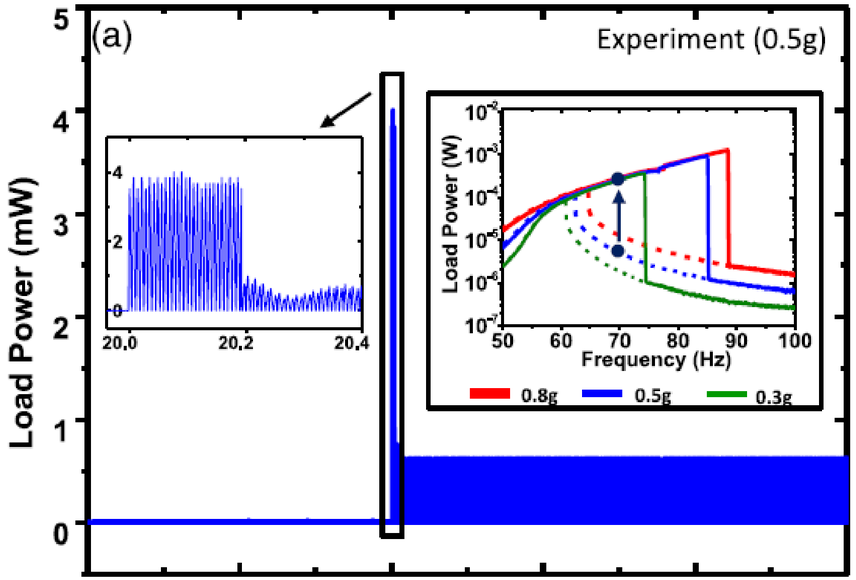
- **Mechanical Non-Linearities** added in transducer design +
- **Non-Linear Electrical Stimuli** to maintain high energy branch resonances
-

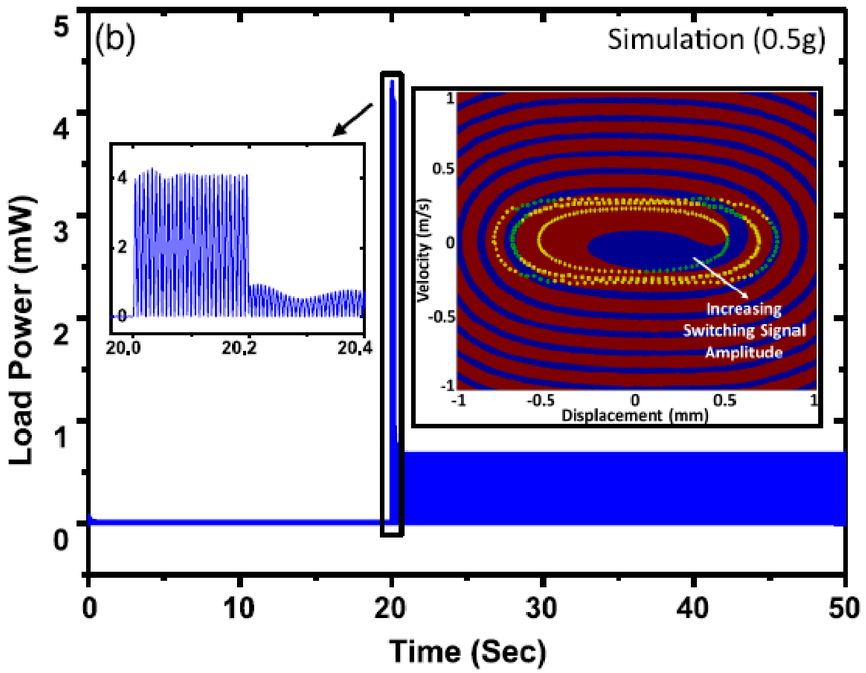
- Design for high reliability involves advanced packaging design
  - Signal interaction, such as displacement, strain measurement
  - Electrical techniques to increase reliability

"'Surfing the high energy branch of nonlinear energy harvesters', D. Mallick, S. Roy, Phys. Rev. Lett., week ending 4 NOVEMBER 2016, claim 32 X

Example for Electromagnetic VEH

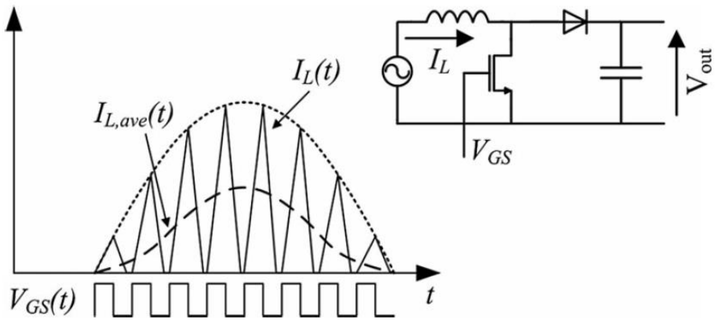
There are analogous techniques for Piezo under review by IEEE MEMS





Electromagnetic transduction – *Power Factor Improvement*

- Higher switching frequency for EMT



Power Factor Improvement Schemes are applicable to future EMT.

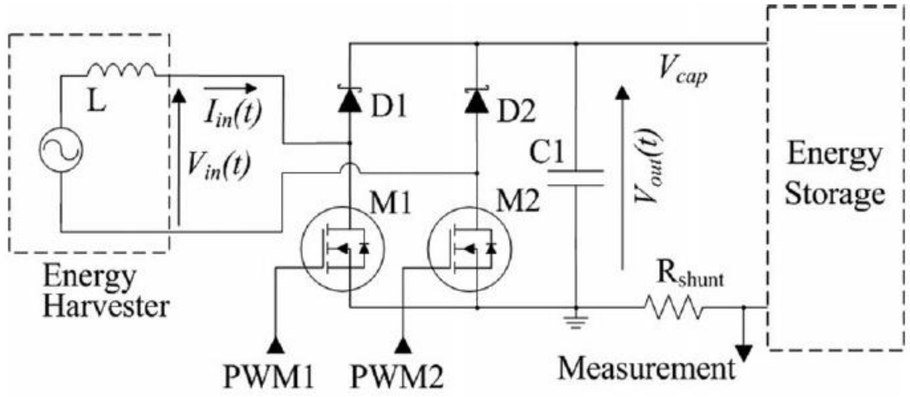
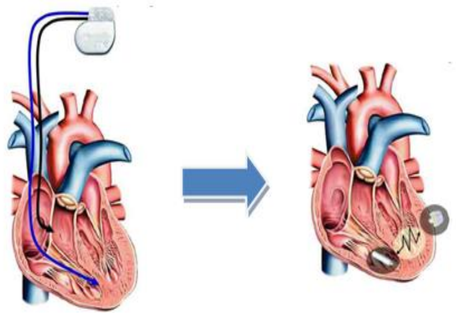


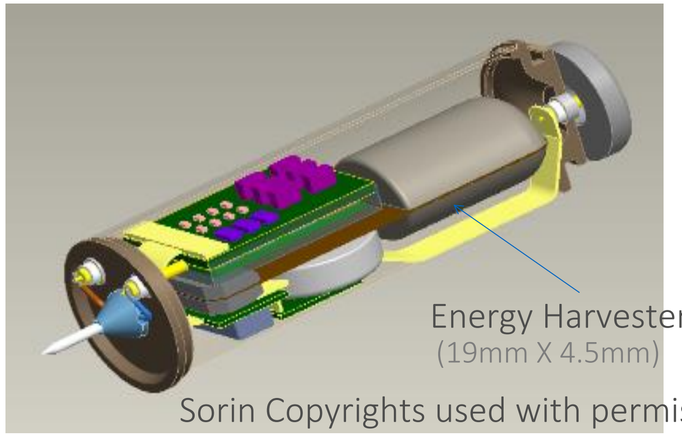
Fig. 9. Circuit schematic of a nonsynchronous, full-wave boost rectifier that uses the parasitic coil inductance as the boost inductor. The semiconductor devices used are M1/M2—PMF-280UN and D1/D2— 1PS79SB30.

SZARKA *et al.*: MAXIMUM POWER TRANSFER TRACKING FOR ULTRALOW-POWER ELECTROMAGNETIC ENERGY HARVESTERS, 2014, IEEE trans on Power Electronics

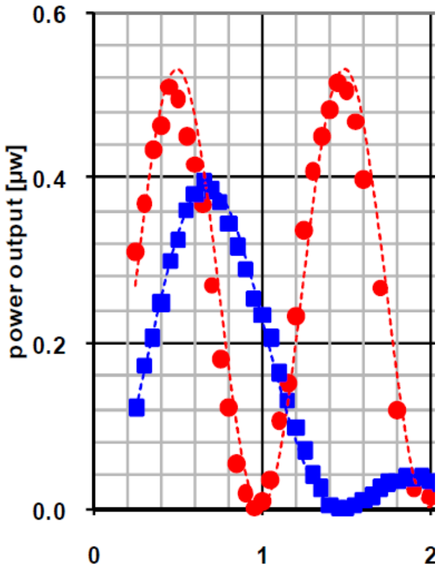
Higher power AC:DC community might describe this as Totem Pole Bridgeless Boost PFC

ULP PIEZO Research – AlN Piezo Harvester





www.themanpowerproject.eu



Elfrink et al. 2010

Blue: Shock induced off resonance

Red: At resonance

Leadless implantable – Tyndall created the Piezo harvester – double cantilever
~3uW (1-10V) average power operating at 60 bpm, fits inside a commercial leadless pacemaker.
Off-resonance based on impulse acceleration method – MEMs compatible process

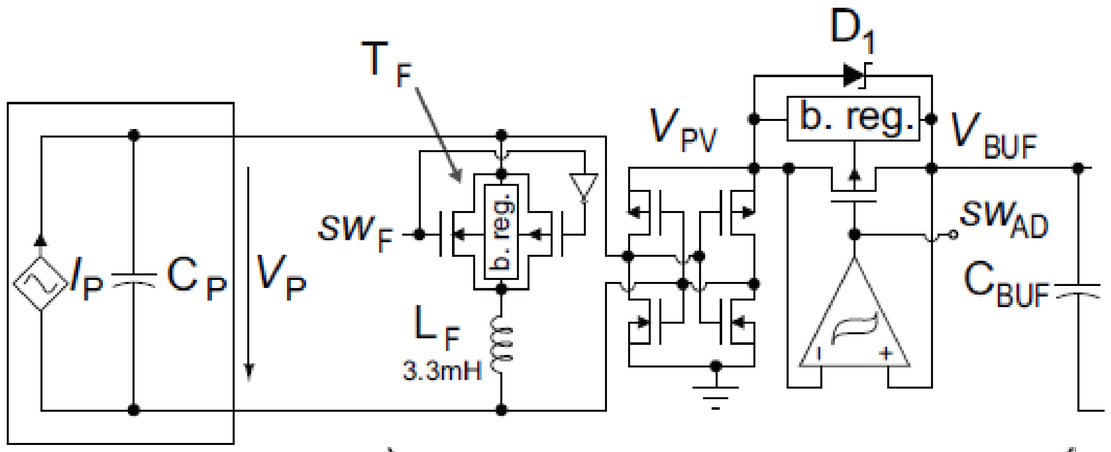
Substantial further improvements are possible and mixed signal control will add value

MCCI have developed 10-20µW PMICs for Pacing (~20V)

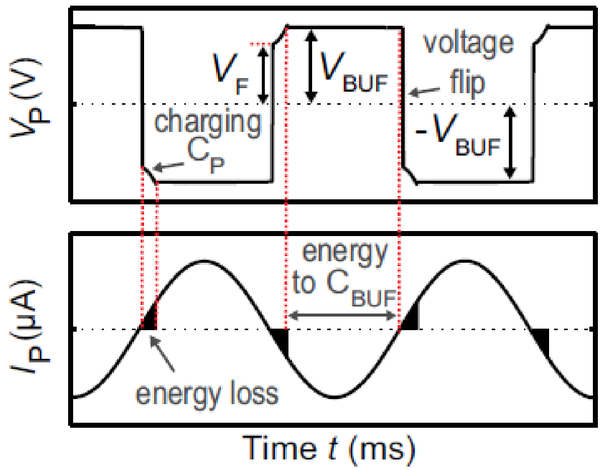
Engineering and development is application specific and about mechanical design, and packaging for reliability

Piezo – Energy Extraction at Mechanical Vibration Frequency from a Capacitive Source

- At the vibration frequency (Ω_M) – facilitates ULP
- A quickly evolving variety of Active Rectifier, Conduction Angle Extension (Bias Flip, Parallel Synchronous Switch Harvesting on Inductor (P-SSHI)) or other Synchronous Charge Extraction (SECE) techniques.



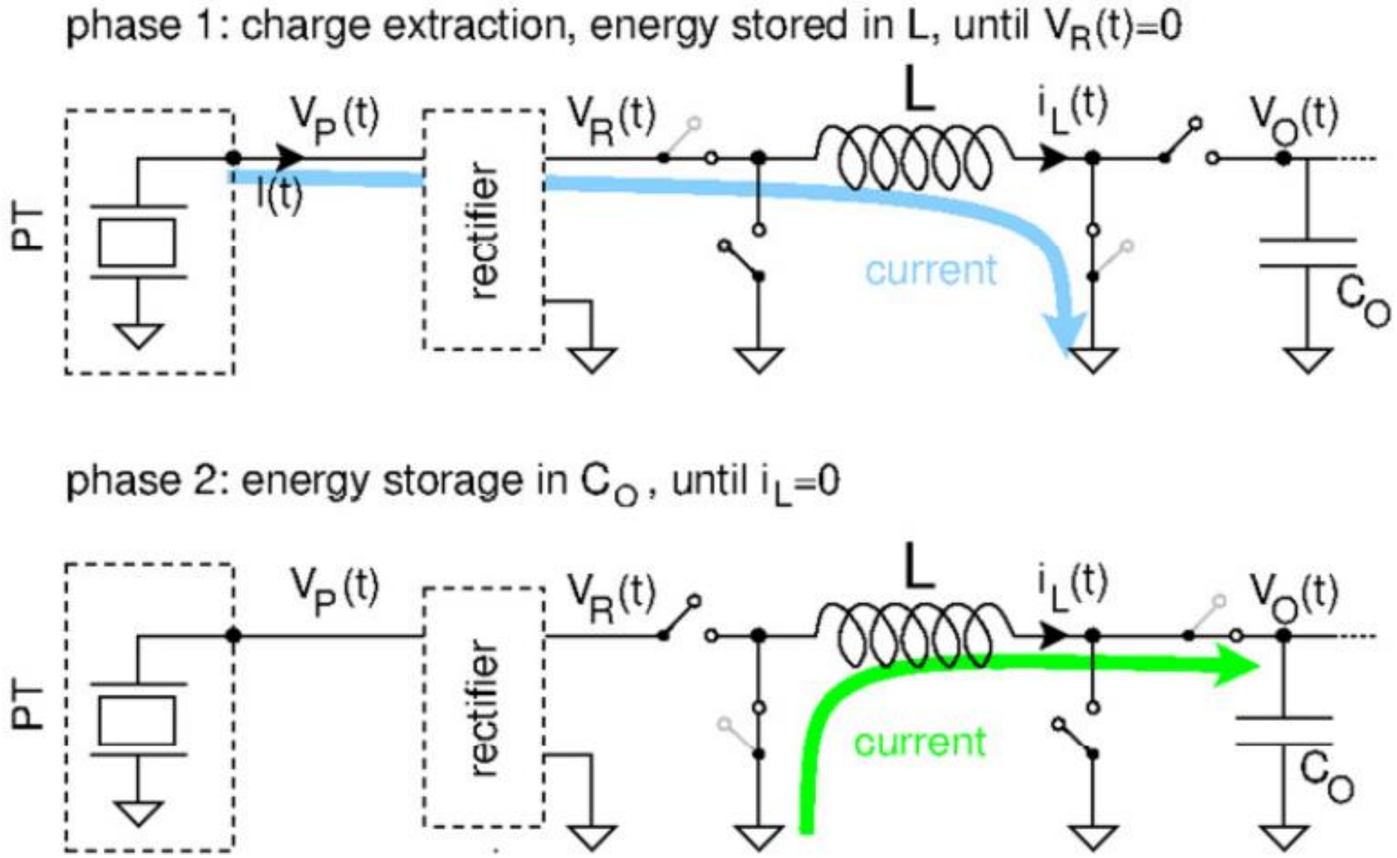
Piezo harvester with self capacitance, Cp

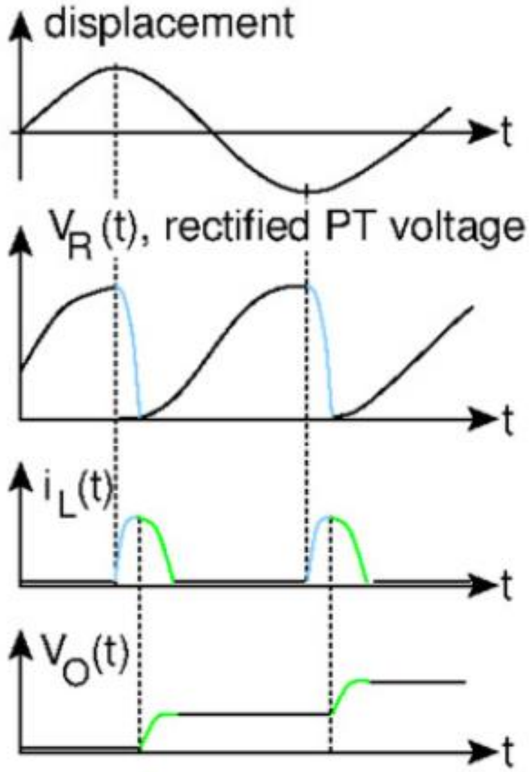


Current Source Generator results in Square Wave Voltage determined by MPPT Control of DC Voltage after the rectifier

"A 4µW-to-1mW Parallel-SSHI Rectifier for Piezoelectric Energy Harvesting of Periodic and Shock Excitations with Inductor Sharing, Cold Start-up and up to 681% Power Extraction Improvement", Daniel A. Sanchez et. al., ISSCC 2016

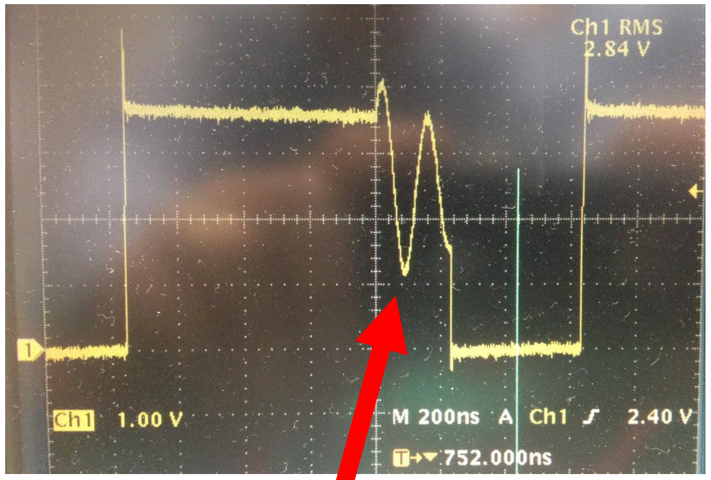
Piezo – *"Quasi-Synchronous Charge Extraction for Improved Energy Harvesting from Highly Coupled Piezoelectric Transducers",* *Aldo Romani*, Matteo Filippi, EUROSENSORS 2014*



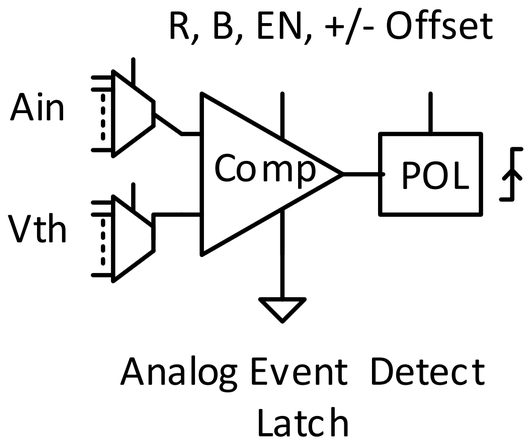


Topology is compatible with the 4 Switch Buck-Boost

ULP Smart Sensor Systems – PMICs integrated into Systems



Boost Switch Node Waveform for QR PMIC Switching



PMIC Controller Block and Triggered ADC Sampler for waveform event measurement

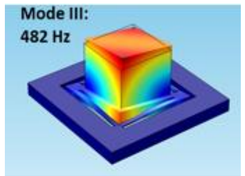
- PMIC blocks such as Resetting Integrators or Signal Interval Measurement will add large value in system
- PMIC switches and RF switches many be similar technology
- PMIC would benefit from blocks such as low energy demand driven ADC, essential in the Smart Sensor/Actuator System
- *The PMIC positions us very well with IP blocks to add value in low power smart system nodes*

Conclusions

- Energy Harvesting, Battery-Less, Maintenance Free or Very Long Life Systems are set for significant progress

- EH PMIC design could be integrated with RF and Controller Section in the ULP Smart Sensing/Actuator EH Battery-less Node SoC

- Our Gen.1 EH PMIC Test Chip Platform will enable SMPS Bucking/Boosting to System Voltages from 1uW upwards
  - Ambient VEH shows particular promise for x-fold improvement in power delivery
  - Mixed Signal features will add real value, with techniques such as Bias Flip/SECE schemes for Piezo or Non-Linear Stimuli for EMT
  - Massively increasing interplay between the mechanical and electrical states



- Tyndall is an ideal multi-disciplinary collaborative research centre
  - We welcome commercial partner engagements – various engagement models

Thank You

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