Industry Session 5: Energy Harvesting

Techniques for reducing ULP device power consumption

Presented By –

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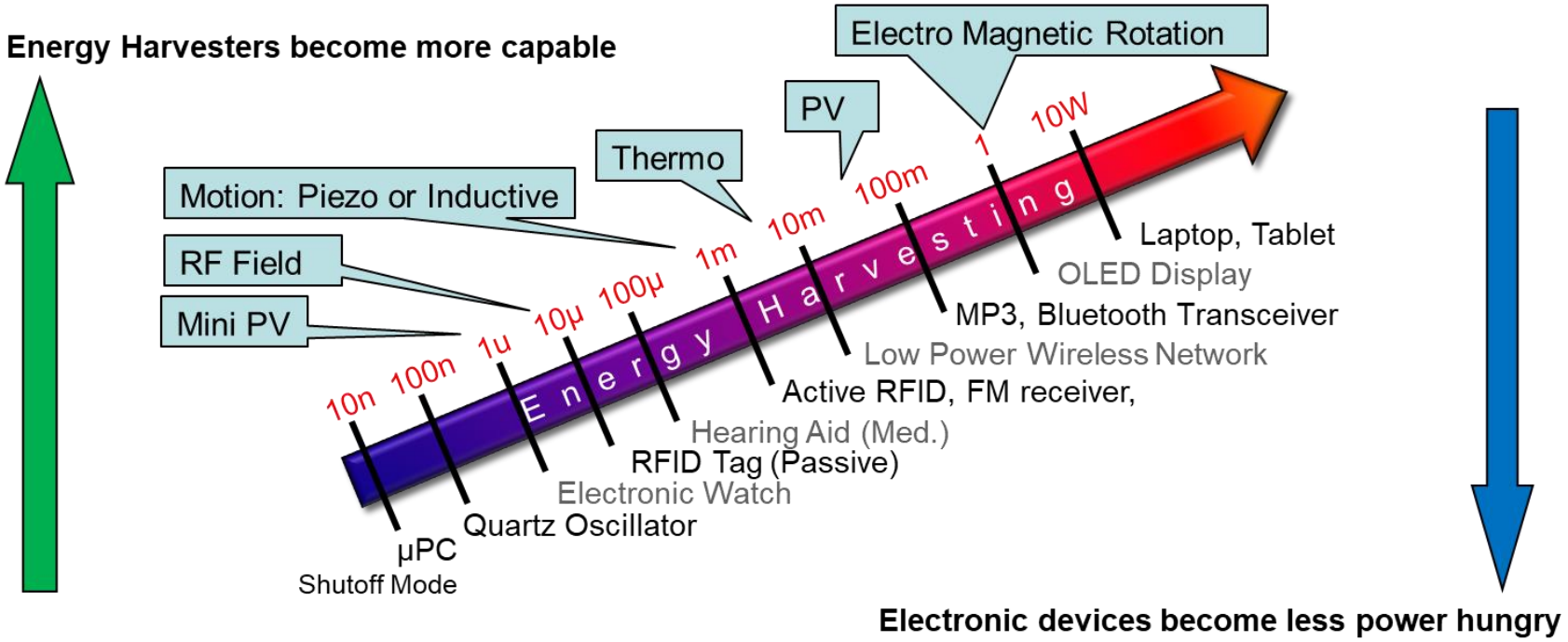
Tuesday, March 6, 2018

Energy Harvesting

- **Typical energy harvester output power**

➢ RF:	0.1μW/cm²	0.01mV
➢ Vibration:	1mW/cm²	0.1 ~ 0.4 V
➢ Thermal:	10mW/cm²	0.02 ~ 1.0 V
➢ Photovoltaic:	100mW/cm²	0.5 ~ 0.7 V typ./cell



Source: *Lorandt Foelkel, "Energy Harvesting Seminar," Wurth Elektronik eiSos, 2013*

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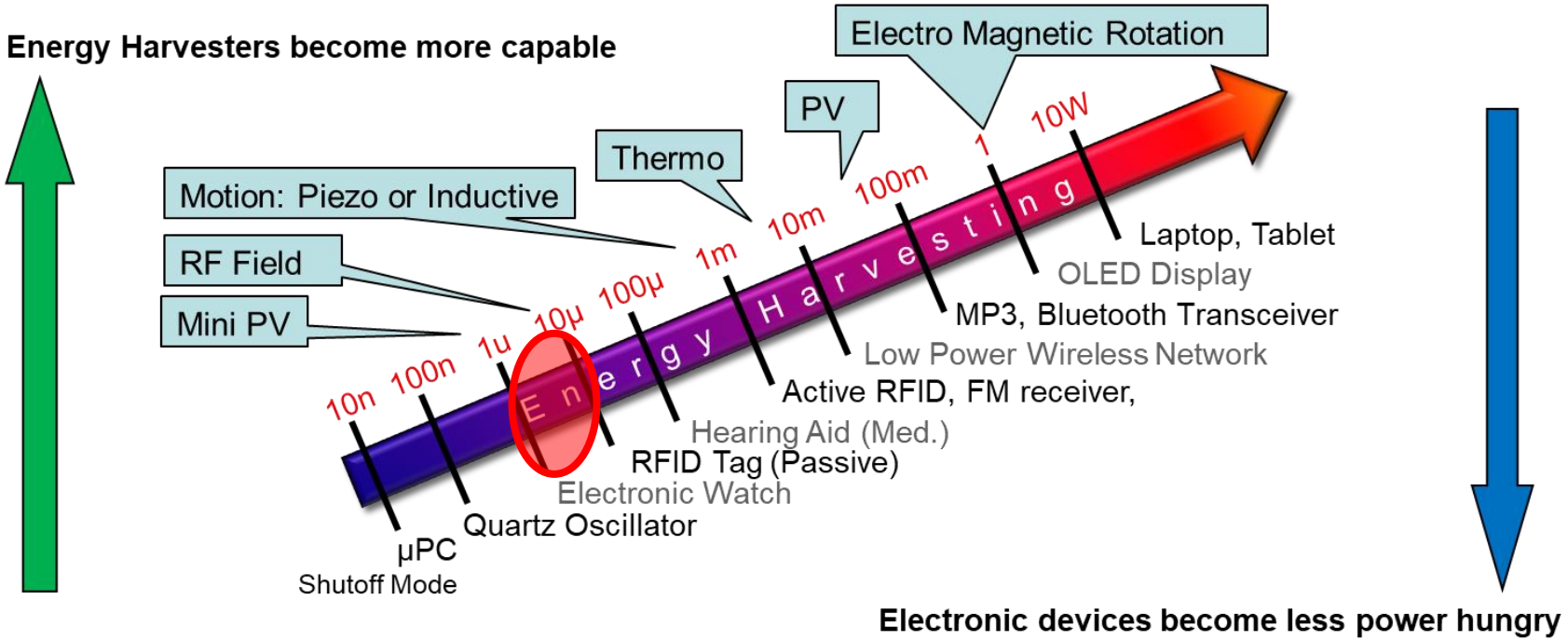

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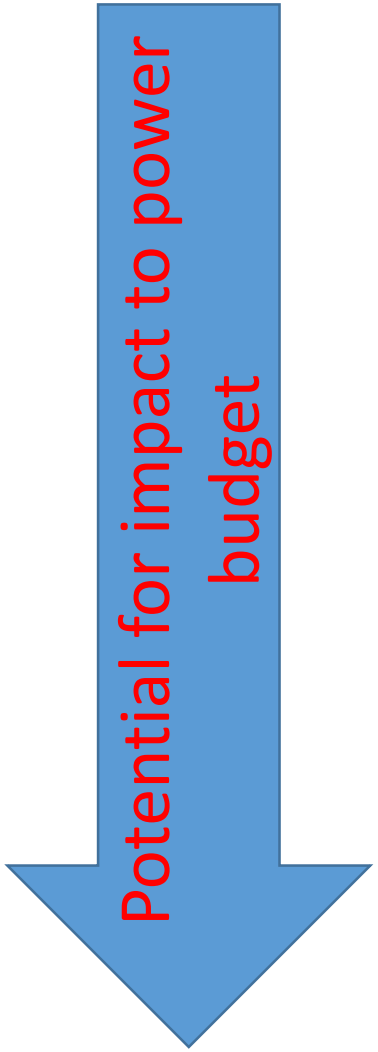
Motivation

- **Address the "Energy Gap"**
- **Designers always look for ways to reduce unwanted components of power consumption**
  - architecting the design in a fashion which includes low power techniques
  - adopting a process which can reduce the consumption
- **Always done at the expense of performance, reliability, chip area, or several of these**
  - one has to reach a compromise between power, performance, and cost

Power Drivers to reduce power consumption

- **Battery Powered Systems – Phones**
  - Mobile revolution has really driven need for low power design
- **High-Performance Systems – Server Farms**
  - Cost of removing the dissipated energy → Heat
  - Reliability
- **IoT**
  - Deploy and forget devices
    - Maximise battery life and minimse power source size
  - Transmitting data → processing at the edge can increase or decrease IoT device power consumption depending on uC, TRX, sensor, duty cycle etc.

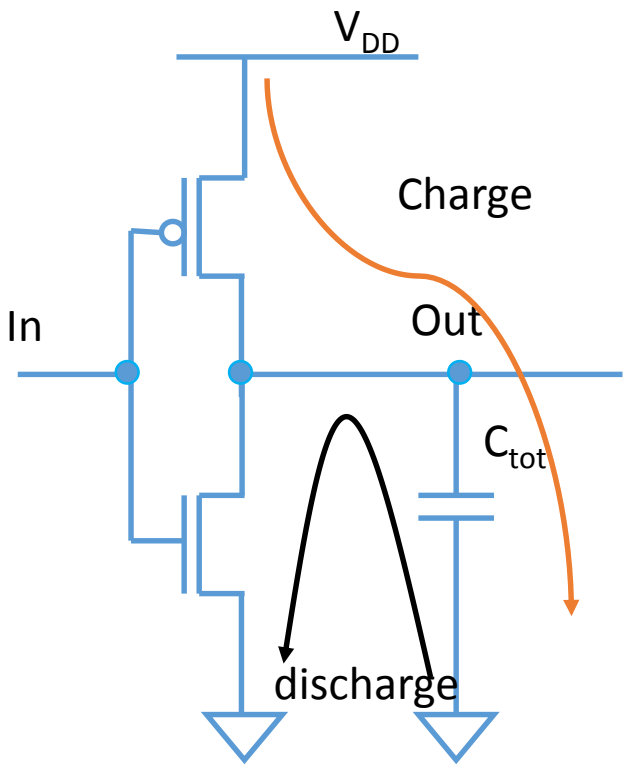
Factors to consider



- **Architectural decisions**
- **Process Technology**
- **Dynamic Power Consumption**
- **Static Power Consumption**

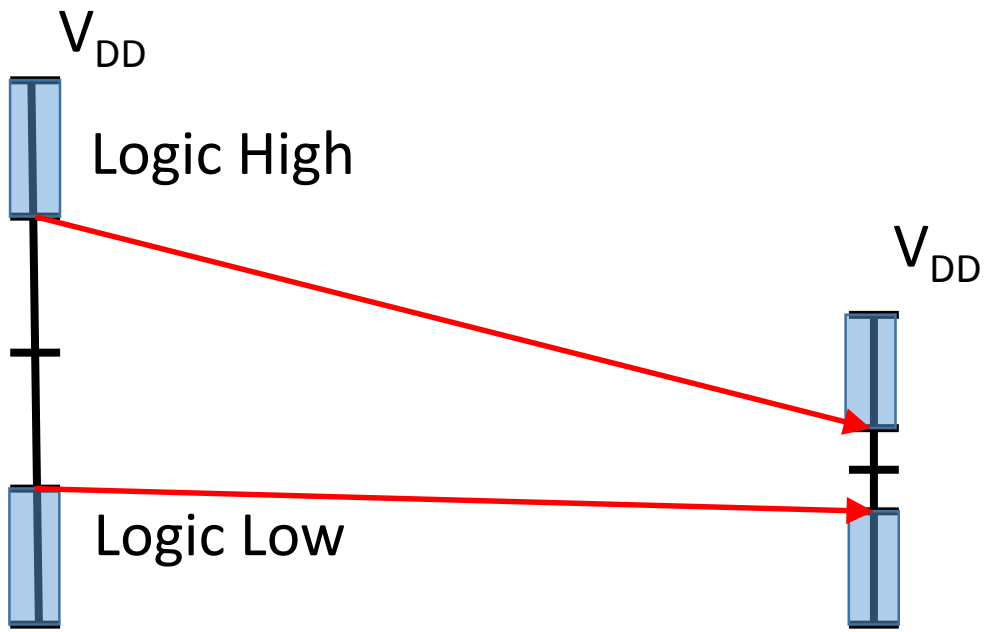
Dynamic Power Consumption

- **Switching & short circuit power**
- $P_{dyn} = \alpha C_{tot} V_{DD}^2 F$
  - $C_{tot} = C_{load} + C_{par}$
  - V_{DD} - Supply Voltage
  - F – clock Frequency



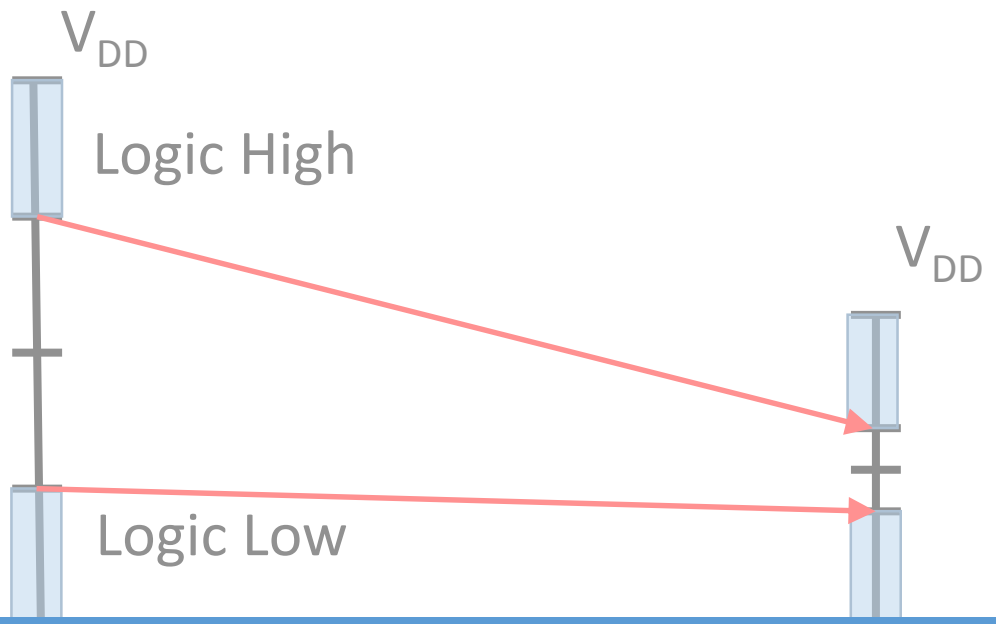
Dynamic Power Consumption ✓ ✓ ✓
Static Power Consumption ✓ ✓
Process Technology ✓
Architectural decisions

Voltage Scaling – Reducing the Supply Voltage



Limited by the ability to accurately differentiate between a 1 and 0

Voltage Scaling – Reducing the Supply Voltage



Limited by the ability to accurately differentiate between a 1 and 0

Dynamic Power Consumption ✓ ✓ ✓
Static Power Consumption ✓ ✓
Process Technology ✓
Architectural decisions

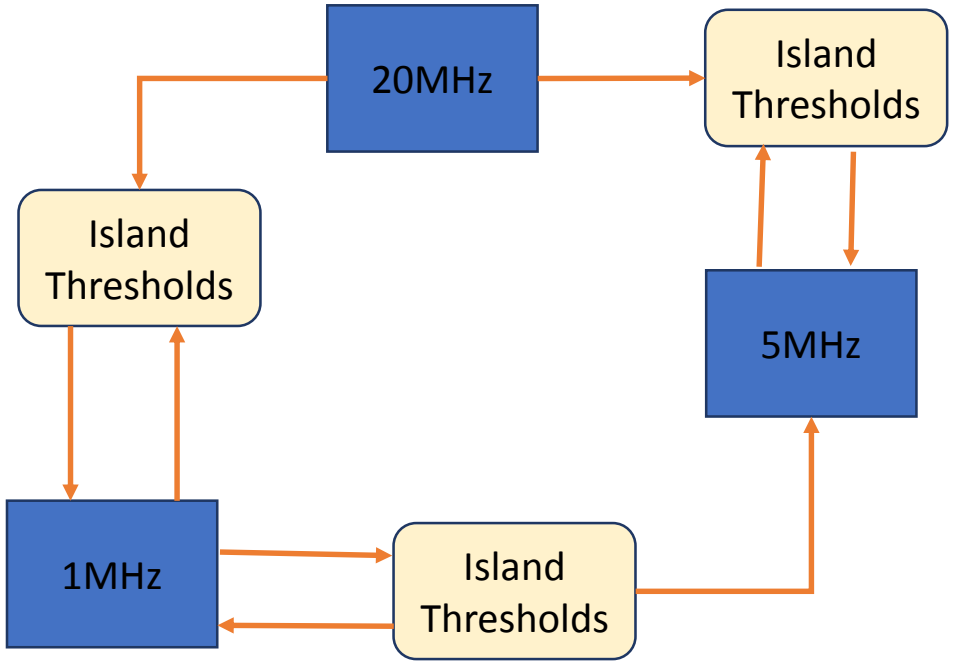
Clock Gating

- Remove unnecessary switching activity
- Only clock necessary blocks
- Remove clock from other blocks

Dynamic Power Consumption ✓ ✓ ✓
Static Power Consumption
Process Technology
Architectural decisions ✓

Frequency scaling

- **Clock frequency adjusted to meet requirements**
- **Frequency islands**



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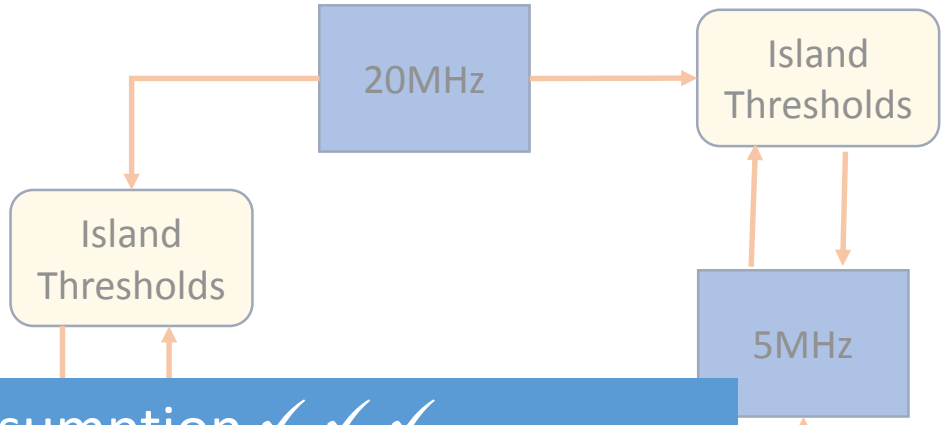

Dynamic Power Consumption ✓ ✓ ✓
Static Power Consumption
Process Technology
Architectural decisions ✓

Asynchronous logic

- **Synchronous**
- **Clock Driven**
- **P_{dyn} → activity independent**

- **Asynchronous**
- **Event Driven**
- **P_{dyn} → activity dependent**

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Dynamic Power Consumption ✓ ✓ ✓
Static Power Consumption
Process Technology
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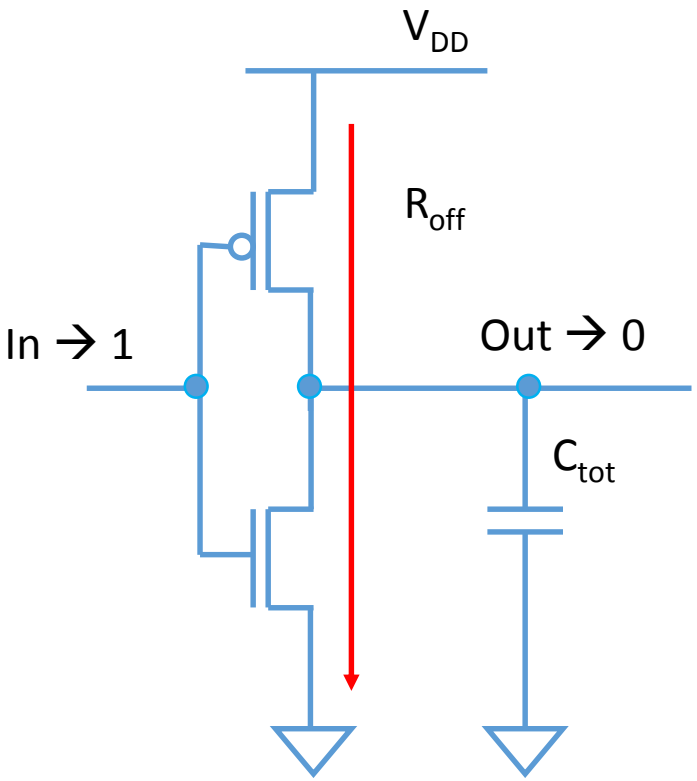
Static – Leakage Power Reduction

- **The power a circuit consumes when it's doing nothing!**
- **Finite off Resistance**
- **$P = k\ V_{DD}$**
  - Voltage scaling
  - Technology
  - Device Selection
    - High Vt Devices



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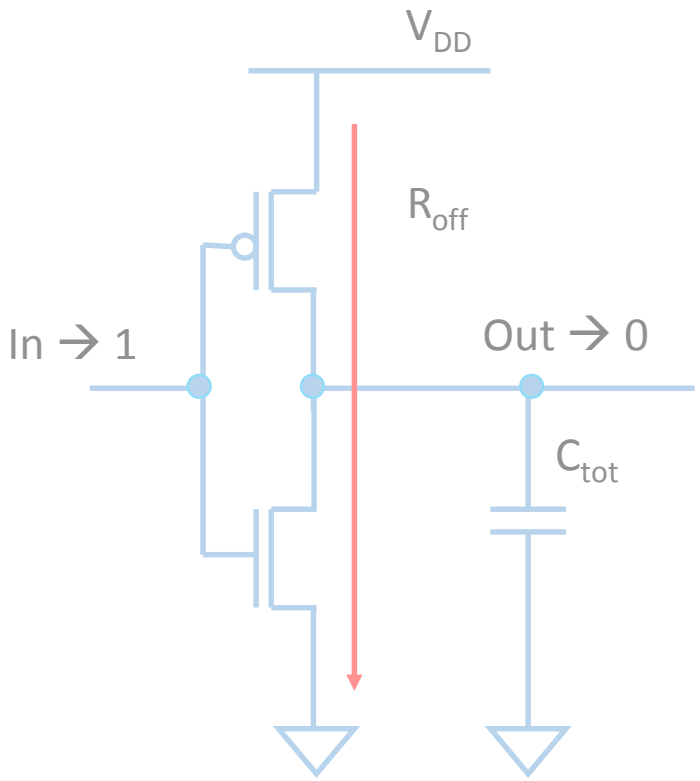
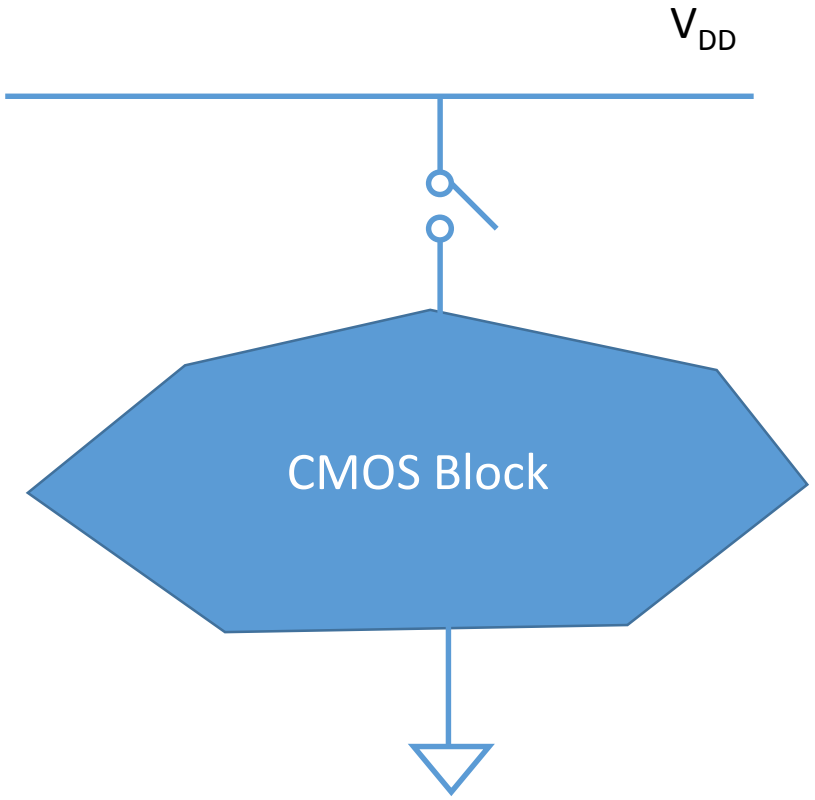


Dynamic Power Consumption ✓
Static Power Consumption ✓ ✓
Process Technology ✓ ✓
Architectural decisions ✓ ✓

Power Gating

- **Remove the power to inactive blocks**
- **Leakage Power → zero**



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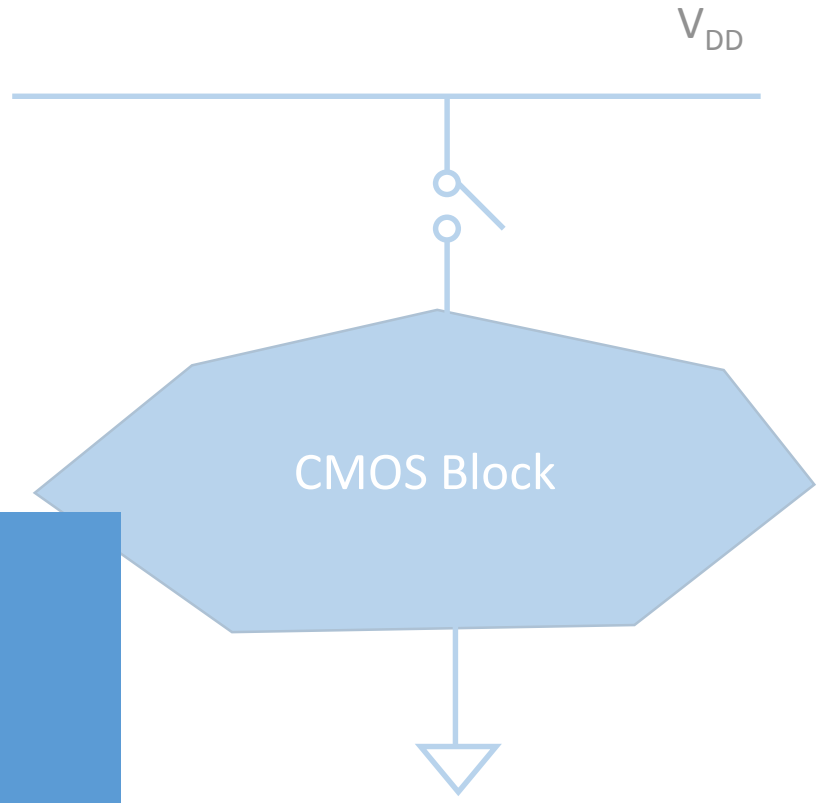
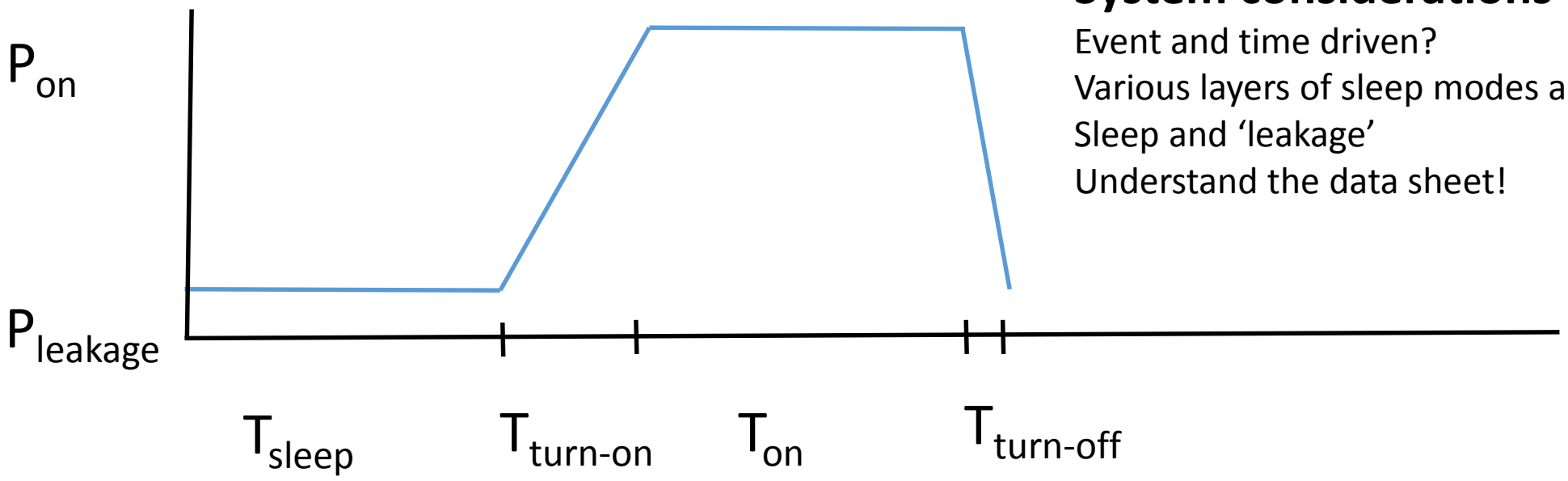


Dynamic Power Consumption
Static Power Consumption ✓ ✓ ✓
Process Technology ✓
Architectural decisions ✓ ✓

Power Duty Cycling

- **Turning on and off sub-blocks to minimise the power consumption**



System considerations

Event and time driven?
Various layers of sleep modes and ability to interrupt?
Sleep and 'leakage'
Understand the data sheet!

Power Duty Cycling

- T_{sleep} – time the device spends in sleep mode
- $T_{turn\text{-}on}$ – time the device/block takes to turn on
- T_{on} – active time
- $T_{turn\text{-}off}$ – time it takes to turn the device/block off

- **Objective**
  - $P_{avg} = 2x\ P_{leakage}$
    - e.g. $P_{on} = 100 \times P_{leakage}$
    - $T_{sleep} = 100 \times T_{on}$

Limited by the Leakage Current

Power Duty Cycling

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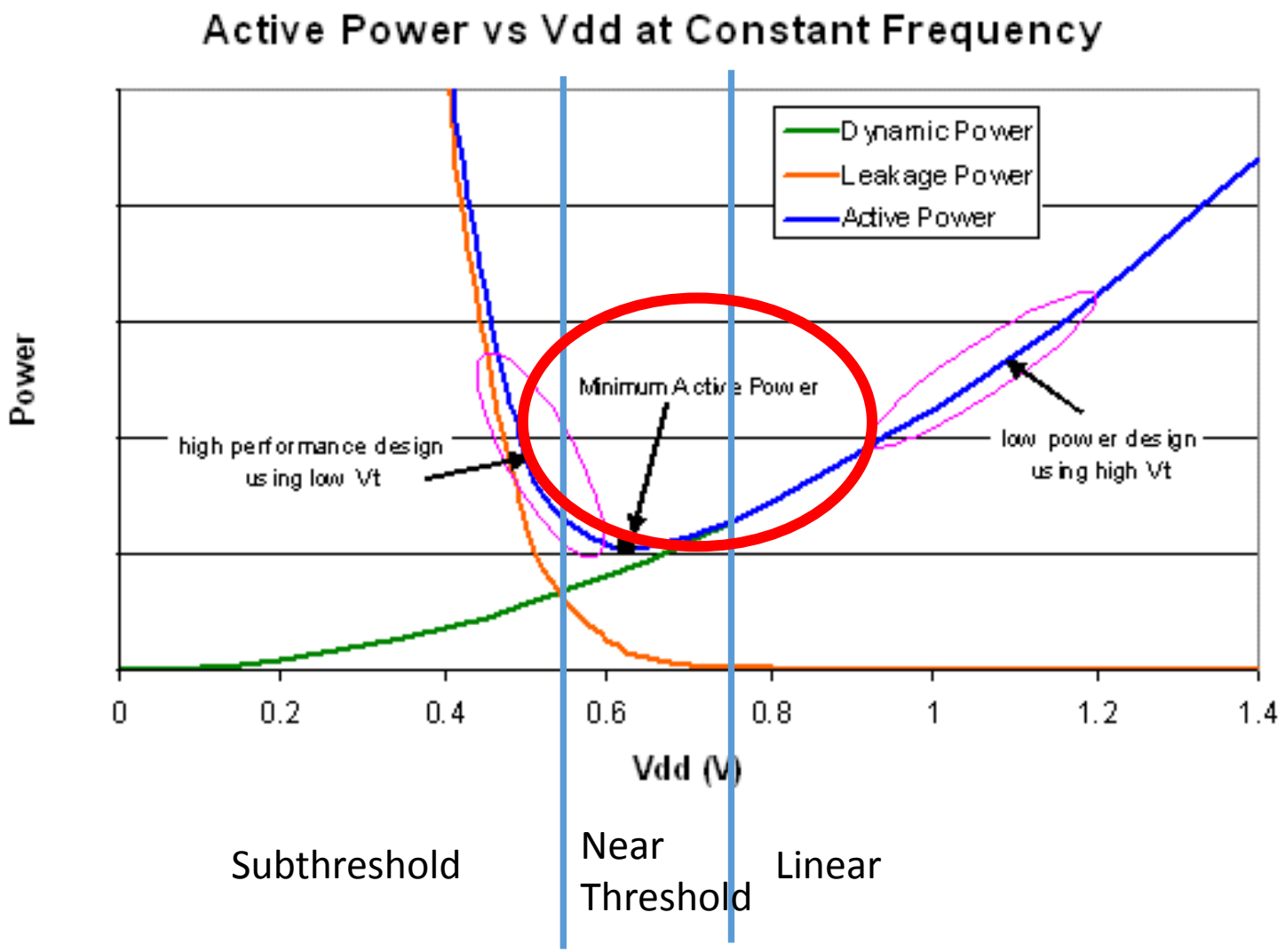
- Objective

Dynamic Power Consumption
Static Power Consumption ✓
Process Technology
Architectural decisions ✓ ✓ ✓

ited by the Leakage Current

MOS Transistor Regions of operation

- **Linear Region**
- **Near Threshold**
- **Sub Threshold**



Source: www.design-reuse.com/news_img/20090316b_5.gif

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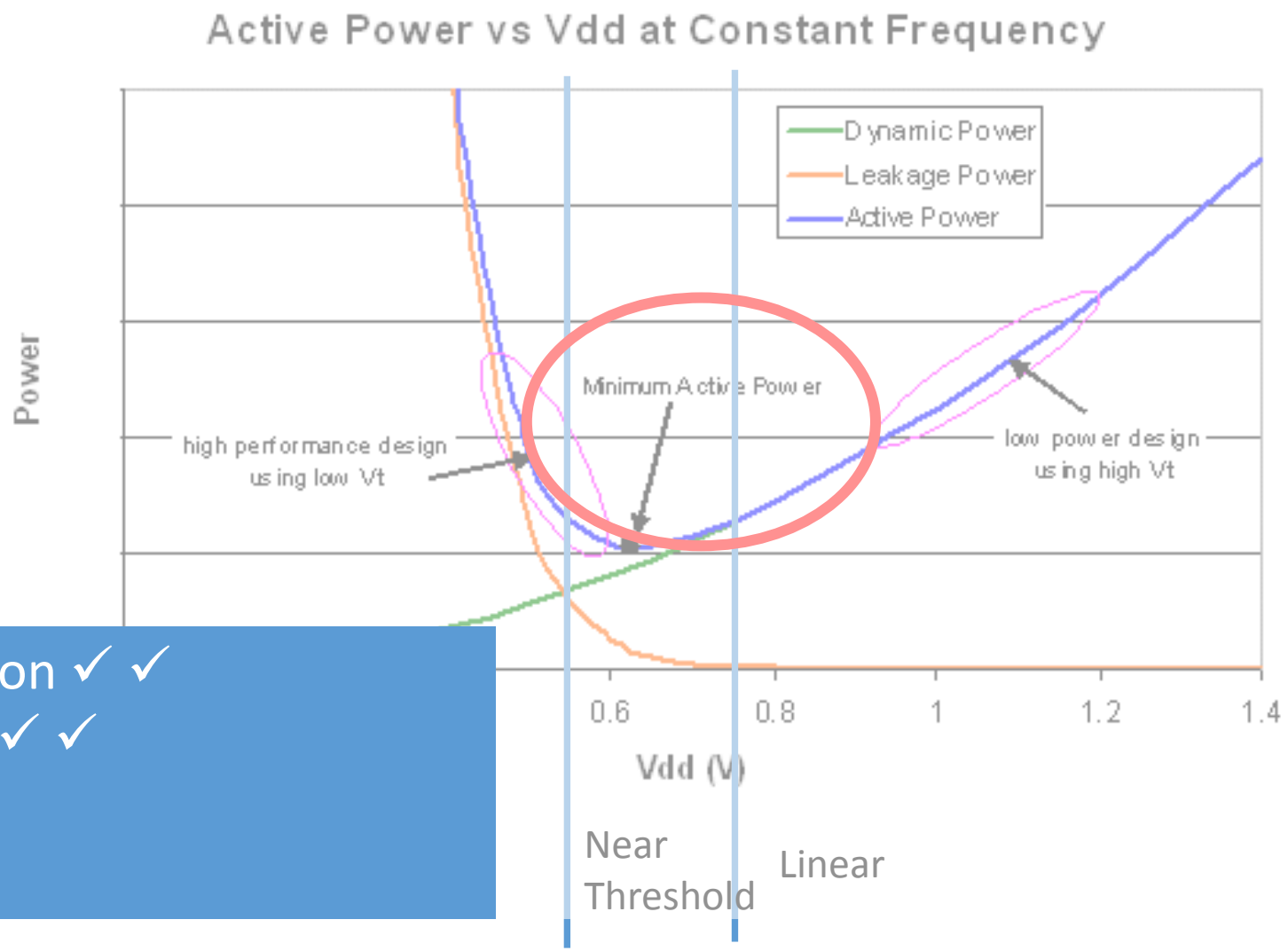

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Technology Scaling – Moore – More than Moore

A-series chip supplier TS

Secure https://9to5mac.com/2018/01/23/tsmc-5nm-3nm/

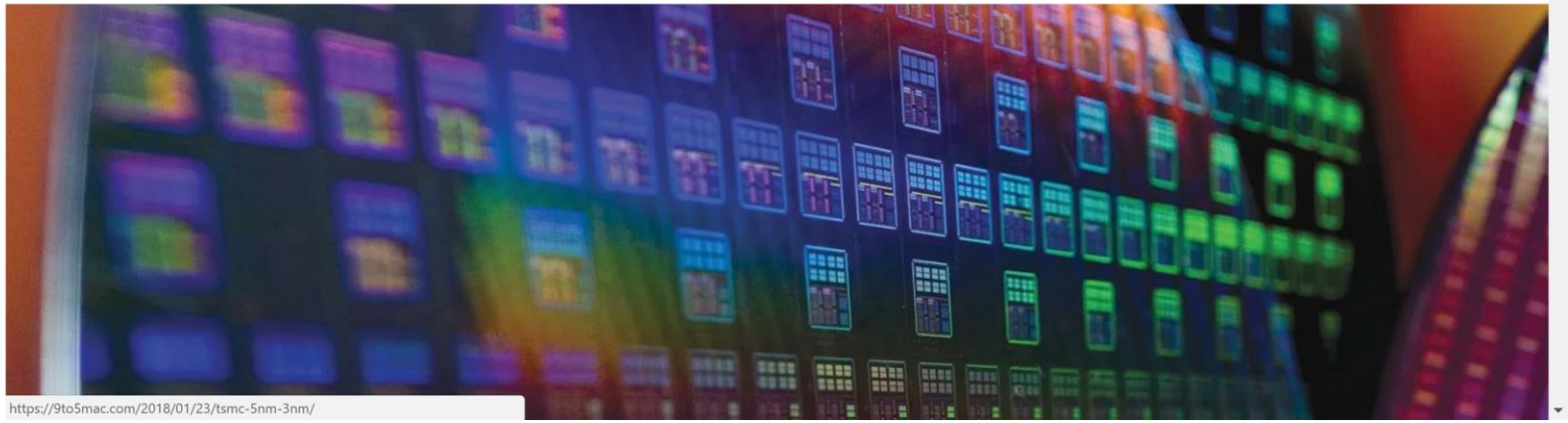
9TO5Mac

Guides Mac iPad iPhone Watch TV Music

JANUARY 23

A-series chip supplier TSMC working on making 5nm chips in 2020, 3nm in 2022

Ben Lovejoy - Jan. 23rd 2018 4:59 am PT @benlovejoy



https://9to5mac.com/2018/01/23/tsmc-5nm-3nm/

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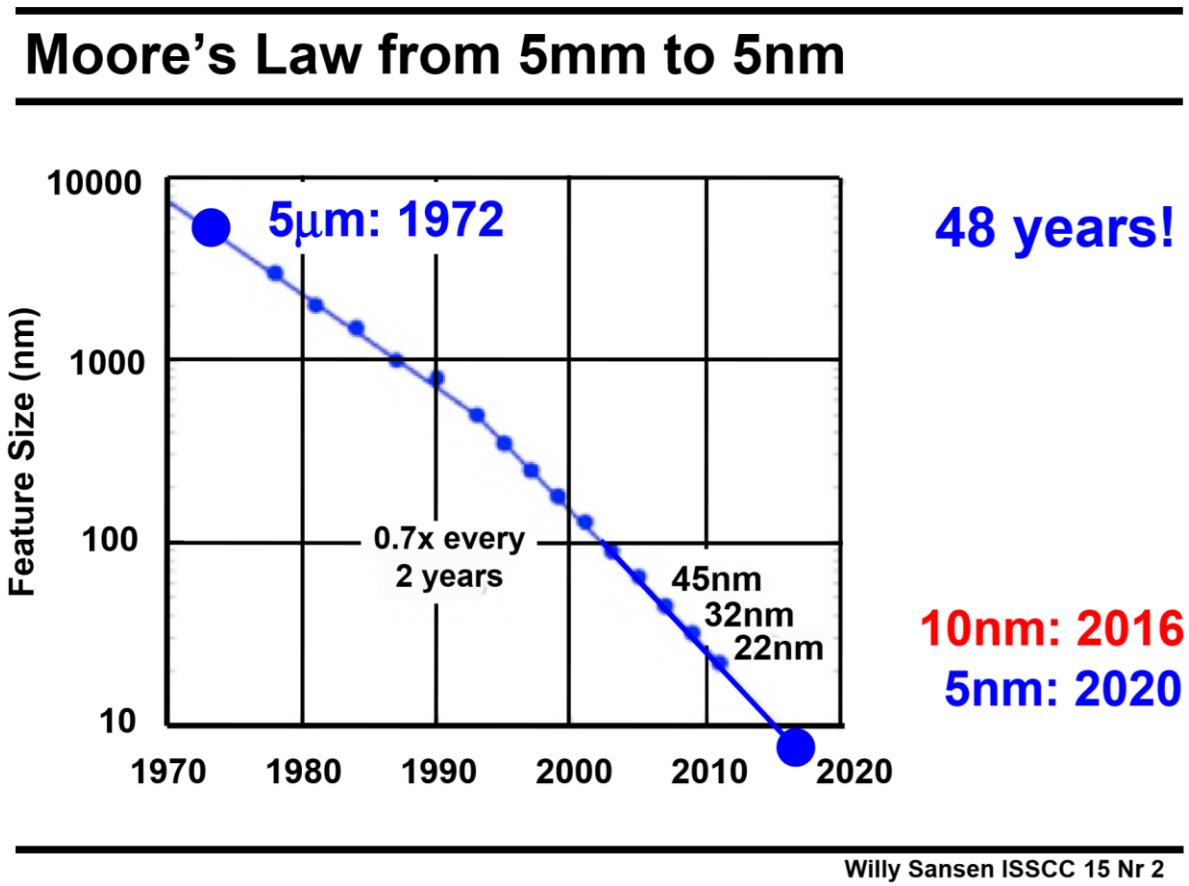
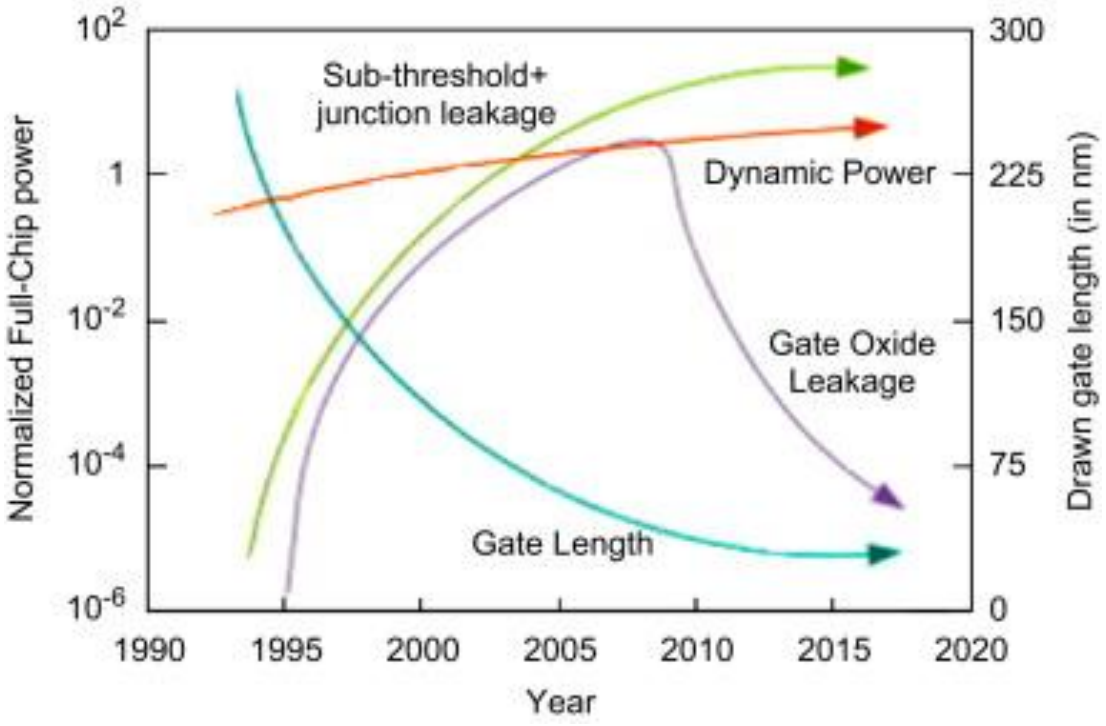


CMOS Technology Scaling

- **Process scaling will continue**
- **Cost/transistor no longer reducing**
- **Energy density increasing**
- **Leakage currents increasing**
- **Mature process nodes here to stay**
  - Driven by reliability requirements
  - Cost



Source: Z. Abbas, M. Oliveri "Impact of technology scaling on leakage power in nano-scale bulk CMOS digital standard cells" Microelectronics Journal

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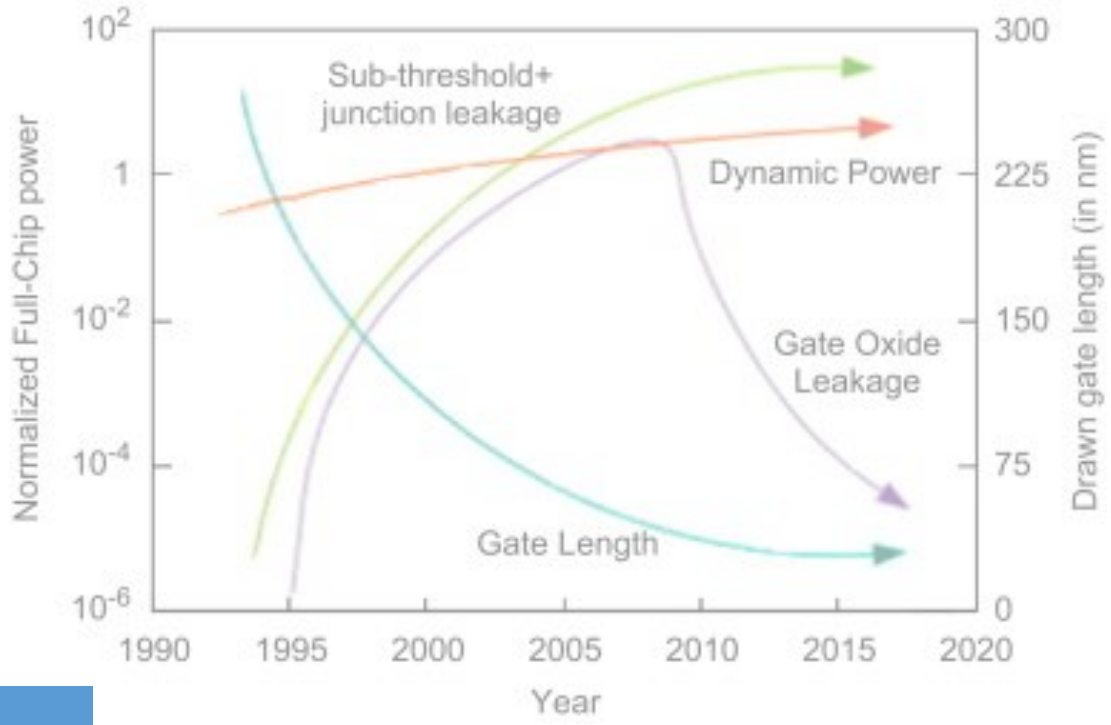

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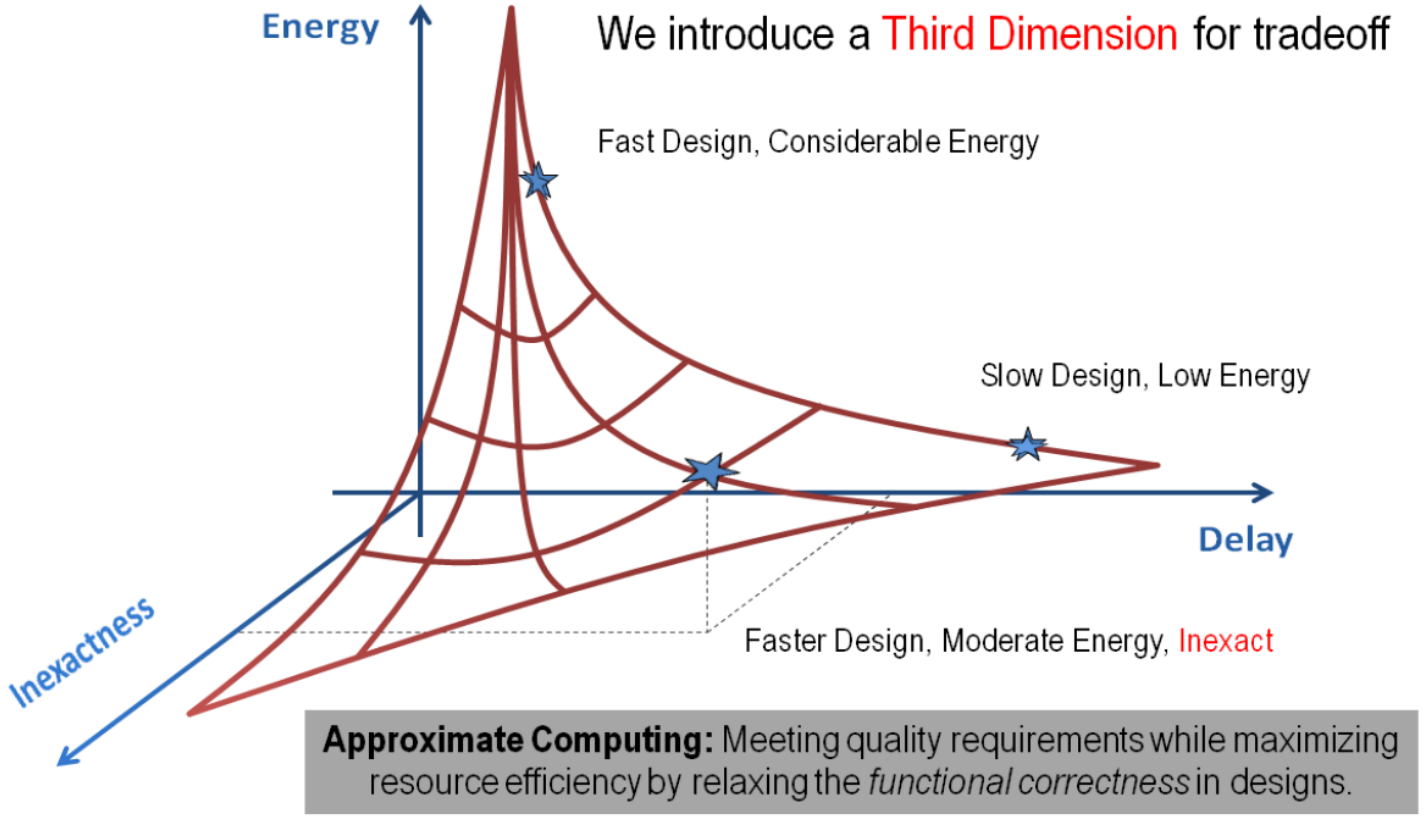
Adequate computing

- **Full precision is not always required!**
- **Circuits / Systems are over designed**
- **Driven by QoS**

The introduction of a New Dimension: Inexactness



- Courtesy: EPFL –

Source: EU Workshop ““Energy-Efficient Computing Systems, dynamic adaptation of Quality of Service and approximate computing”

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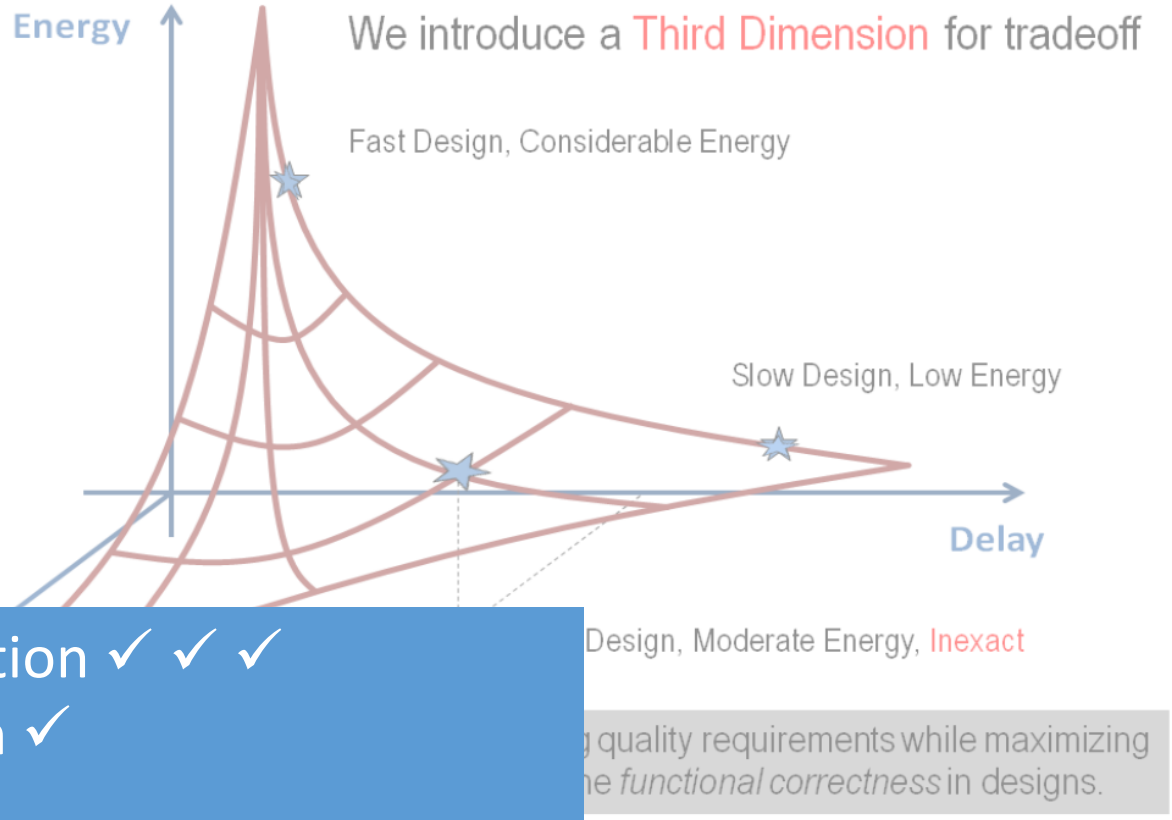

Dynamic Power Consumption ✓ ✓ ✓
Static Power Consumption ✓
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Source: EU Workshop ""Energy-Efficient Computing Systems, dynamic adaptation of Quality of Service and approximate computing"

Some recent developments – self powered

ISSCC 2018 / SESSION 17 / TECHNOLOGIES FOR HEALTH AND SOCIETY / 17.3

17.3 A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Employing a 180nW 64dB SNR Passive ΔΣ ADC and a 920MHz Wireless Transmitter

Ali Fazli Yeknami, Xiaoyang Wang, Somayeh Imani, Ali Nikoofard, Itthipon Jeerapan, Joseph Wang, Patrick P. Mercier

University of California, San Diego, La Jolla, CA

Wearable physiochemical biosensors offer an exciting opportunity to monitor the

or PMOS transistors, and are activated by a 3× clock booster (NMOS), or a -200mV charge pump (PMOS), as shown in Fig. 17.3.3 (top middle).

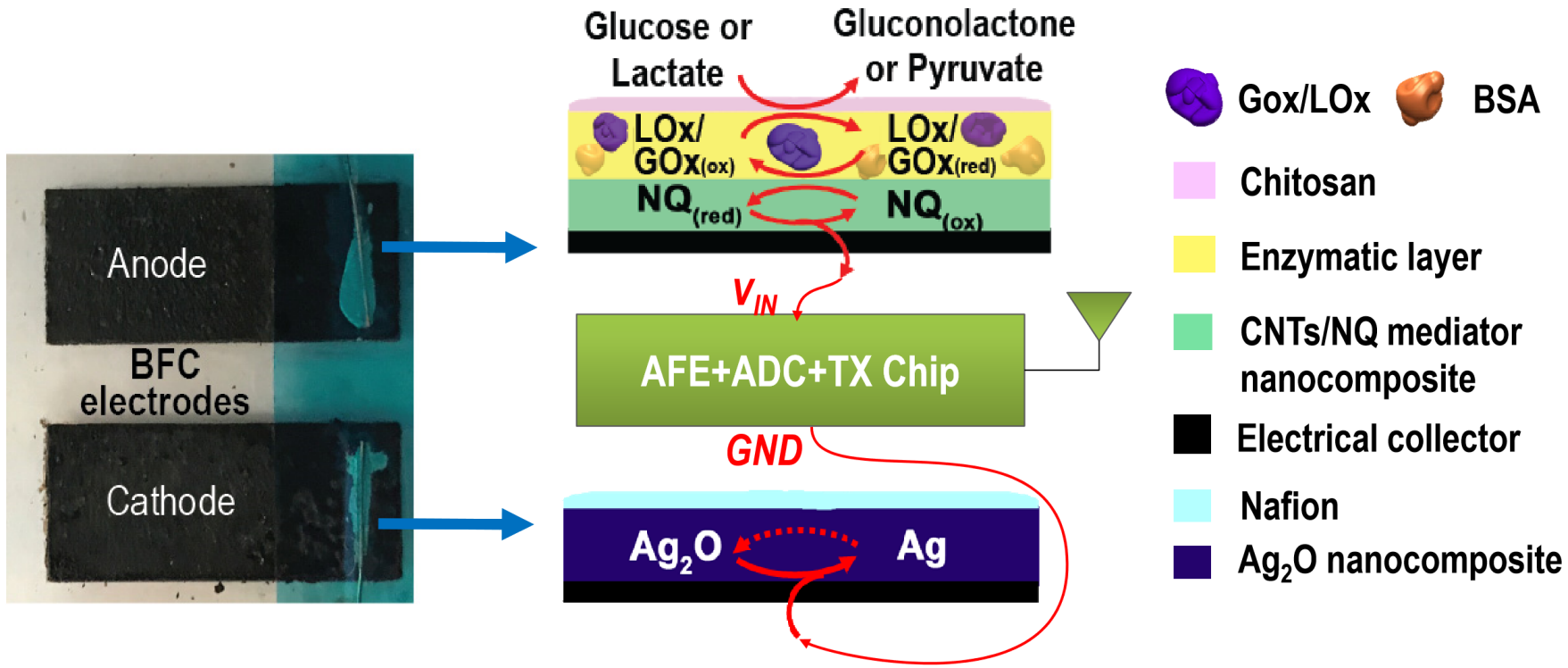
Output bits from the ΔΣM are passed through a *sinc*² decimation filter, and stored in a FIFO until the TX is activated. The TX is designed as a single-stage direct-RF OOK-modulated power oscillator (RFPO) [6] that provides inherent impedance matching with a 1cm 920MHz on-board loop antenna (Fig. 17.3.4). Unfortunately, the 0.3-to-0.4V supply would limit the efficiency, the I_{ON}/I_{OFF} ratio, and the start-up time of the circuit in [6], and boosting the main power supply to compensate would require unnecessarily large inductors or capacitors. Instead, in this design the tail transistor, M_0, is designed to operate in triode by boosting its gate voltage

- **0.3 V system**
- **1.15 μW**
  - Signal acquisition 180 nW
  - Tx Active power 30.1 μW

Source: ISSCC 2018: 17.3 A.F. Yeknami et al "A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Employing a 180nW 64dB SNR Passive ΔΣ ADC anda 920MHz Wireless Transmitter"

Some recent developments – self powered

BFC Material Composition



- BFC cathode material composition

Conclusions

- **A lot of progress has already been made…**
  - Energy Gap is reducing (e. ISSCC – disappeared)
  - Portfolio of tricks/techniques available
  - No silver bullet technique
- **Application driven system level approach required**
  - Block performance vs overall system
    - Revisit system partitioning!
- **Much more work to do in PMICs area**
  - Managing multiple sources
- **Much more work to do in Power Usage**

Q & A

Thanks a lot for your time and attention!

Any questions and/or comments?