

Attracting Tomorrow

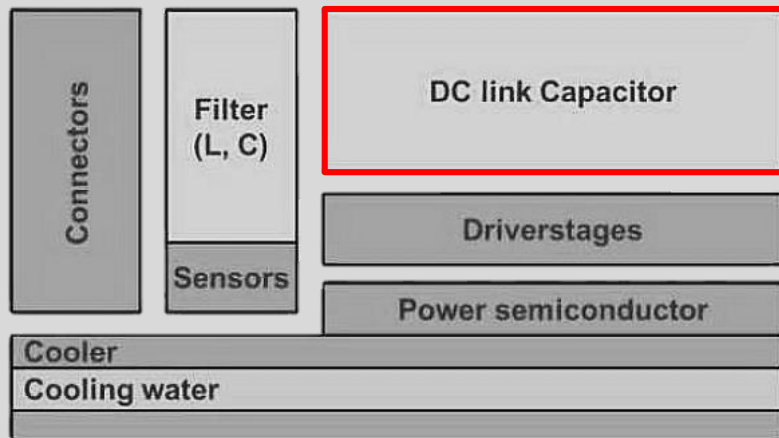


PLZT (lead-lanthanum-zirconium-titanate) Capacitors for High Frequency Operation

Presenter: Matt Reynolds / Suresh Chandran

New demands on DC-link capacitors

Improvements in power density and efficiency were mainly driven by semiconductor technology in the last decade.



Example: principle block picture and size comparison of a motor inverter

“Today the package of a motor inverter is mainly driven by the size of the capacitor, the bus bars, the terminal box and the filter components.”

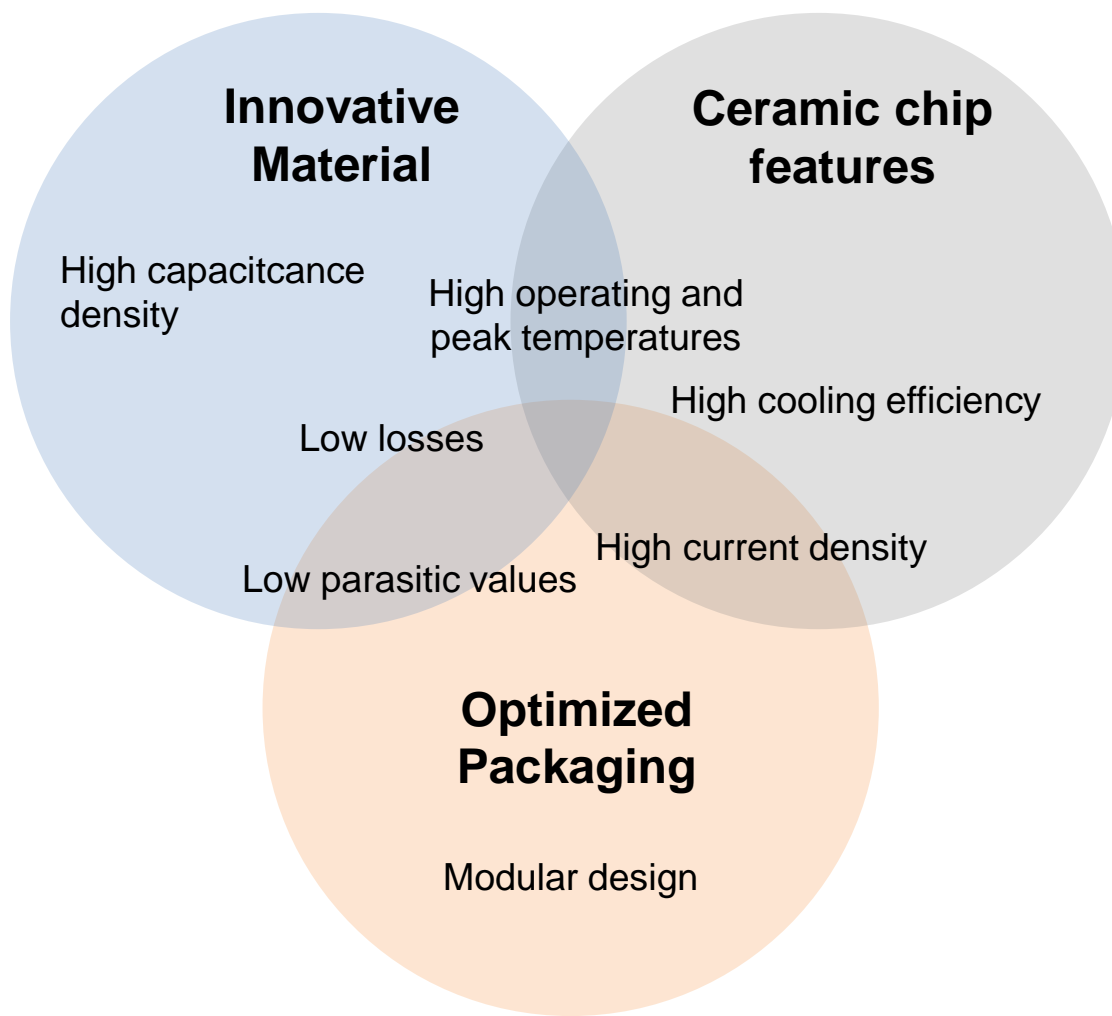
from: Plikat, Mertens, Koch, Volkswagen AG, Corporate Research, 2013

Requirements for a DC link capacitor

- High capacitance density
- High current density
- Low parasitic values (ESR / ESL) for fast switching
- Low losses in operation
- High operating and peak temperatures
- High cooling efficiency due to high thermal conductivity
- Support of distributed DC link capacitor topologies with low inductance components (modular design)

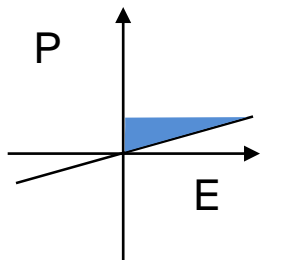
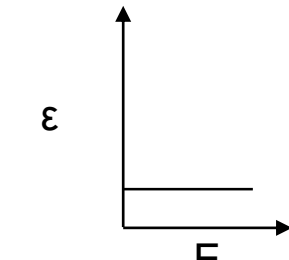
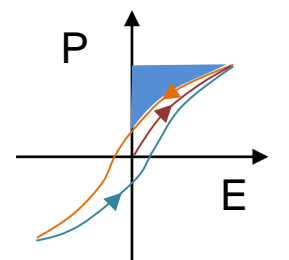
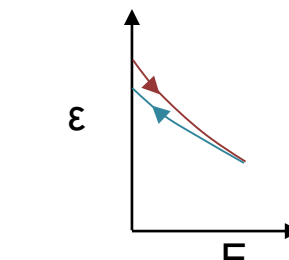
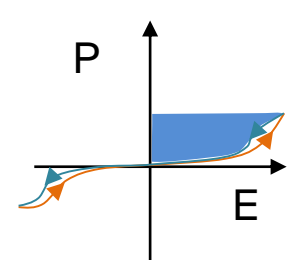
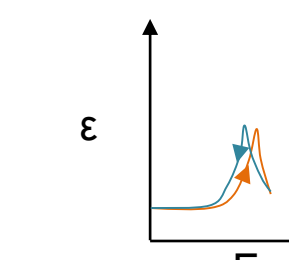
How does PLZT Capacitor meet these requirements?

TDK PLZT Capacitor is meeting the demands on three levels:



PLZT – comparison to other materials



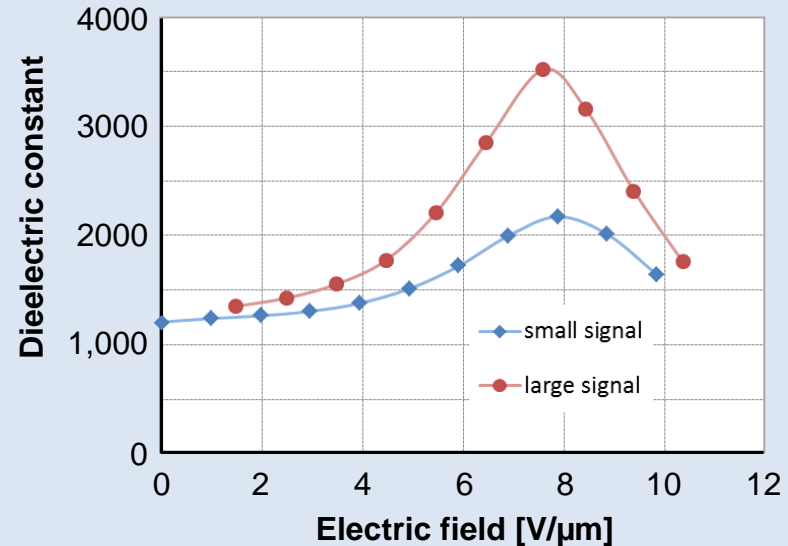
	Linear	Ferroelectric	Antiferroelectric
	 	 	 
Nature of electrical polarization	electronic, ionic	permanent dipoles form ferroelectric domains	permanent dipoles form antiparallel zones
Material class	(Ba,Nd)TiO, typ. NP0, C0G	BaTiO ₃ (BTO), typ. X7R	(Pb,La)(Zr,Ti)O ₃ (PLZT)
Advantages	ε constant over electric field and temperature	ε up to 10,000 is possible	ε increases with field
Disadvantages	ε < 100	ε decreases strongly with electrical field	ε low at zero bias

P Dielectric polarization
E Electrical field strength
ε Dielectric constant.

High capacitance density under electrical field

- Due to antiferroelectric behaviour, CeraLink's features are strongly non-linear and optimized for conditions under operation in power electronics
- Film capacitors and class 1 ceramics have a dielectric constant (nearly) independent on the electrical field. ($\epsilon < 100$)
- The permittivity of ferroelectric (BTO) MLCC capacitors is decreasing with electrical field
- CeraLink™ features an increasing dielectric constant up to the operating voltage
- At higher AC voltage (peaks), the material is able to provide even higher permittivities

DC bias characteristics at room temperature



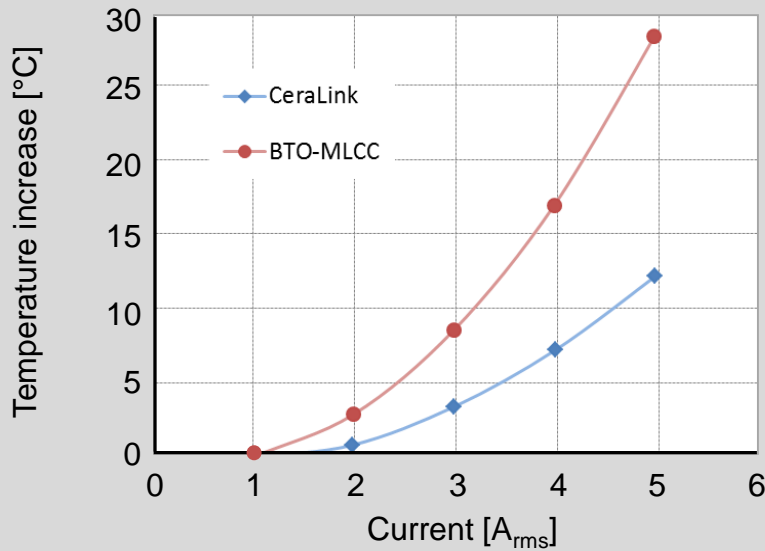
	MKP film capacitor	BTO Class 2 MLCC	CeraLink™
Nominal / rated capacitance	100 %	100 %	100 %
No bias voltage 0.5 V _{RMS}	100%	100 %	35 %
DC link voltage 0.5 V _{RMS}	100 %	35 %	60 %
DC link voltage 20 V _{RMS}	100 %	35 %	100 %

High current density – low self heating

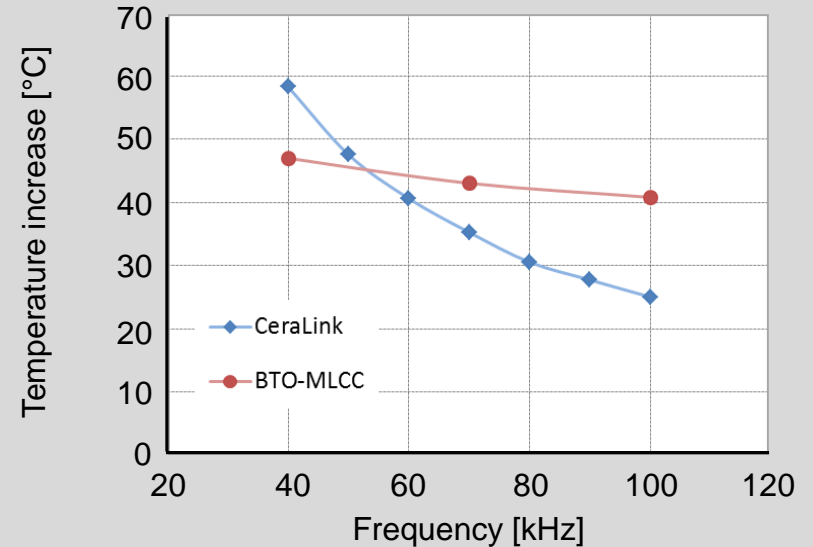
- Due to low losses at high temperature and high frequency, CeraLink™ can carry more current under these conditions

Measurement condition	MKP film capacitor	BTO Class 2 MLCC	CeraLink™
Typical capacitance density @ DC link voltage, 20 V _{RMS} , 25°C	0.7 μF/cm ³	2.5 μF/cm ³	4.9 μF/cm³
Typical current rating per capacitance @ 100 kHz, 105°C	< 1 A/μF	< 4.5 A/μF	12 A/μF

Comparison @ 400 V_{DC}, 105 °C, 200 kHz



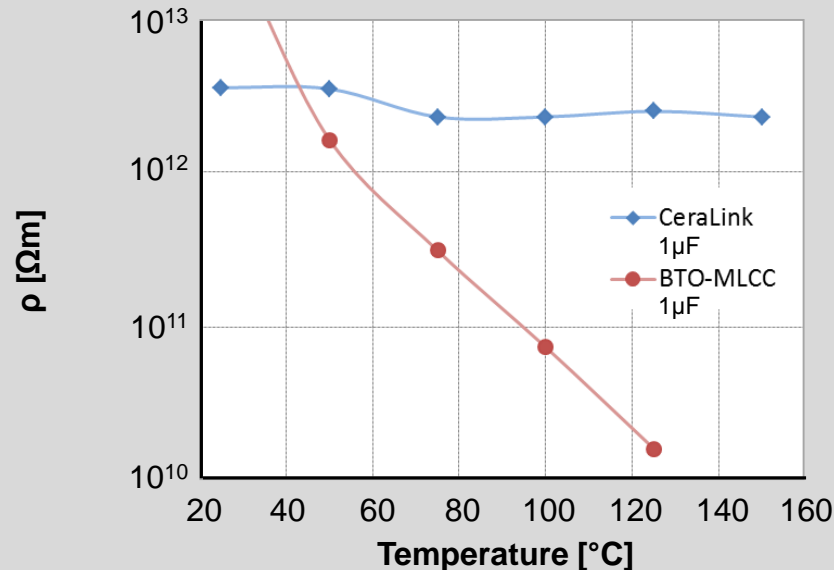
Comparison @ 400 V_{DC}, 85 °C, 5 A_{rms}



Measurements were carried out without active cooling (no forced air flow, no heat sink)

Low leakage current at high temperatures

Comparison @ 400 V_{DC}

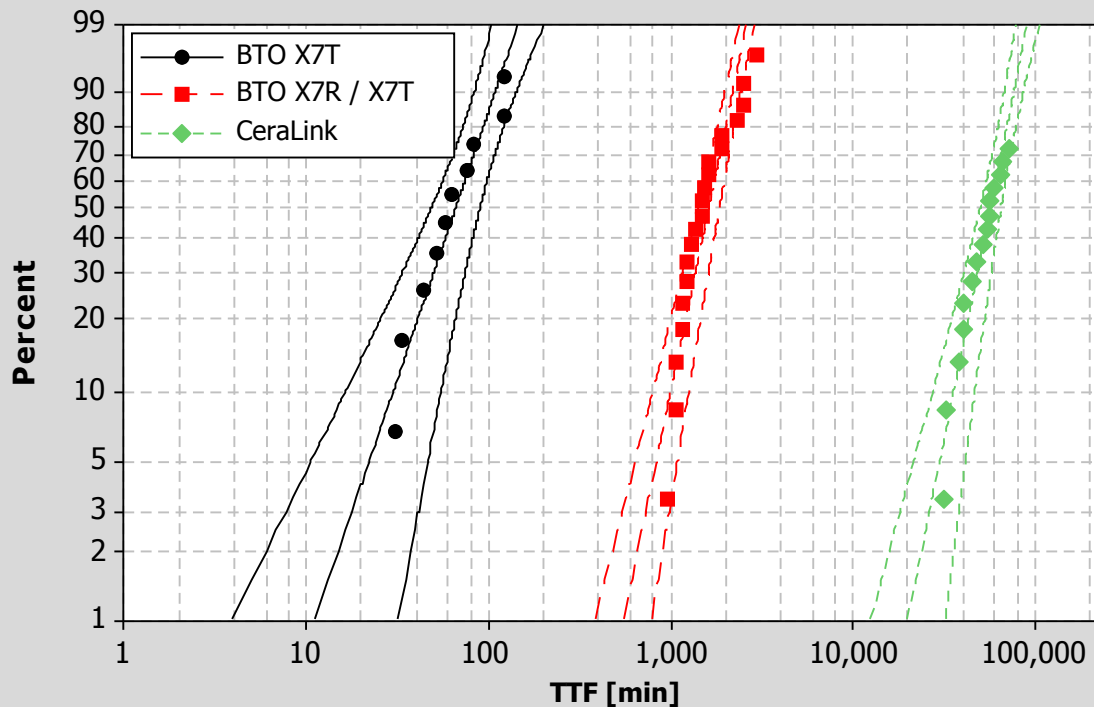


- CeraLink shows stable and outstanding high isolation properties compared to all existing capacitor technologies
 - ➔ low leakage current at elevated temperatures even above 150°C
 - ➔ No thermal runaway observed for CeraLink ceramic material

Exceptional lifetime at high temperatures

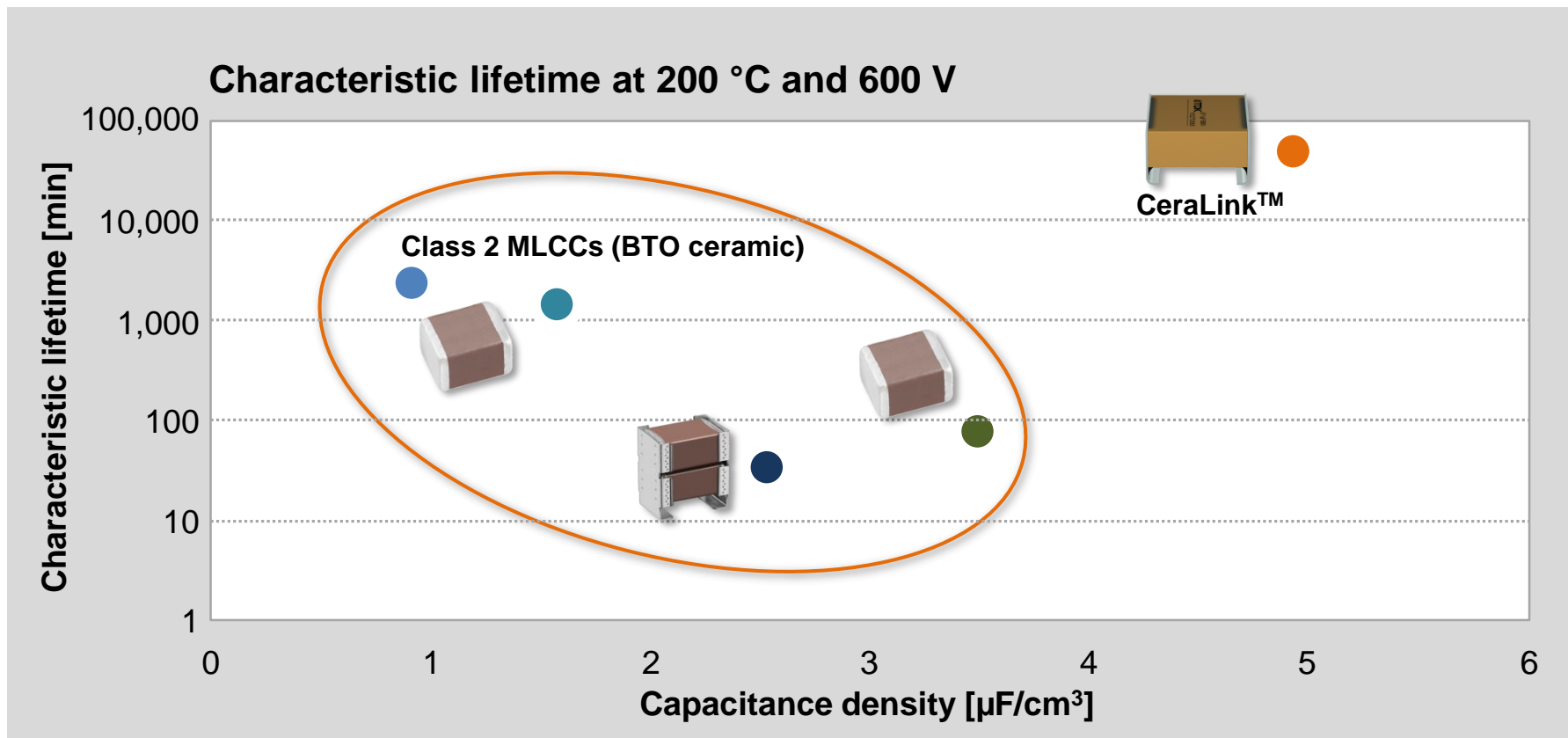
Highly accelerated life test (HALT) 200°C / 600 VDC

Weibull - 95% CI



Lifetime @ 200 °C more than one order of magnitude higher than that of conventional ceramic capacitors.

Lifetime at high temperatures - comparison of ceramic capacitors



CeraLink offers highest lifetime and highest capacitance density compared to conventional ceramic capacitors.

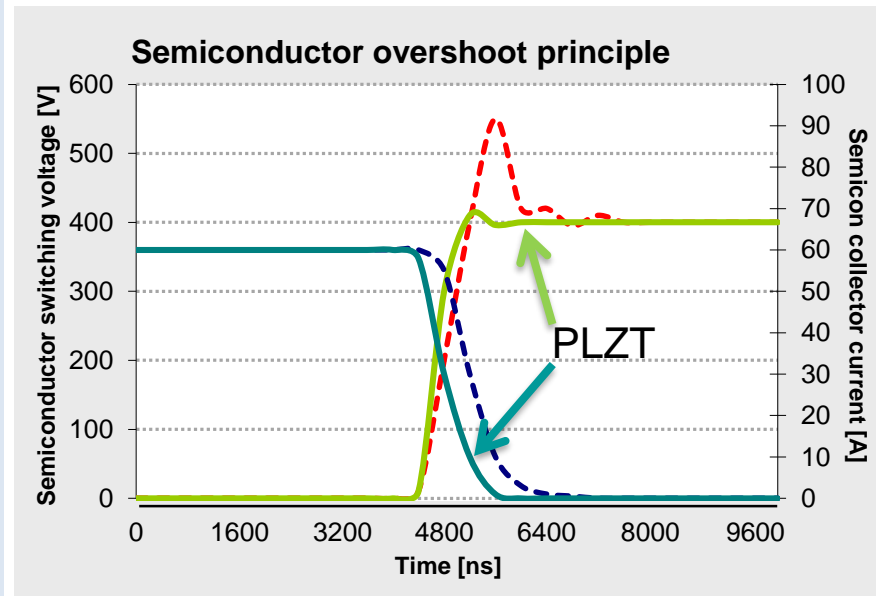
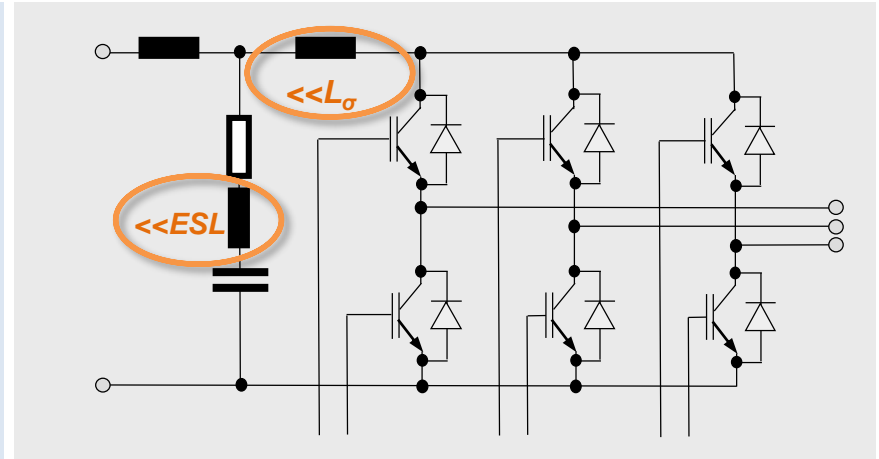
Low parasitic values

Device characteristics lead to a low inductive commutation loop

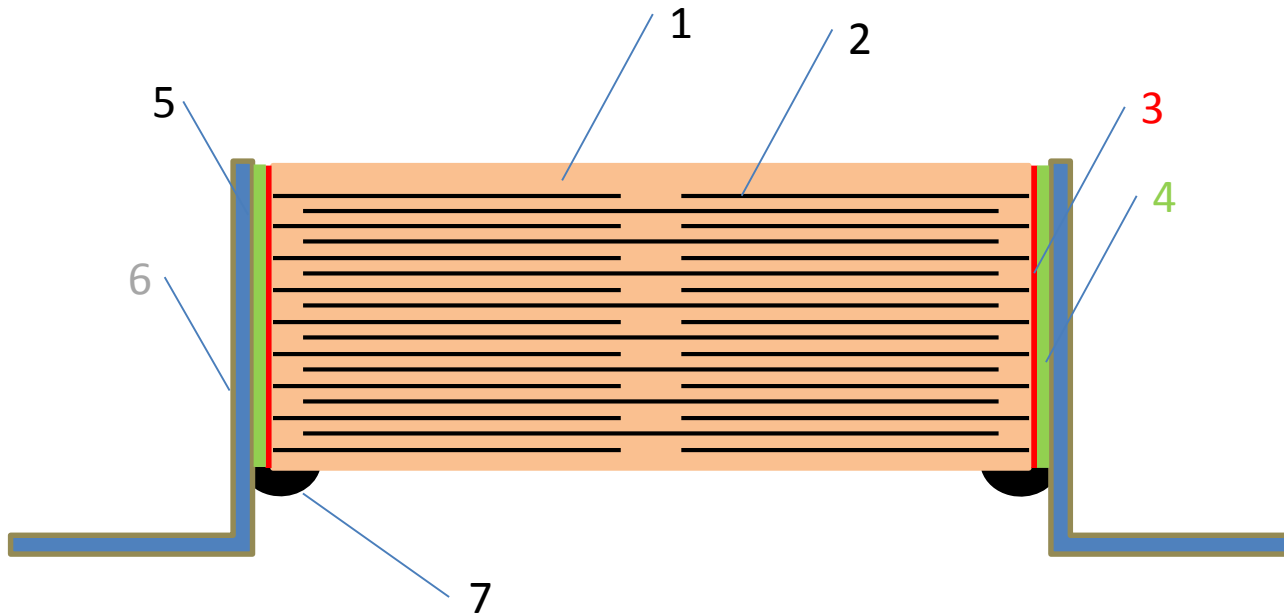
- Low self-inductance (ESL) of 2.5 to 4 nH
- High capacitance density of 2 to 5 $\mu\text{F}/\text{cm}^3$
- High thermal robustness allows PLZT to be placed very close to the semi-conductor with operation up to 150 °C permissible

System-enabled benefits lead to miniaturization

- **Lower voltage overshoot** during semiconductor switching
- **Faster switching with higher di/dt and dv/dt values** decrease the switching losses
- Higher switching frequencies achievable



Typical Ceramic based PLZT Capacitor Construction

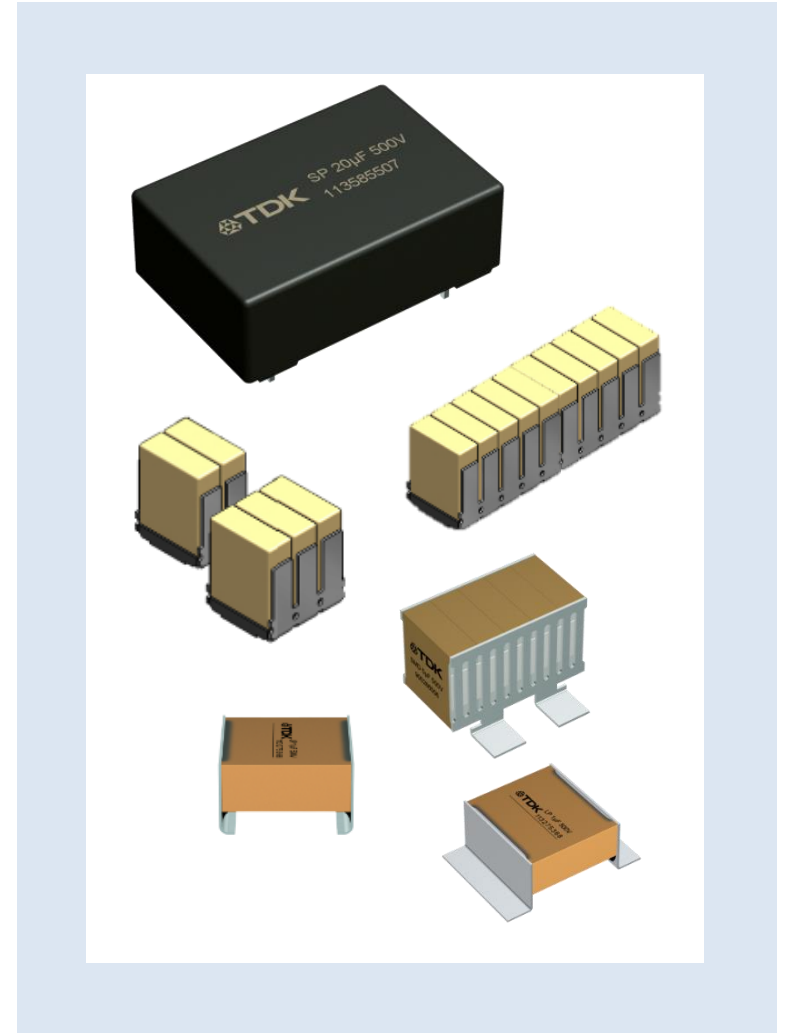


nr.	name	material
1	Dielectric ceramic	PLZT
2	electrode	Cu
3	sputter layer	Cr Ni Ag
4	sinter silver	Ag
5	lead frame	Cu Fe Ni
6	coating	Ag
7	adhesive	epoxy resin



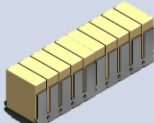
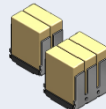

Summary

Key benefits of PLZT

- Effective capacitance increases with rising voltage and leads to **high capacitance density**
- **Low ESL** and low inductive connection
- **Low ESR** especially at high frequencies and high temperatures
- **High current density**
- **High operating and peak temperatures** with temperature excursions up to 150°C
- **High robustness against high temperatures**
- Supports **fast-switching semiconductors** and high switching frequencies
- Supports further **miniaturization** of power electronics at the system level



Device portfolio

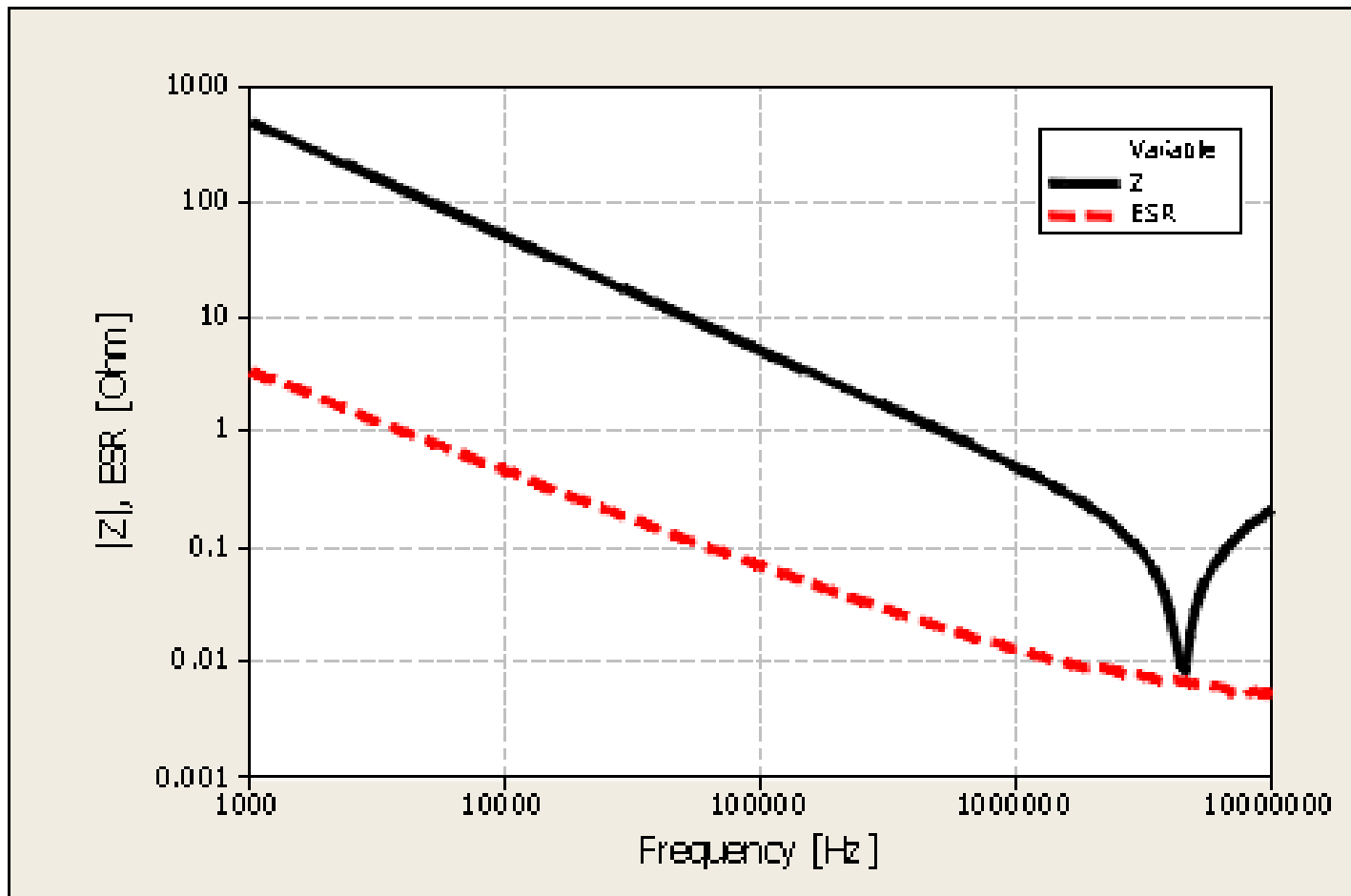
Nominal capacitance / rated voltage		Designed for 650V semiconductors	Designed for 900V semiconductors	Designed for 1300V semiconductors
Low Profile series LP (L leads)		1μF / 500V Released	0.5μF / 700V Released	0.25μF / 900V Released
Low profile series LP (J leads)		1μF / 500V Released	0.5μF / 700V Released	0.25μF / 900V Released
Flex Assembly FA10		10 μ F / 500V Samples available	5 μ F / 700V Samples available	2.5 μ F / 900V Samples available
Flex Assembly FA2 / FA3		2/3 μ F / 500V Samples available	1/1.5 μ F / 700V Samples available	0.5/0.75 μ F / 900V Samples available
Solder Pin series SP		20μF / 500V Released	10μF / 700V Released	5μF / 900V Released

All products shown share the same ceramic material. Different voltage performance is adjusted by internal layer thickness.



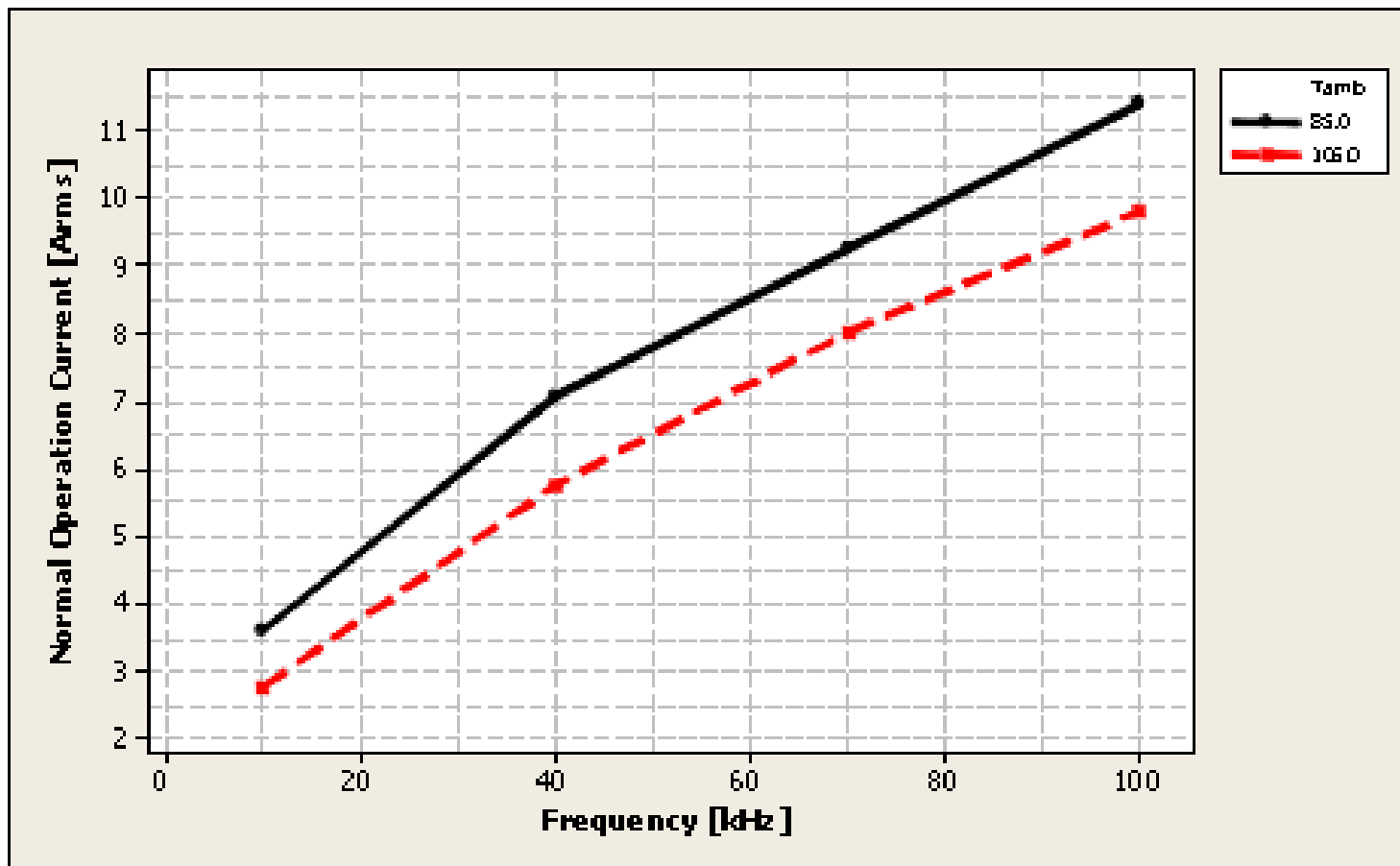
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Typical Impedance and ESR vs Frequency



$V_{DC} = 0\text{ V}$, $V_{AC} = 0.5\text{ V}_{RMS}$, $T_{device} = 25\text{ }^{\circ}\text{C}$

Typical permissible current vs frequency



Measurement performed at V_{op} .
 The values correspond to a device temperature
 of 150 °C.
 No forced cooling was used.