

Title slide for presentation given at the Industry Session of the 2013 APEC Conference.


**120 Hz Power Filtering
using
Electric Double Layer Capacitors**

John R. Miller
JME, Inc. and Case Western Reserve University
23500 Mercantile Road, Suite L
Beachwood, OH 44122
jmecapacitor@jmi.net
216-995-9630

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JME 2013 Applied Power Electronics Conference



120 Hz Power Filtering

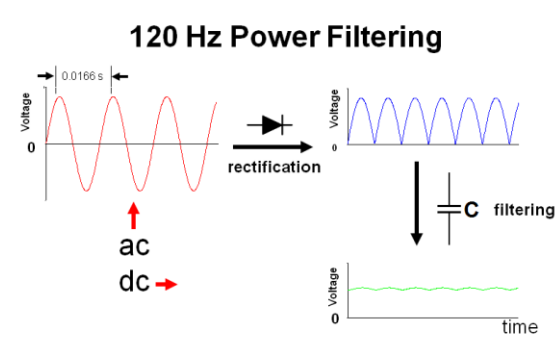
- **Aluminum electrolytic capacitors are the present solution**
 - Often the largest component
 - Usually the component with the lowest reliability
- **Electric double layer (EDLC) with 120 Hz performance may--**
 - Reduce the volume of the power electronics
 - Increase system reliability

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Introduction and motivation for development of an electric double layer capacitor that can provide 120 Hz power filtering

120 Hz Power Filtering

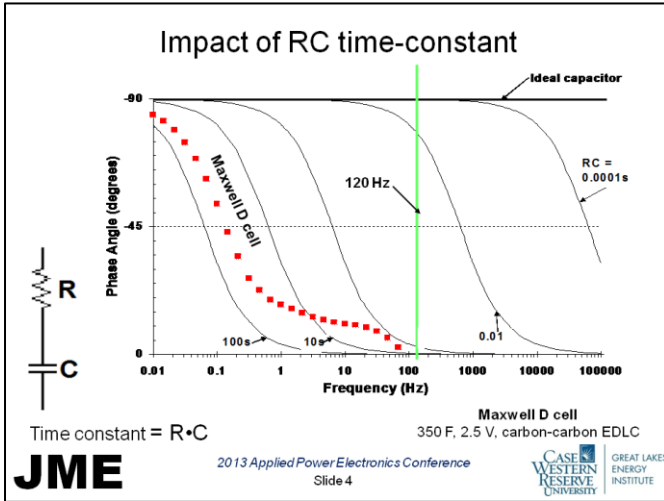


ac line filtering removes ripple to create pure dc voltage

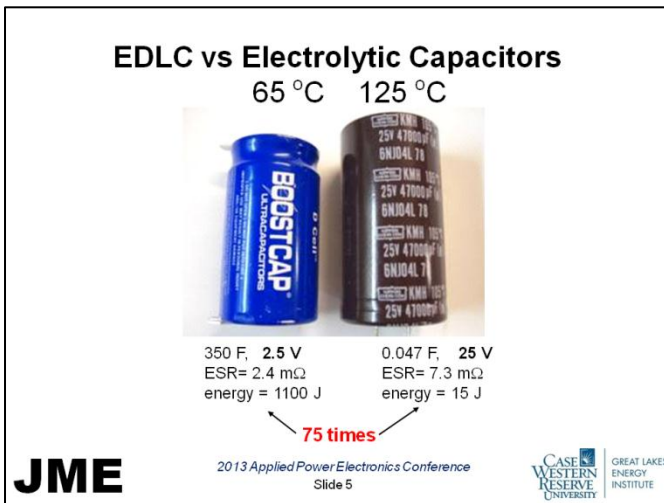
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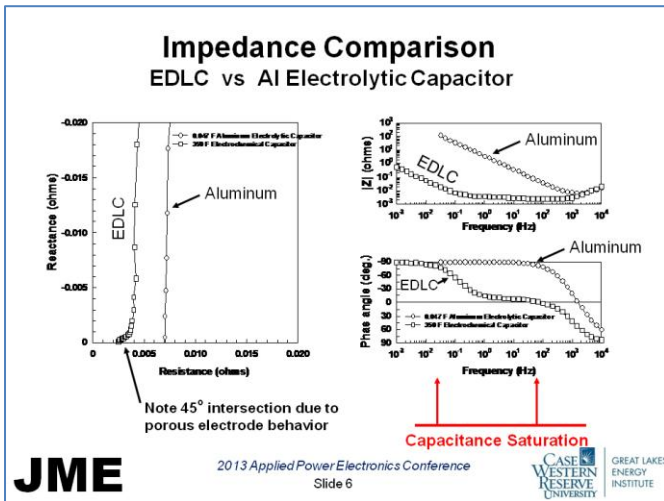
120 Hz power filtering means converting ac “wall power” to dc power to run modern portable electronic equipment such as laptop computers, cell phones, or personal data assistants. The conversion process involves diode rectification followed by removal of voltage fluctuations followed by filtering with a capacitor.



An ideal capacitor has a 90-degree phase angle between voltage and current at all frequencies. A series resistance produces changes as shown. For an RC product of 0.01 seconds, the -45 degree phase angle is reached at about 1 kHz and the -90 degree value reached at about 10 Hz. Thus, one needs to have $RC \ll 0.01$ seconds to efficiently filter 120 Hz power. The red dots are phase angle measurements from a 350 F state of the art commercial EDLC, showing that no filtering is achieved at 120 Hz.



Capacitors of the same approximate physical size comparing two different technologies. The EDLC has smaller ESR and stores 75 times more energy than the electrolytic capacitor, yet it has no 120 Hz power filtering capability.



Complex plane plot (left) comparing the two technologies. Note the aluminum electrolytic capacitor shows no porous electrode behavior (vertical behavior on the left figure.) Note the aluminum electrolytic capacitor maintains negative 90 degree phase angle at greater than 120 Hz.

Equivalent circuit models of the two technologies. The EDLC model has three time constants.

Equivalent Circuit Model Comparison

25 V Electrolytic 0.047 F	2.5 V EDLC 350 F
------------------------------	---------------------

$R_1 C_1 \approx 250 \text{ ms}$
 $(R_1 + R_2) C_2 \approx 340 \text{ ms}$
 $(R_1 + R_2 + R_3) C_3 \approx 900 \text{ ms}$

$RC \approx 0.3 \text{ ms}$

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Attractive features of EDLCs and an approach for making an EDLC that can perform power filtering.

Electric Double Layer Capacitor (EDLC)

- Exceptionally high capacitance density
- Achieved by use of highly porous electrodes
- Porous electrodes creates distributed charge storage
=> limited frequency response ($RC \sim 1 \text{ s}$)
- EDLCs typically rated at $<85^\circ\text{C}$ operation

Question:
How can an EDLC be made to operate at 120 Hz?

Answer:
Reduce series resistance (ionic and electronic)
Eliminate distributed charge storage (single time constant)

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Cross section of a hypothetical electrode used to develop impedance response equations. This work was originally performed by De Levie and published in 1963.

Impact of high-surface-area electrode material

De Levie Porous Electrode Model

Cross-sectional view of the model used to represent a porous electrode: the electrode surface is supposed to consist essentially of circular cylinders of radius r . The influence of the cylinder ends and of the macroscopic, external surface is neglected.

De Levie, Electrochim Acta. 8, 751 (1963)

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Impact of high-surface-area electrode material

Porous Electrode--Transmission Line Response

A small section dx of the equivalent circuit of a pore with uniformly distributed solution resistance R and double layer capacitance C , both per unit pore length

$$Z_p = \frac{(1-f)}{2\pi\sqrt{r^3\kappa\omega C_{dl}}} \coth \left[l \sqrt{\frac{\omega C_{dl}}{\kappa r}} (1+j) \right]$$

Where $j = (-1)^{1/2}$
 n = number of pores in the electrode
 r = radius of a cylindrical pore
 κ = electrolyte conductivity
 ω = angular frequency
 C_{dl} = double layer capacitance per unit area
 l = length of a cylindrical pore

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This is the Impedance of the hypothetical porous electrode shown in the previous figure. The response has transmission-line characteristics and is dependent on the parameters as listed.

Sources of EDLC Series Resistance (Cell Cross-section)

Electronic resistance
 current collector
 electrode material
 contact resistance

Ionic resistance (electrolyte)
 separator
 porous electrode

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Here is a typical EDLC cell cross section showing two identical electrodes separated by a separator. Current collectors contact each electrode. The sources of resistance are identified and must be minimized to achieve high-frequency EDLC operation.

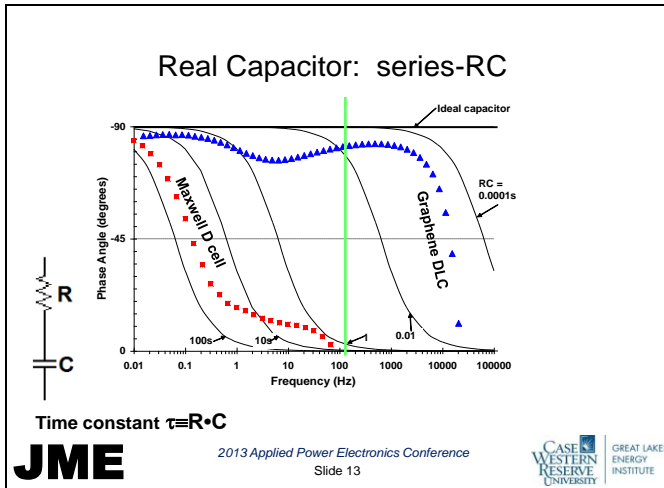
Graphene Double-Layer Capacitor with ac Line-Filtering Performance

John R. Miller,^{1*} R. A. Outlaw,² B. C. Holloway³ SCIENCE VOL 329 24 SEPTEMBER 2010

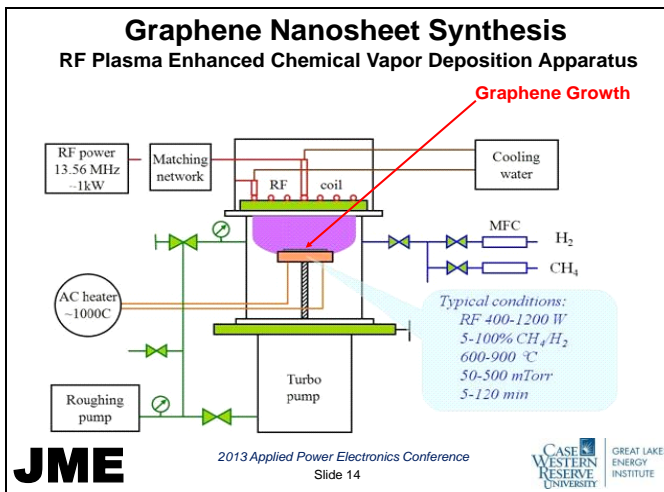
No distributed charge storage behavior

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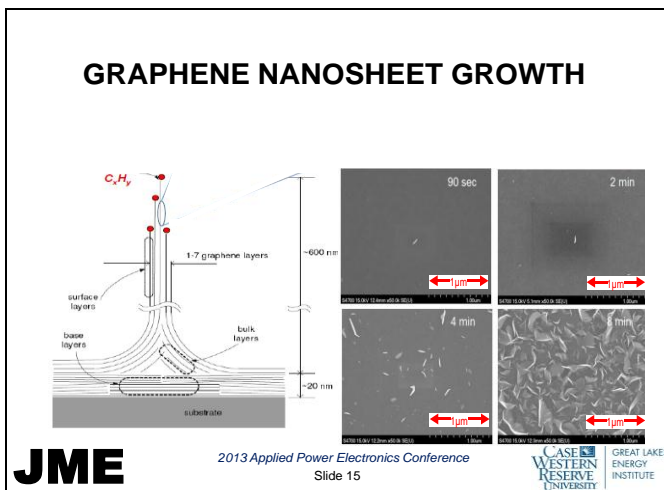
This highlights previous publication title and citation, SEM plan view of a vertically oriented graphene nanosheet electrode, and complex plot of the measured impedance. The nanosheets are approximately 1 micrometer tall on a nickel substrate. No porous electrode behavior was observed.



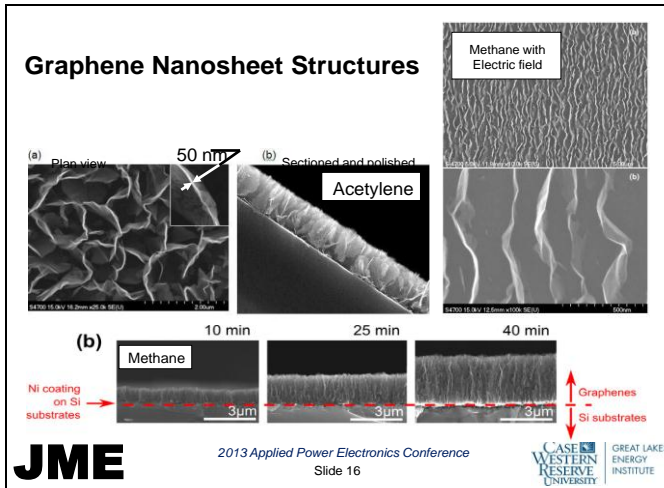
Here is a modification of slide 4 with additional plot of graphene DLC. The commercial EDLC is in red, the vertically oriented graphene nanosheet electrodes (blue), and the series-RC model calculations.



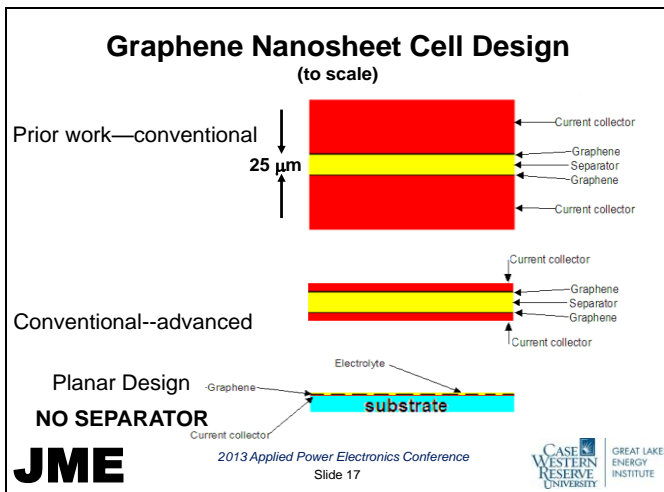
Apparatus used to synthesize the vertically oriented graphene nanosheets used for the EDLC electrodes. RF energy is used to decompose a hydrocarbon gas like methane and deposit carbon atoms.



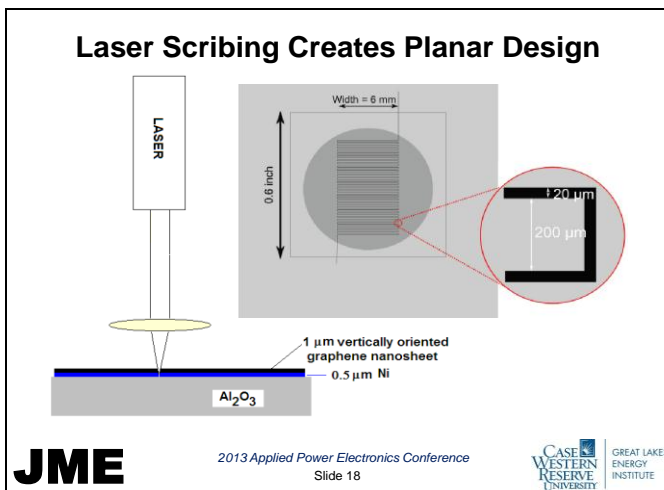
This shows the sequence of graphene nanosheet growth. Decomposed carbon deposits on the nickel substrate where it forms thin islands that increase in size until they eventually impinge on each other and turn upward and then continue to grow vertical (off the surface).



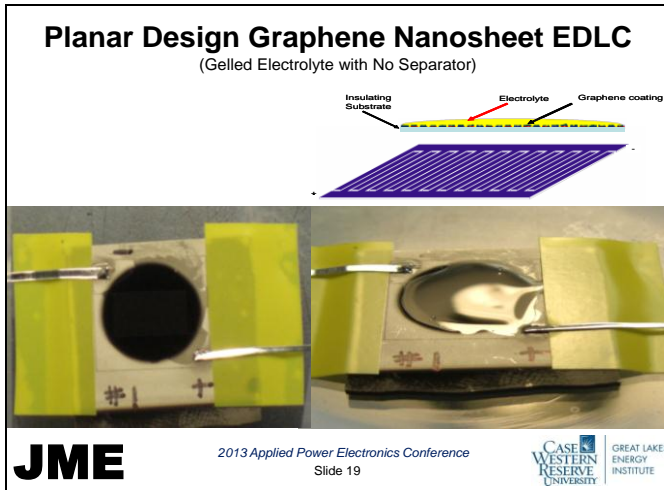
Process conditions dictate the graphene nanosheet structure. Application of an electric field can cause alignment as shown.



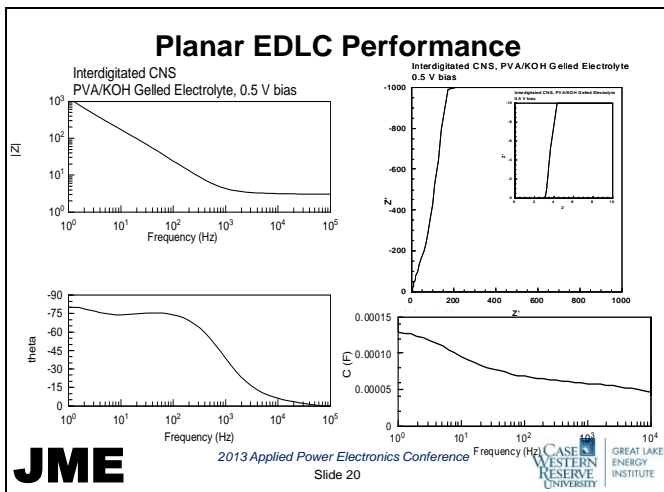
Here is a schematic of capacitor device using the graphene nanosheet electrodes. The top figure shows low volume efficiency—the graphene is less than 1% of the total volume. The middle figure shows higher volume efficiency through use of thinner metal substrates. The bottom figure shows a planar design with no separator, which has even higher volume efficiency.



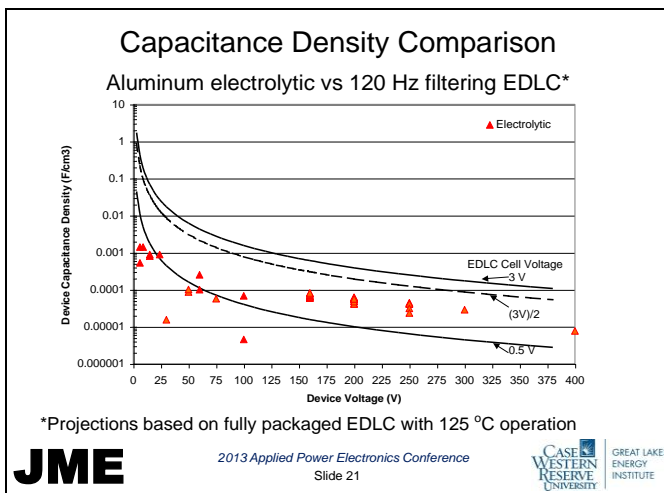
Laser scribing was used to cut an interdigitated pattern on the graphene surface and through a 0.5-micrometer thick nickel layer under the graphene, all on an insulating substrate. The laser-cut lines are 20 micrometers wide and make two electrodes.



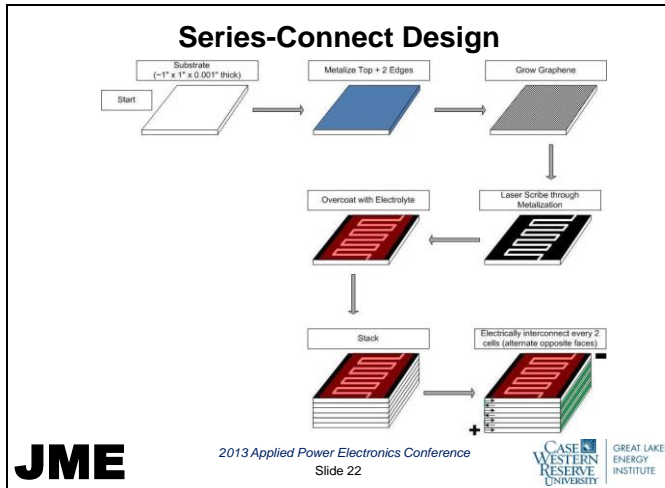
Here is the interdigitated pattern before and after application of a gelled electrolyte. This electrolyte covers the voids and the graphene structure to create a single cell electric double layer capacitor.



Impedance measured on the planar EDLC using a gelled electrolyte. No porous electrode behavior is observed.



Red triangles represent locations of commercial aluminum electrolytic capacitors on this capacitance density versus voltage plot. Planar EDLC predictions for a fully packaged EDLC are the lines shown, for cells operating at 0.5, 1.5 and 3 V per cell. Note that the 1.5, and 3.0 V EDLC lines are above the red triangles, i.e. the EDLC has higher capacitance per volume than the commercial aluminum electrolytic capacitors.



This details a possible sequence for connecting planar cells in series to achieve higher voltage operation. Each element might be 0.02" thick glass covered by nickel, graphene, and electrolyte then stacked.

SUMMARY

- 120 Hz power filtering demonstrated using electric double layer capacitance
- Key to fast response is minimization of all resistance elements (ionic and electronic)
- Planar design demonstrated and appears suitable for assembling series-strings of EDLC cells
- Goal is to develop an EDLC power filtering capacitor with ↑ reliability and ↓ volume than Al electrolytic

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Summary slide

Acknowledgment

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 College of William and Mary, Williamsburg, VA

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