FPGA Cost And Efficiency For PV Inverter Power Electronics

APEC 2013
Jason Chiang
Altera Industrial BU
About The Speaker

- Jason Chiang is a senior strategic marketing manager in Altera’s MIC Division-Industrial BU in San Jose, California
- Responsible for developing marketing strategies and FPGA solutions for Smart Grid and industrial automation applications
- Prior to rejoining Altera in 2008, Jason held various product marketing and business development roles at PMC-Sierra, P.A. Semi, Hitachi, and several other semiconductor companies
- Holds a BSEE from Cal Poly, San Luis Obispo
Solar energy growing from $91.6 billion in 2011 to $130.5 billion by 2021
Europe still leads market while growth in U.S. and Asia Pacific
Driven by regional green energy mandates and feed-in-tariffs (FITs)
PV Inverter Preferences, By Type

- Global PV inverters to grow from ~23 GW to over 42 GW by 2015, primarily in residential and commercial
- String inverters expected to dominate inverter types
- Microinverters/power optimizers may capture 15% (~6 GW) of residential by 2015
PV Inverter Emerging Trends

Reliability & Usability

- Fast user interfaces
- More diagnostic functions and communications
- Mobile monitoring of inverters
- Product longevity
PV Inverter Emerging Trends

Reliability & Usability
- Fast user interfaces
- More diagnostic functions and communications
- Mobile monitoring of inverters
- Product longevity

Lower Cost, Increased Efficiency
- Highly efficient multi-level IGBT and wideband gap power topologies
- Advanced digital control & advanced MPPT for efficiency
- Higher switching frequency to enable smaller passive components
- Achieve >20% cost reduction in next generation designs

Grid Compliance
Efficiency & Cost (and Size, Weight)
Reliability & Usability
PV Inverter Emerging Trends

Reliability & Usability
- Fast user interfaces
- More diagnostic functions and communications
- Mobile monitoring of inverters
- Product longevity

Lower Cost, Increased Efficiency
- Highly efficient multi-level IGBT and wideband gap power topologies
- Advanced digital control & advanced MPPT for efficiency
- Higher switching frequency to enable smaller passive components
- Achieve >20% cost reduction in next generation designs

Grid Compliance
- Power quality monitoring & control for commercial/residential
- Grid code compliance for power generation
PV Inverter Design Challenges

Switch Faster
Scalable High Switching Frequency Design

Switch Better
Modular Complex Topologies 3L/5L Control Loop

Switch Cheaper
Reduce Cost in Passive & Heat Sinks (using SiC/GaN)

Efficiency
Reliability
Cost of Ownership

Design Flexibility
Platform Integration Performance

DSP Algorithms
Embedded Processing Evolving Standards

Long Life Cycle

Realm of low-cost FPGAs
Typical PV Inverter Architecture

- Architectures vary by
  - Inverter power topology
  - Control loop complexity

- DSP for MPPT and DC-DC control

- MCU/DSP with (optional) FPGA for DC-AC control

- MCU/DSP architectures running out of bandwidth for next generation designs
FPGA For Platform Scalability

Coprocessor/DSP Offload
- Reuse hardware/software
- Offload to FPGA to speed up complex control loops
- Integrate and scale PWM channels, I/Os, glue logic

System-on-Chip (SoC)
- SoC integration of control loops, PWMs, I/Os, communications,…
- Embedded processing for real-time & apps. control
- Fewer components for reliability, lower cost

© 2012 Altera Corporation - Public
FPGAs enable Advanced Shade-Tolerant MPPT to sweep for both local and global maxima (channels) to maximize I-V curve

Low-cost DSPs limited to 1-channel MPPT and limited performance

MPPT sample code available
Power Stage – 3L IGBT Cost & Efficiency

- 3-level IGBTs increase inverter efficiency to > 98%
  - Silicon (IGBT & MOSFET) devices are nearing theoretical limits
- Complex control algorithm with 3L IGBTs for efficiency
  - Lower EMI, better voltage quality, less current ripple (vs. 2L IGBTs)
- Higher precision pulse-width modulation (PWM) inverter control for more efficient energy recovery back into the grid
  - DSP technology struggle with 3-level or more level topologies
Power Stage – Wideband Gap Materials

- Wideband gap (WBG) power electronics – SiC, GaN

<table>
<thead>
<tr>
<th>Trend</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Ruggedness</td>
<td>WBG Device</td>
</tr>
<tr>
<td>Higher Switching Frequency</td>
<td>WBG Device</td>
</tr>
<tr>
<td>Higher Breakdown Voltage</td>
<td>WBG Device</td>
</tr>
</tbody>
</table>

Achieve higher efficiency at same level of power topology

Cost/efficiency and power density ideal for 10kW-40 kW inverters
- > 600 V high-voltage inverters (SiC devices still cost more than IGBTs)

Higher switching frequencies (beyond DSP capabilities) to reduce inductive component ratings and cost
Switch Faster/Better – FPGA For DC-AC

Achieve higher efficiency with complex control in FPGA
Achieve higher efficiency with increased switching frequencies
  • ~50% reduction in inductive component costs with 2x increase in frequency with wideband gap material (Source: Fraunhofer)
DSPs struggle with multi-level and special topologies

<table>
<thead>
<tr>
<th>Trend</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Quality Output Sinewave</td>
<td>Performance</td>
</tr>
<tr>
<td>Low Current Distortion (THD)</td>
<td>Performance</td>
</tr>
<tr>
<td>Reduced Reactive Power (cosφ = 1)</td>
<td>Performance</td>
</tr>
<tr>
<td>Overload Protection</td>
<td>Performance</td>
</tr>
<tr>
<td>Compliant to grid codes</td>
<td>Flexible I/O &amp;</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
</tr>
<tr>
<td>Compliant to all standards</td>
<td>Flexible I/O &amp;</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
</tr>
</tbody>
</table>

Three-Phase Topologies with 98% Efficiency

© 2012 Altera Corporation - Public
Silicon Convergence – Best of All Worlds

Mixed System Fabric

- Support for legacy code
- Familiar C-code methodology

Wide Application Scope

- Optimized for DSP operations

Wired Speed Wired Efficiency

- Support for high volume applications
- Application-specific IP

FPGA Domain

- Off-the-shelf availability
- Support for changing standards / reconfigurable systems

DSP

µP

ASIC / ASSP

IP

IP

FPGA
System-Level Benefits of SoC FPGA

Increased system performance
- 4,000 DMIPS for under 1.8W
- Up to 1,600 GMACS, 300 GFLOPS DSP
- >125 Gbps processor to FPGA interconnect
- Cache coherent hardware accelerators

Reduced power consumption
- Up to 30% power savings vs. 2-chip solution

Reduced board size
- Up to 55% form factor reduction
- As few as two power rails

Reduced system costs
- Lower component cost
- Reduction in PCB complexity and cost
  - Less routing with fewer layers
SoC FPGA Example

Notes:
(1) Integrated direct memory access (DMA)
(2) Integrated ECC

© 2012 Altera Corporation - Public
FPGA Tool For DSP System Design

- Move from Simulink model into FPGA design
- MPPT perturb & observe example shown
# Commitment To Long Life Cycles

## Alignment to application lifecycle dynamics

<table>
<thead>
<tr>
<th></th>
<th>R&amp;D (2 – 4 years)</th>
<th>Active (5 – 10 years)</th>
<th>Phase Out (1-3 years)</th>
<th>Obsolete</th>
</tr>
</thead>
<tbody>
<tr>
<td>Military, Industrial, Automotive, Computer, Medical</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **t = 0**
- ASSP: 5 years (typical)
  - Low Prices, Consumer Driven
- MCU: 7-10 years (typical)
  - Low Prices, Embedded Driven
- ASIC: 10 years (typical)
  - High NRE, 100% Application Specific
- Programmable Logic Devices (CPLD, FPGA): 15+ years (typical)
  - Long life, Lower cost of ownership, Off-the-shelf, Wide customer base

### PCN procedure meets or exceeds industry standards (JEDEC, ISO-9000, etc.)

**Example 1:** PV inverters need to last 25 years to match panel warranties

**Example 2:** Average substation equipment (e.g., in NA) is > 40 years old
# PV Inverter Reference Design Example

- State-of-the-art 3-phase/3-level inverter reference design
  - Ideal for 3~ Solar Inverter
  - Reduced current ripple
  - Reduced EMI
  - Reduced passives (size, weight and cost)

- Reasonable 3-Level IGBT resource usage

<table>
<thead>
<tr>
<th>Function</th>
<th>IP</th>
<th>Size</th>
<th>Performance</th>
<th>IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter Control on Cyclone FPGA</td>
<td>MPPT &amp; DC-DC control (Single Channel P&amp;O)</td>
<td>&lt;1K LEs</td>
<td>100 MHz</td>
<td>1x Voltage Sensor 1x Current Sensor</td>
</tr>
<tr>
<td></td>
<td>DC-AC control (Switching Frequency 16kHz, capable up to 50kHz)</td>
<td>14K LEs</td>
<td></td>
<td>PWM (3L IGBTs): 12 Gate Signals 6 Vcc Fault Signals 3 Current &amp; 2 DC Voltage ΣΔ signals</td>
</tr>
</tbody>
</table>
Summary

- Switch Better/Cheaper – Increased efficiency using FPGA control loop & multi-level IGBTs

- Switch Faster/Cheaper – Increased switching frequency and further reduce inductive component costs with FPGAs & wideband gap materials

- Switch Easier – From simulation to FPGA implementation using Simulink to FPGA tool flow

- Manage Life Cycle – FPGAs stay in production for a long time

- Migrate Smoother – Partition hardware/software and recompile IP for next generation FPGAs and SoCs
Thank You