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# Triple Pulse Core Loss testing

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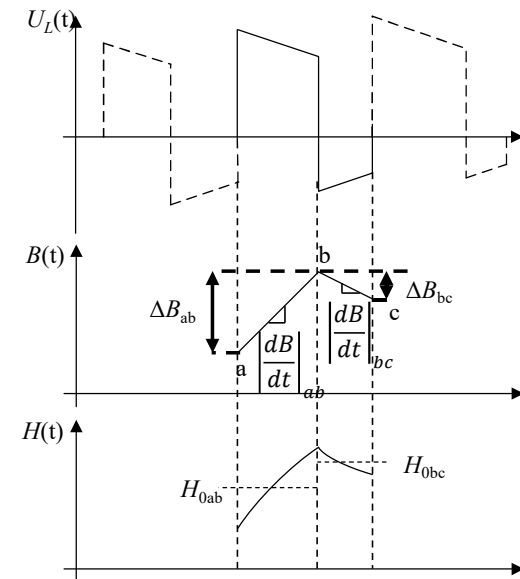
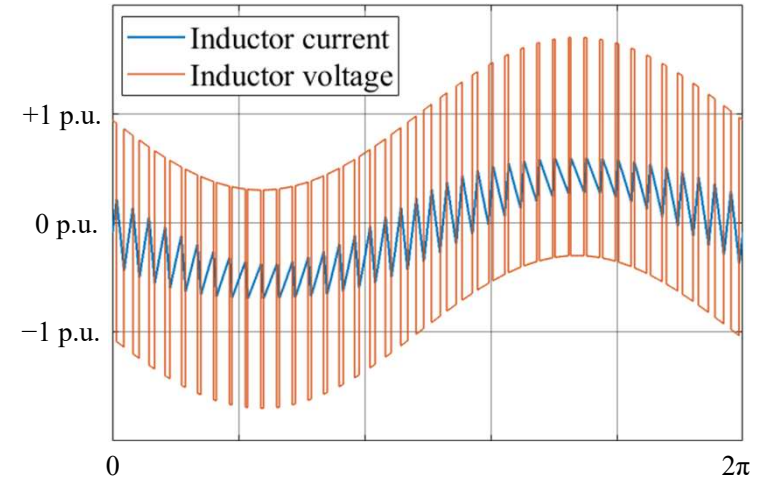
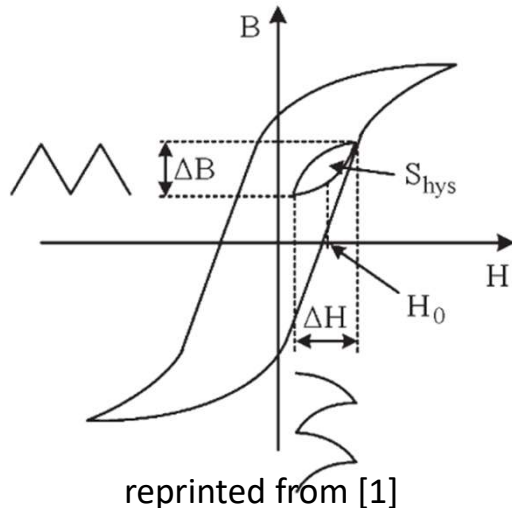
# High-frequency loss of magnetic components in PWM converters

- Inductor loss = core loss + copper loss
- Copper loss
  - Can be accurately predicted by analytical or FEA models
  - Challenging for random conductor placements  
e.g. hand-wound inductors
- Core loss
  - No full physical model due to non-linear magnetization process
  - Rely on empirical data, typically based Steinmetz Equation (SE)  
Steinmetz parameters are frequency-dependent  $P = kf^\alpha \Delta B^\beta$   
Originally for sinusoidal excitations only  
SE + FFT does not work for PWM waveforms due to non-linear effect  
improved Steinmetz Equation (iGSE) neglects the dc-bias effect



# Core loss in PWM converters

- Rectangular voltage
  - Wide-spread frequency components
  - Varying duty cycles
- DC-biased current
  - Pre-magnetization (can cause up to 300% error [5])
  - Floating BH loop



# Testing and estimating core loss from rectangular voltages

- Testing core loss from rectangular voltages

(T. Shimizu, 2009 [1]; C. Sullivan et. al., 2010 [4])

- Avoids the conversion from sinusoidal Steinmetz parameters
- Include dc-bias current in the testing

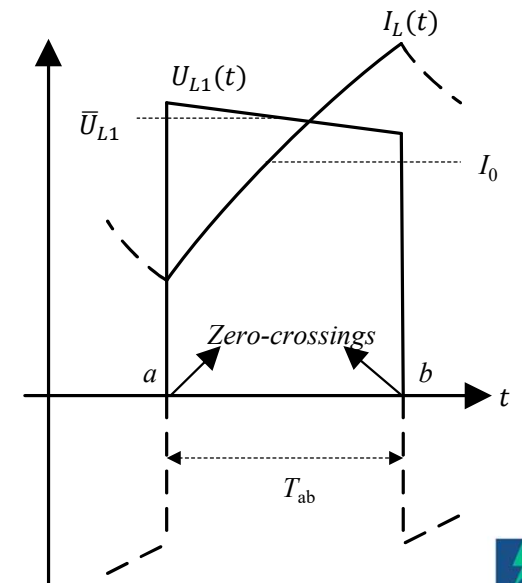
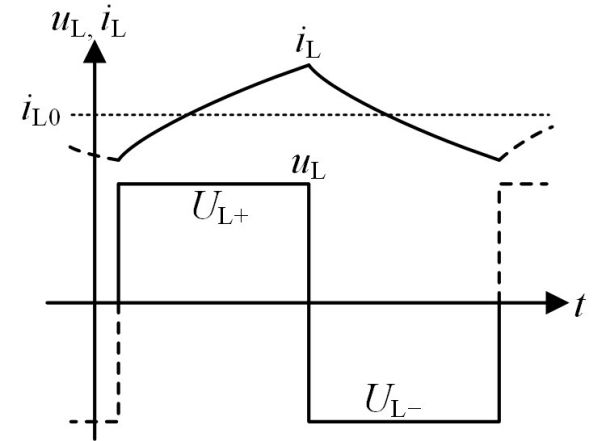
- Testing core loss for one magnetic component

(J. Wang et.al, 2019 [2])

- Performed by the manufacturer
- No geometry information required for core loss estimation
- No conversion for gapped cores
- Include airgap associated losses

- Estimating core loss from rectangular-based data

- Decompose PWM waveform into pulse segments [1],[2]



# Two-winding BH loop testing

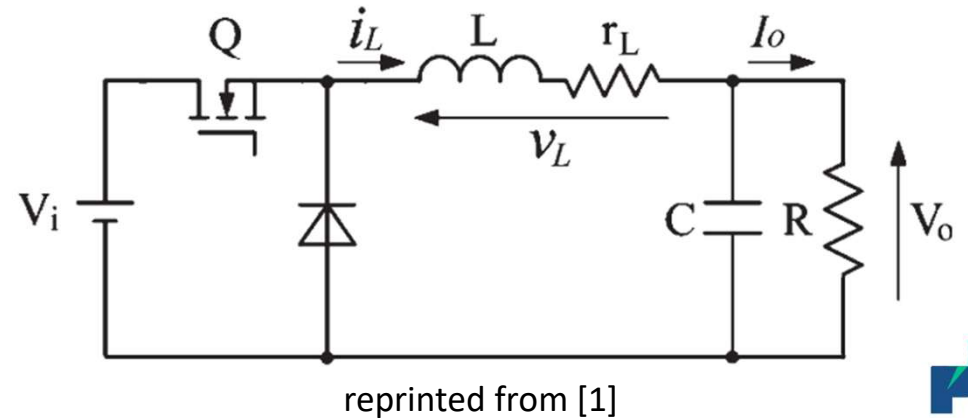
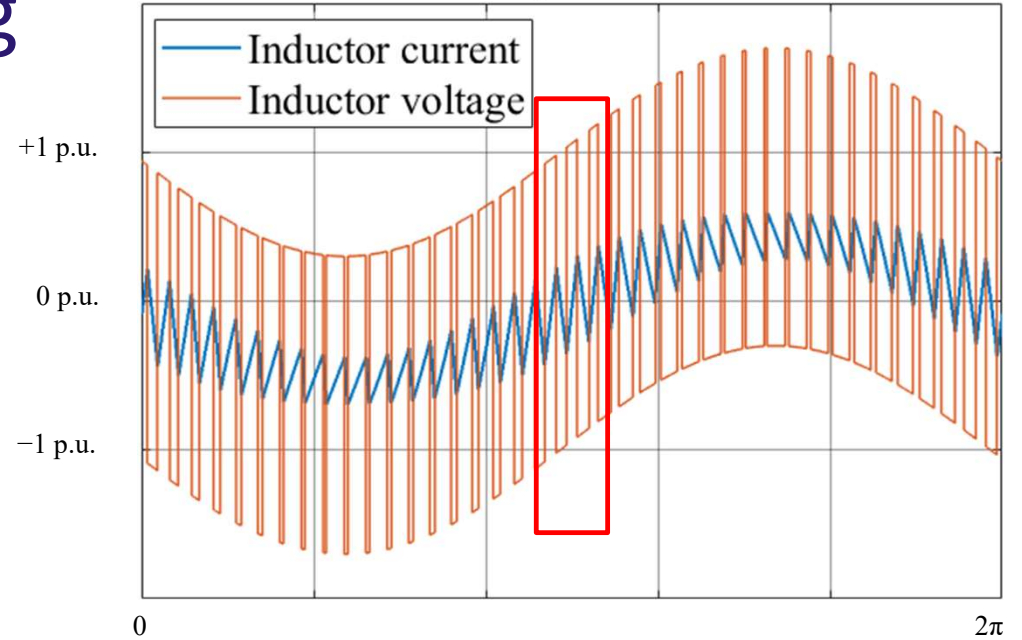
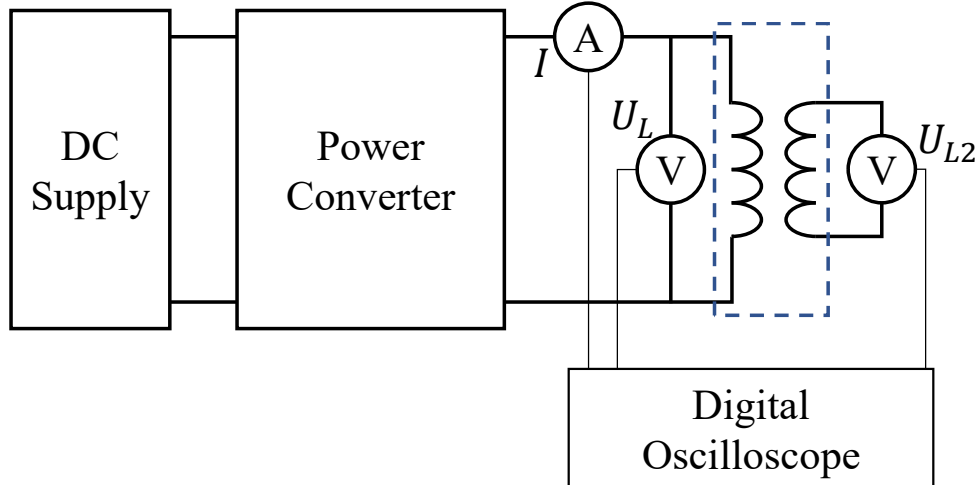
- Two-winding BH loop testing

- Core loss only
- Capture core loss in short transition

$$H(t) = \frac{N_1 \cdot I(t)}{l_e} \quad B(t) = \frac{1}{N_2 A_e} \int_0^t U_{L2}(t) dt \quad (B(0) = 0)$$

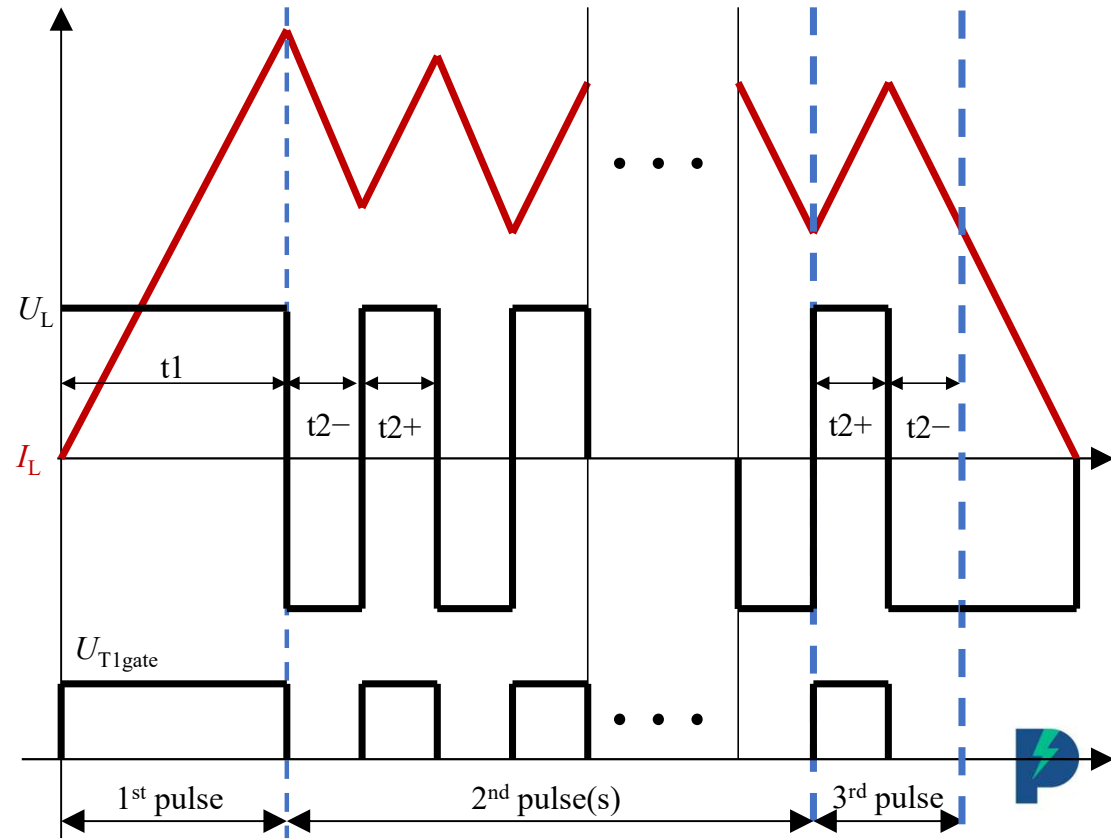
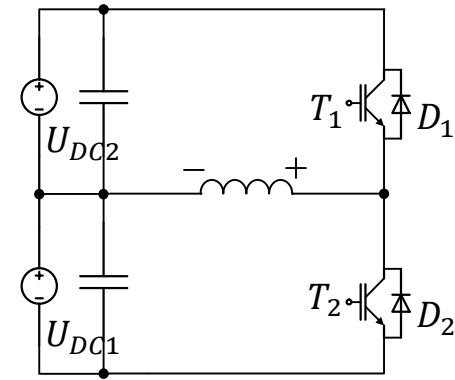
$$S_{hys} = E_{core} = A_e l_e \int H dB = \frac{N_1}{N_2} \int_0^{2T} I(t) \cdot U_{L2}(t) dt$$

Inductor under test



# Testing procedure – Triple Pulse Test

- Discontinuous procedure
  - First pulse – establish dc-bias
  - Second pulse(s) – stabilizing
  - Third pulse – target cycle
- Features
  - Short transition (100 ~ 500  $\mu$ s)
  - Reduced setup requirement
  - Neglectable heat generated
    - reduced cooling requirement
    - constant temperature in testing



# Testing circuit

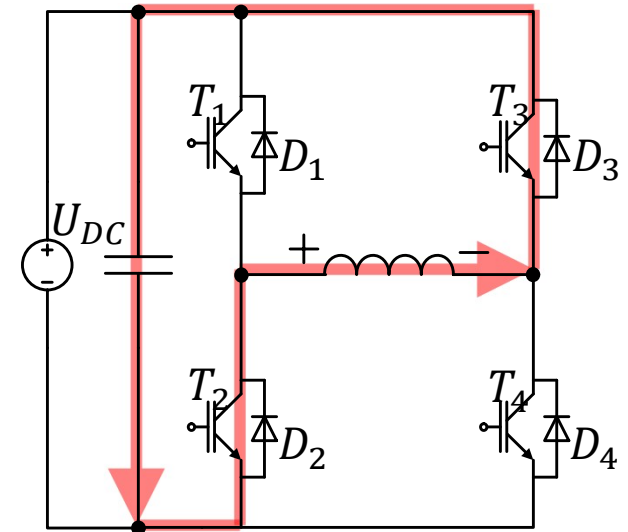
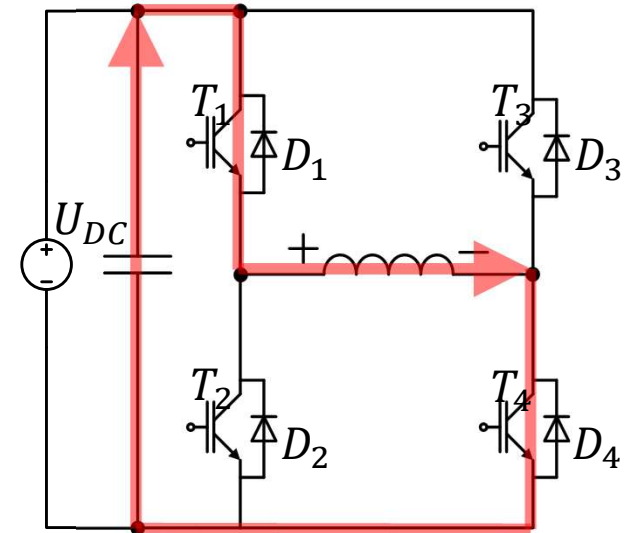
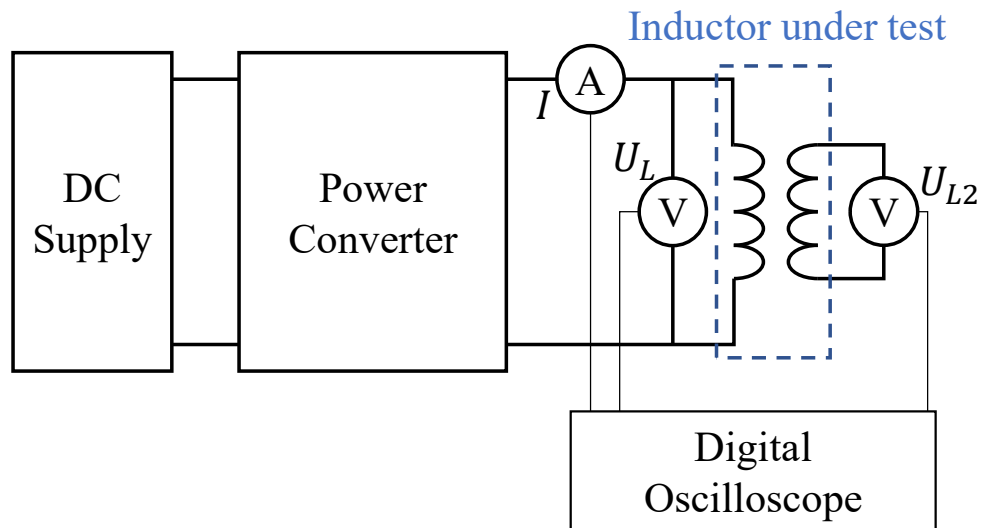
- Full bridge

- $U_{L+} = U_{DC} - 2U_{IGBT}$

- $U_{L-} = -(U_{DC} + 2U_{Diode})$

E.g.  $U_{IGBT} = 3V, U_{Diode} = 2V, U_{DC} = 50V$

$\Rightarrow U_{L+} = 47V; U_{L-} = -52V$



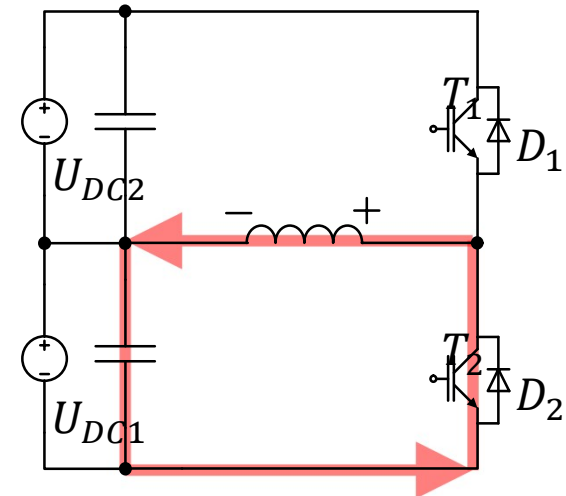
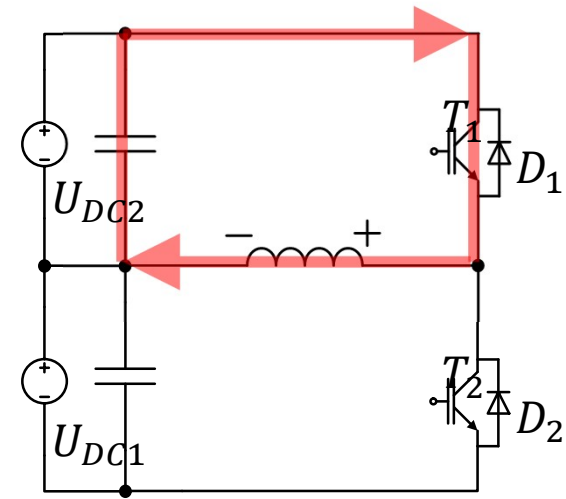
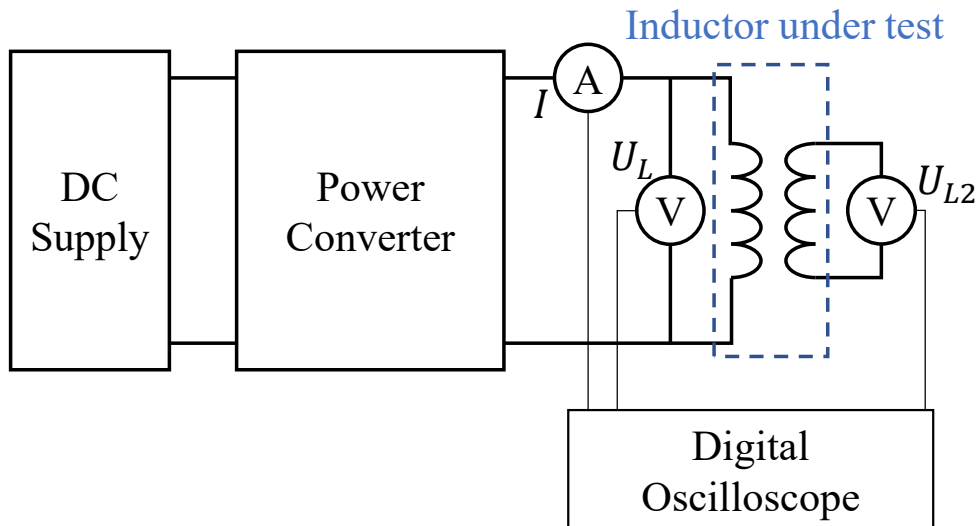
# Testing circuit

- Proposed half bridge

- $U_{L+} = U_{DC2} - U_{IGBT}$

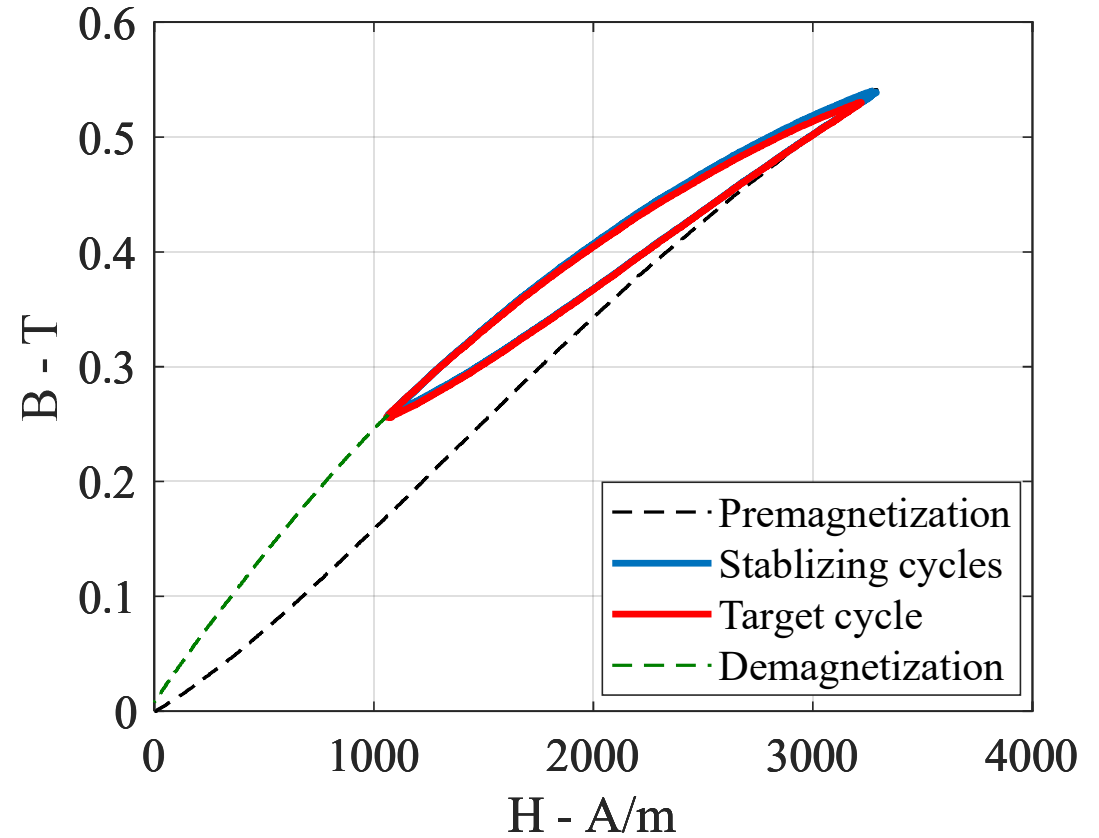
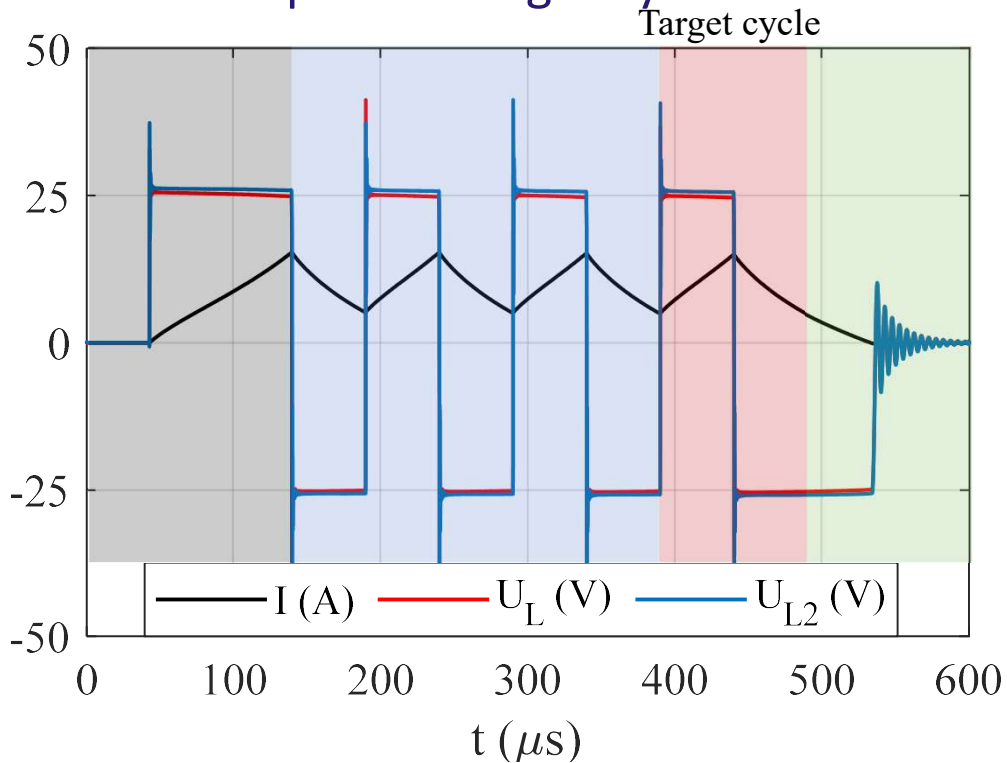
- $U_{L-} = -(U_{DC1} + U_{Diode})$

E.g.  $U_{IGBT} = 3V, U_{Diode} = 2V, U_{DC2} = 53V,$   
 $U_{DC1} = 48V \Rightarrow U_{L+} = |U_{L-}| = 50V$



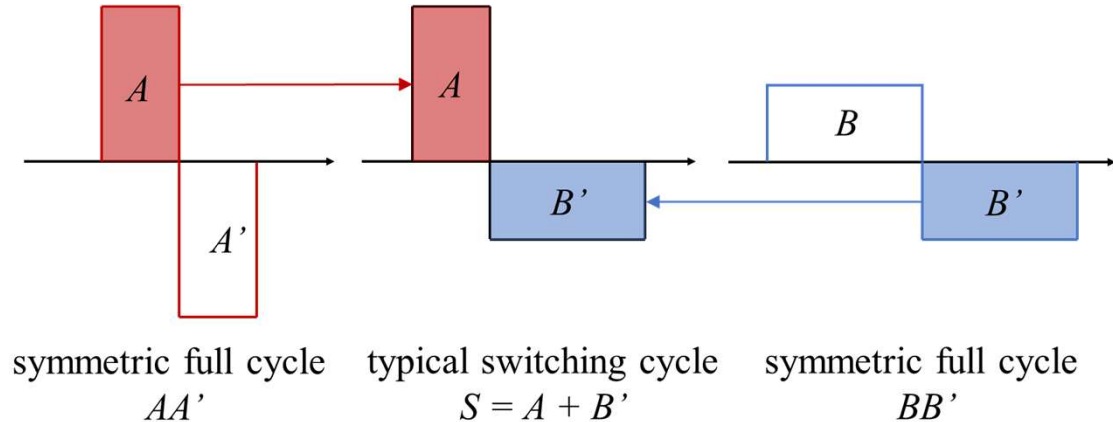
# Testing procedure - example

- Discontinuous procedure
  - First pulse – establish dc-bias
  - Second pulse(s) – stabilizing
  - Third pulse – target cycle

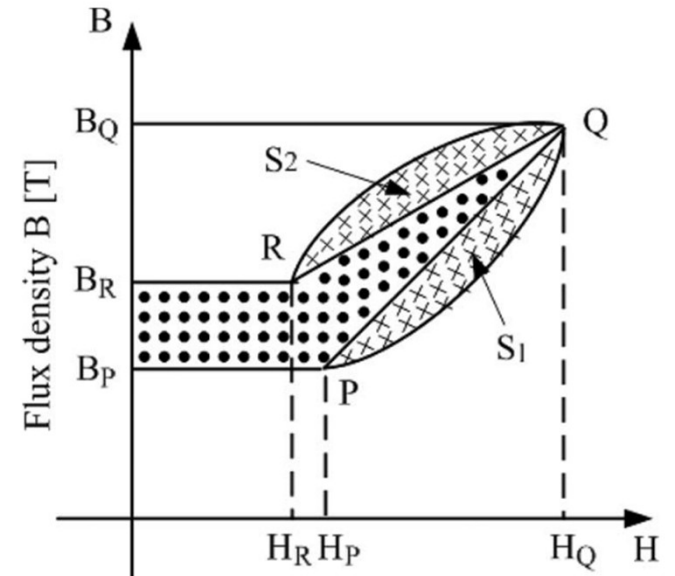
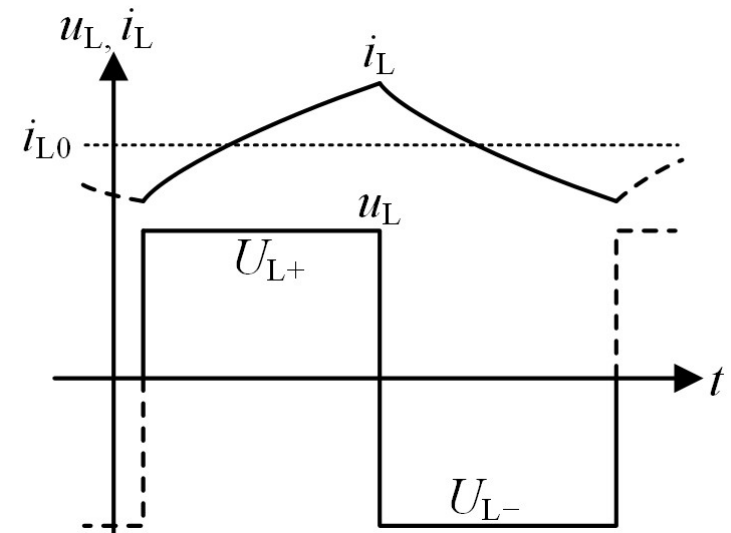


# Practical considerations

- The captured floating BH loop should be closed
  - Only account for real energy loss
  - Foundation of the Composite Waveform Assumption [2],[4]
- Practical considerations
  - Symmetric rectangular excitation voltage
    - Pulse width and amplitude
  - Target cycle should be in the steady state
  - Phase discrepancy and dc offset of the probes



Composite Waveform Assumption

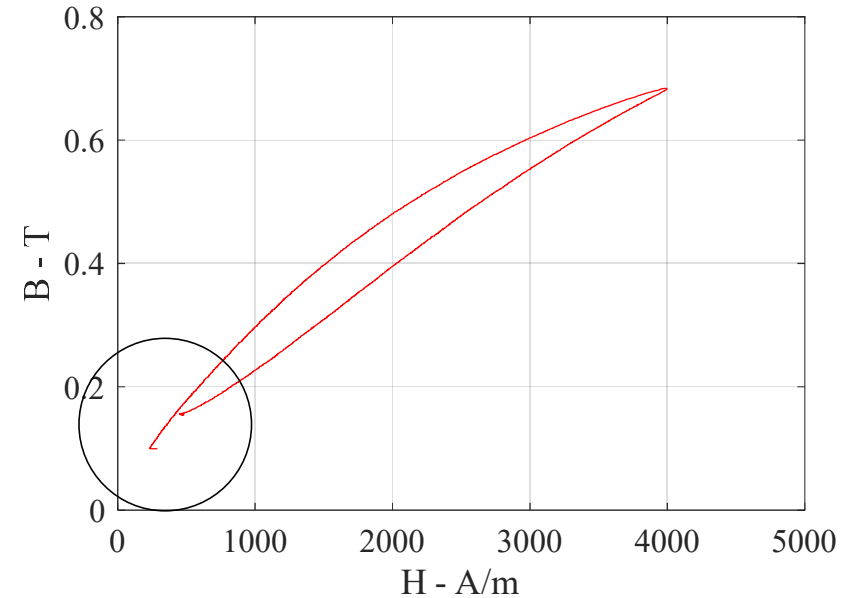
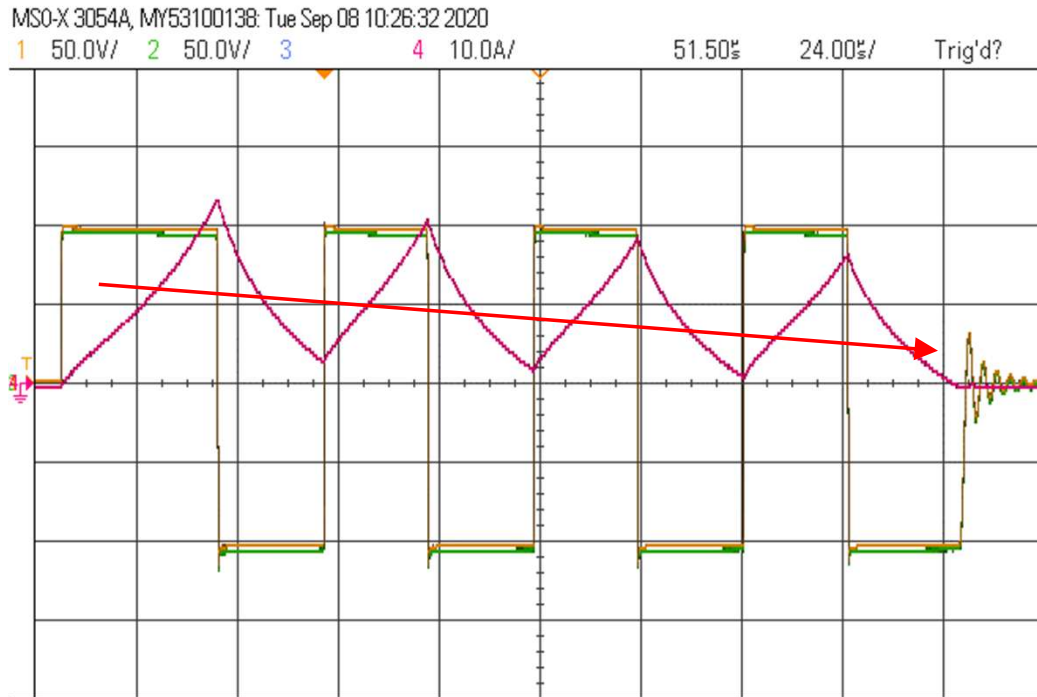


Magnetic field H [A/m]  
reprinted from [1]



# Practical considerations

- E.g. Asymmetric voltage amplitudes due to device voltage drops



$$E = 3.98 \text{ mJ}$$

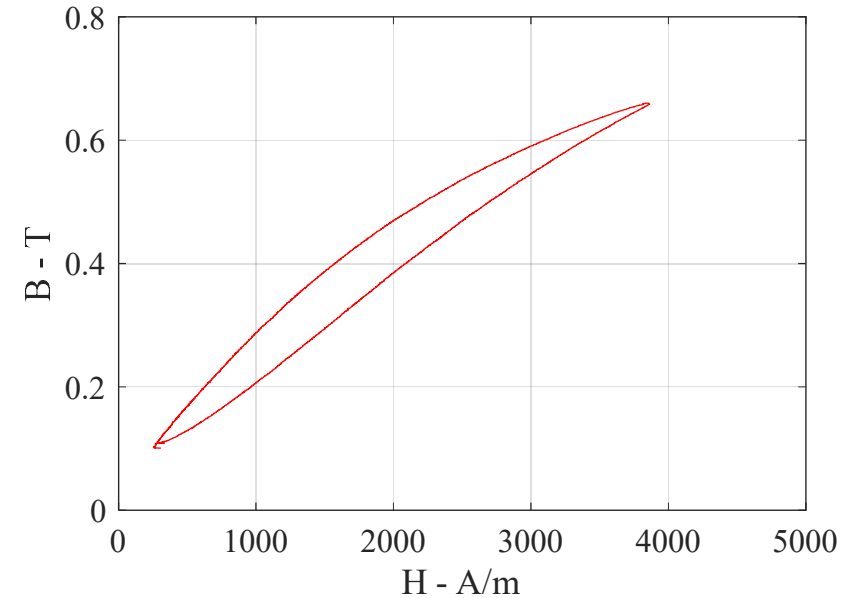
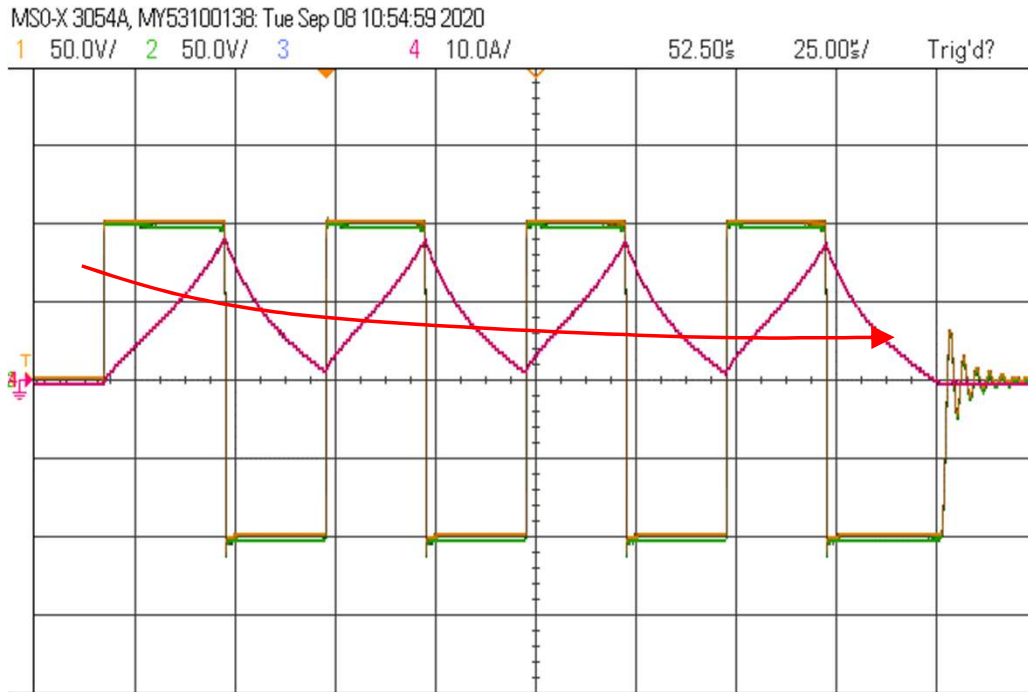
$$U_{L+} = 97 \text{ V}$$

$$U_{L-} = -104 \text{ V}$$



# Practical considerations

- Compensated voltage amplitudes
  - minimize the effect of unclosed BH loop



$$E = 4.44 \text{ mJ (+11\%)}$$

$$U_{L+} = 100 \text{ V}$$

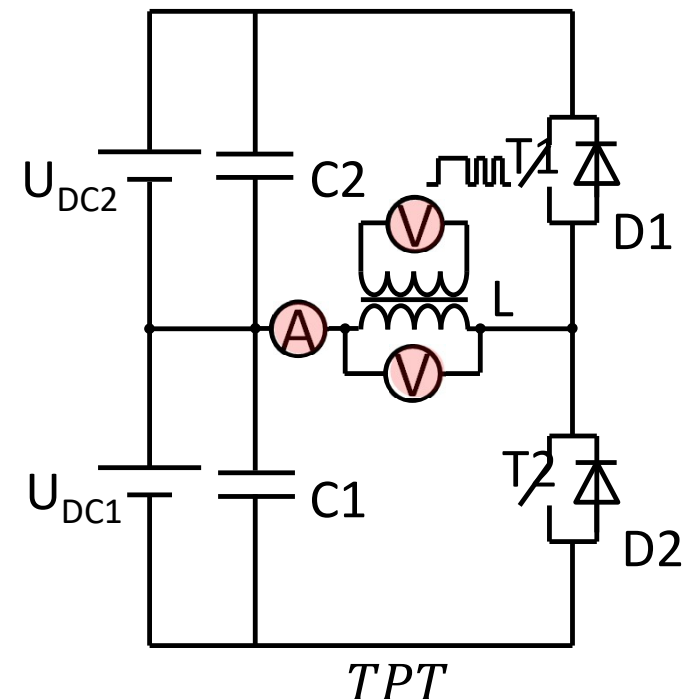
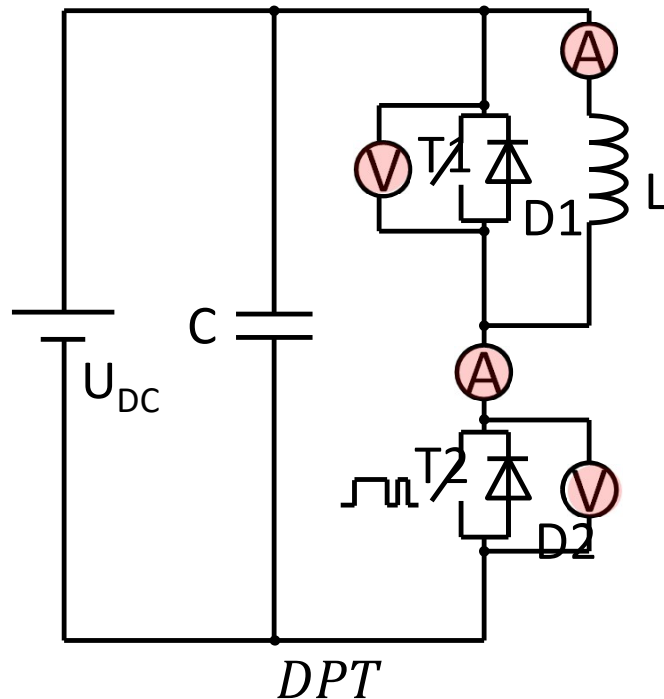
$$U_{L-} = -100 \text{ V}$$



# Analogy to Double Pulse Test

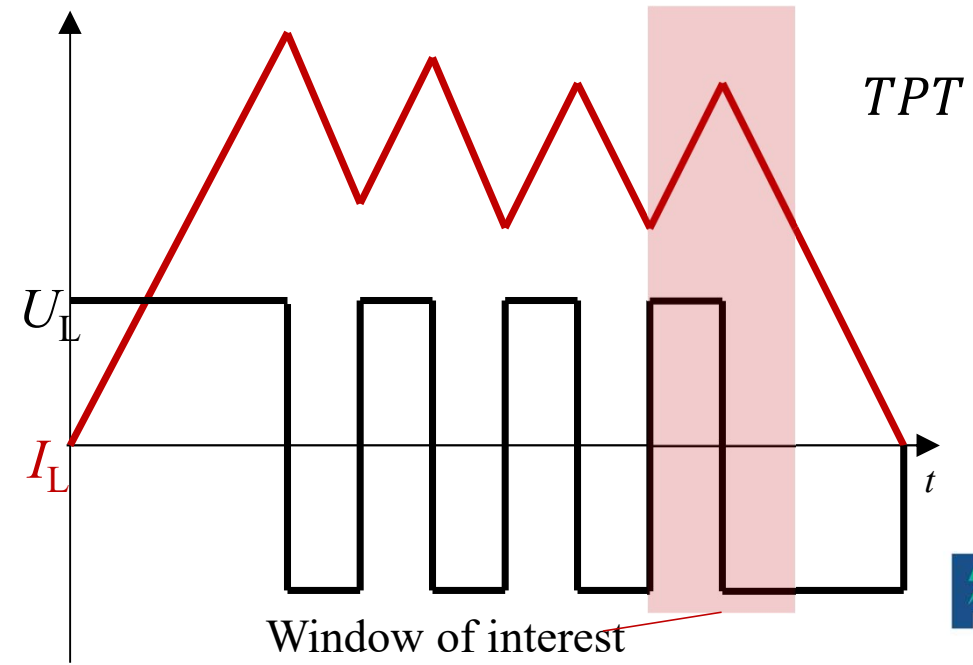
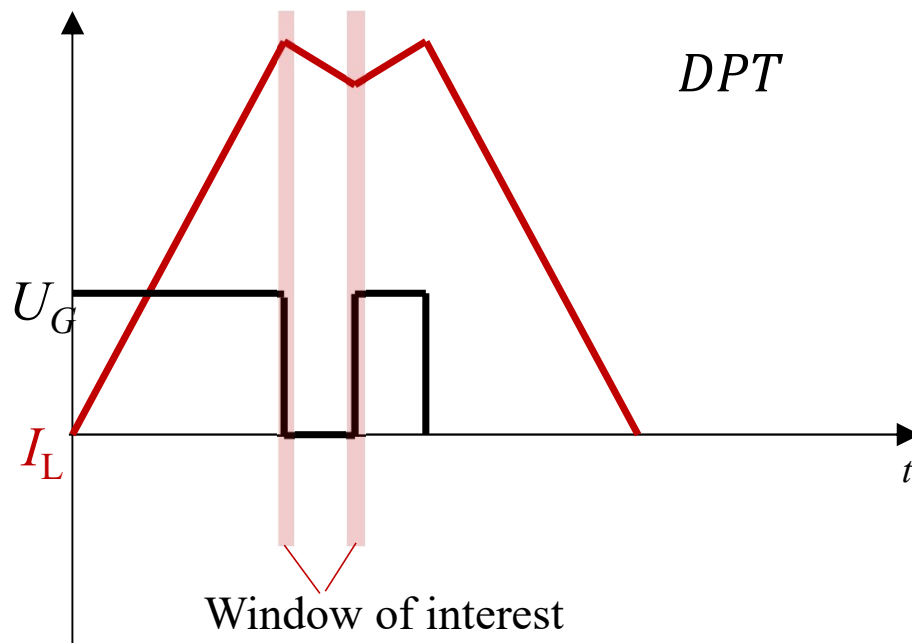
- Testing circuit

- Half bridge configuration
- High-bandwidth current and voltage measurement instruments
- Large dc-link capacitance for transitional current



# Analogy to Double Pulse Test

- Testing circuit
- Testing procedure/waveform
  - discontinuous -> minimized process
  - neglectable temperature rise

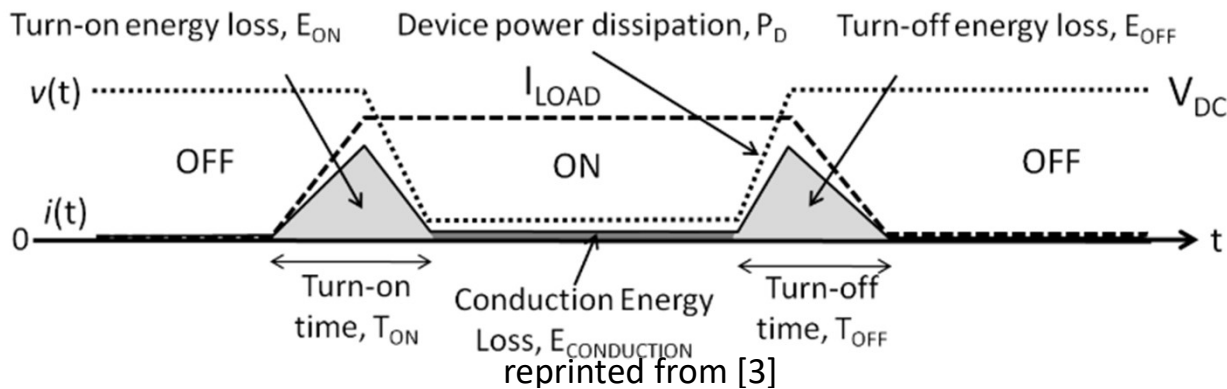


# Analogy to Double Pulse Test

- Testing circuit
- Discontinuous concept
- Generated data pools
  - Three-variable empirical data pools
  - Bypass the need of modelling the transitional waveforms

Switching loss datasheet

$$E_{SW}(mJ) = f(R_G, U_{SW}, I_{SW})$$

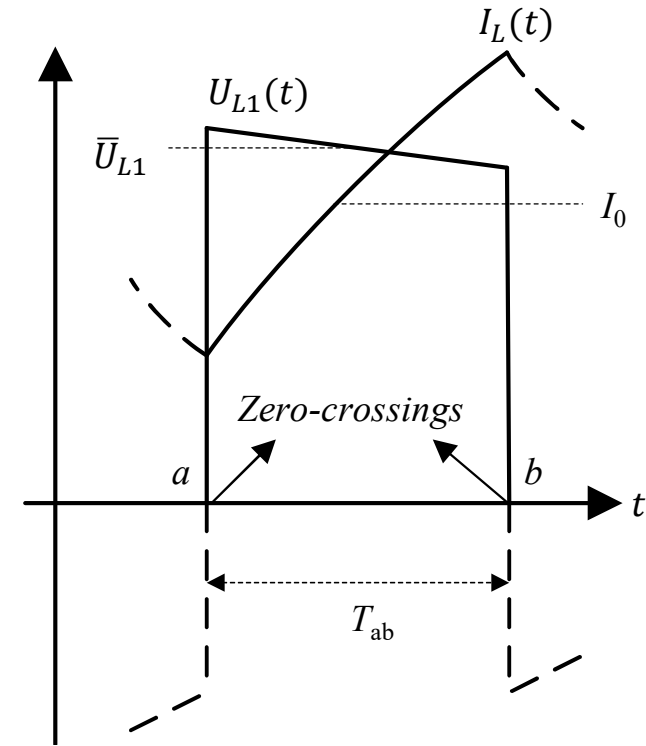


Loss Map [1]

$$E_{core}(mJ) = g(\Delta B, \frac{dB}{dt}, H_0)$$

User-friendly Loss Map [2]

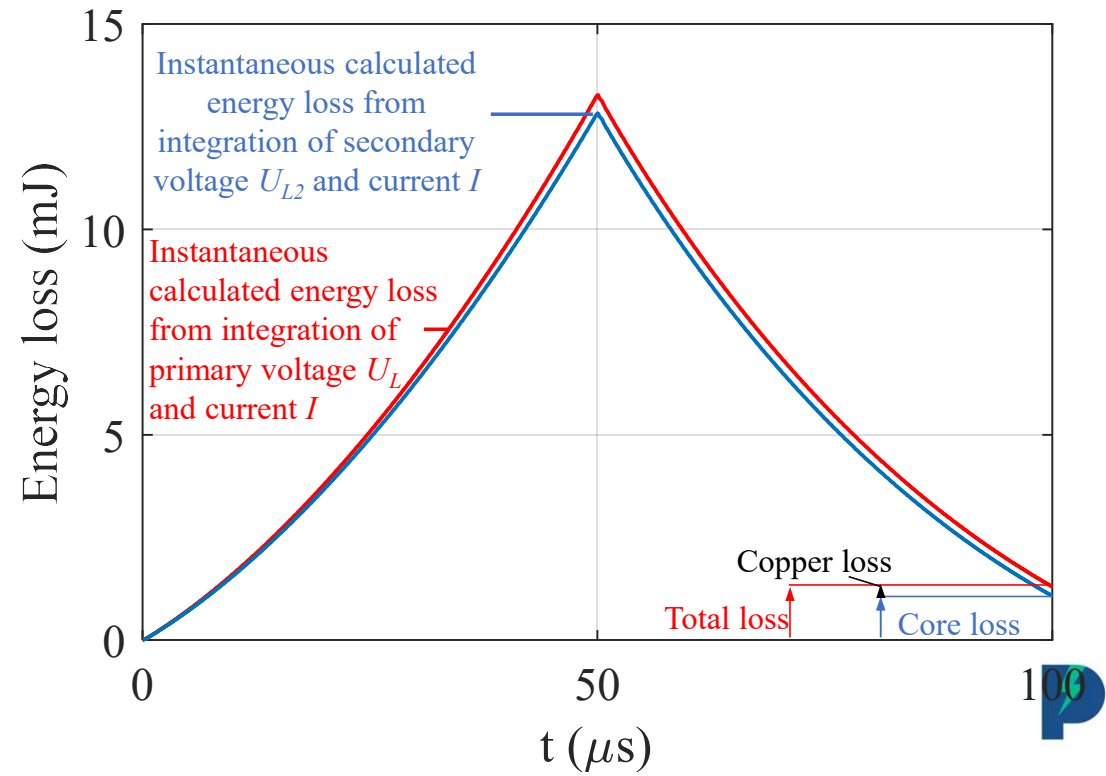
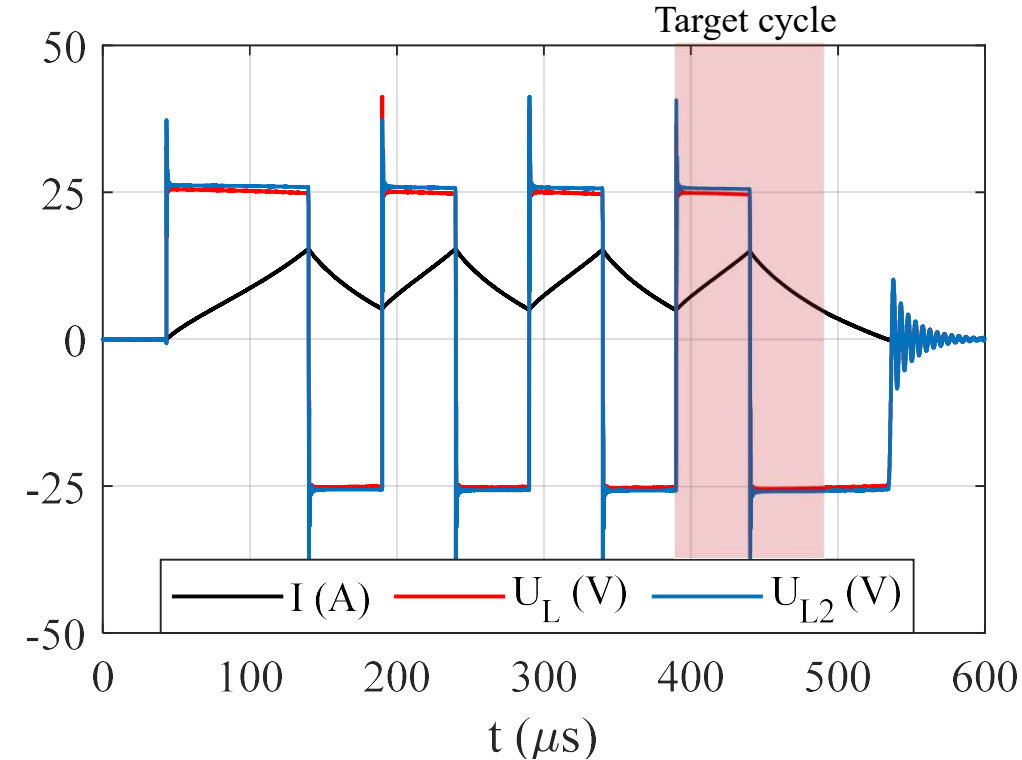
$$E_{core}(mJ) = h(U_L \cdot T, U_L, I_0)$$



# Triple Pulse Test for copper and component loss

- Inductor loss = core loss + copper loss

$$E_{core} = \frac{N_1}{N_2} \int_0^{2T} I(t) \cdot U_{L2}(t) dt \Rightarrow E_{total} = \int_0^{2T} I(t) \cdot U_L(t) dt$$



# Triple Pulse Test for component loss map

## • Component-based Testing

- Fixed core geometries and materials
- Fixed winding placement

## • Component loss map

- Core loss

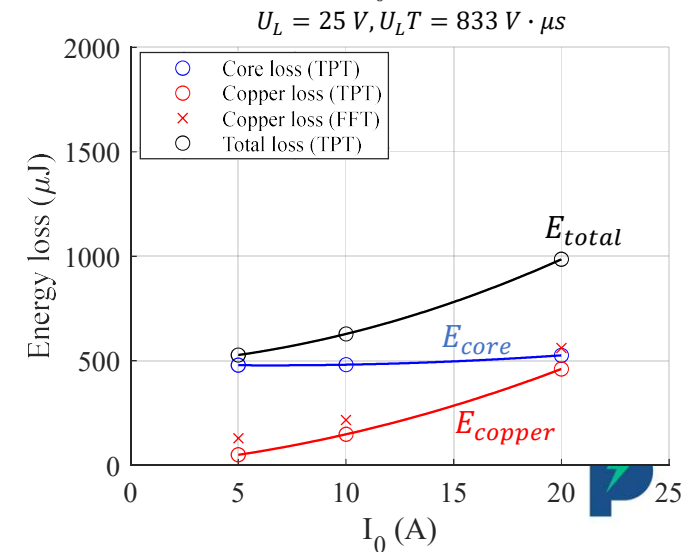
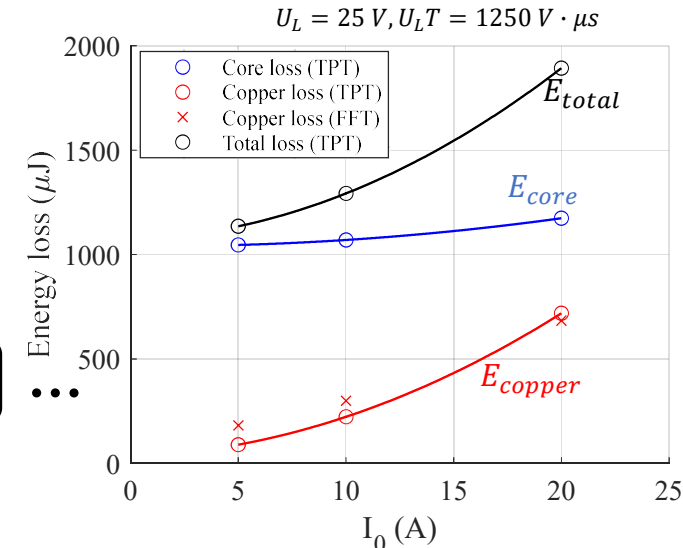
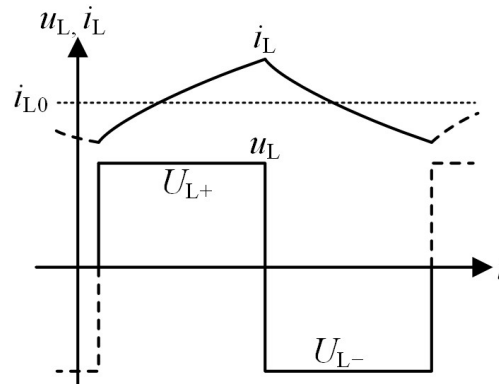
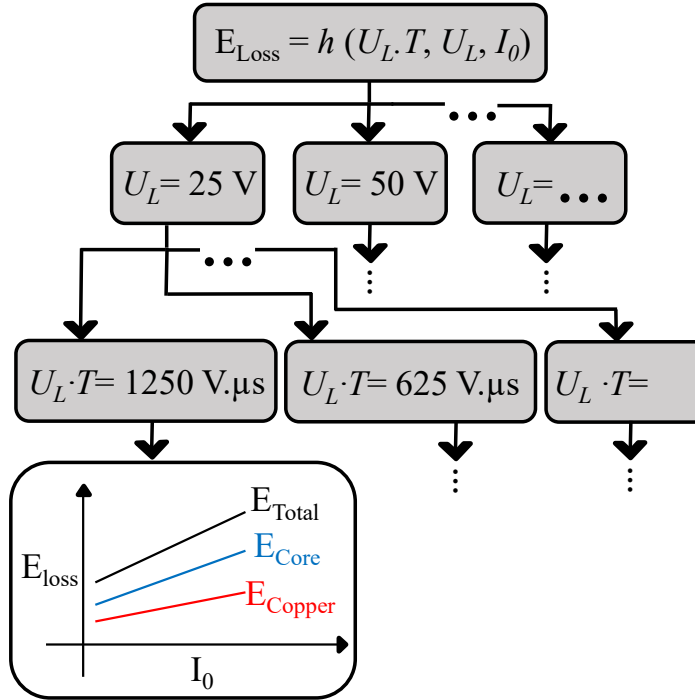
$$E_{core}(mJ) = h(U_L \cdot T, U_L, I_0)$$

- Copper loss

$$E_{copper}(mJ) = r(U_L \cdot T, U_L, I_0)$$

- Total loss

$$E_{total}(mJ) = s(U_L \cdot T, U_L, I_0)$$



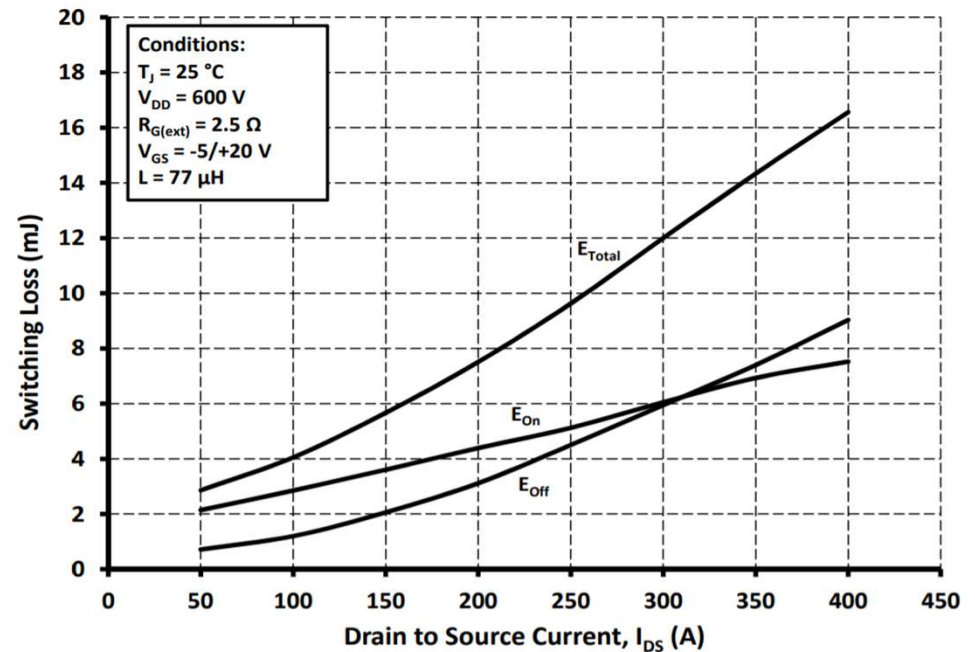
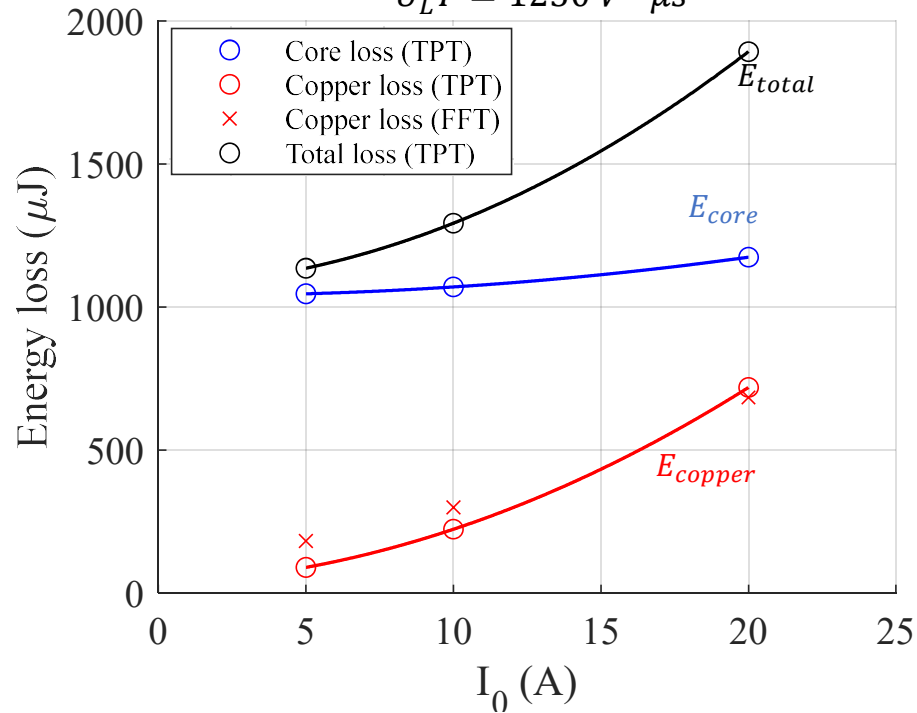
# Triple Pulse Test for Component-based Datasheet

- Copper loss verified against measured ac resistance + FFT results

$$P_w = R_{wdc}I_{dc}^2 + \sum_{n=1}^{\infty} R_{wacn}I_n^2$$

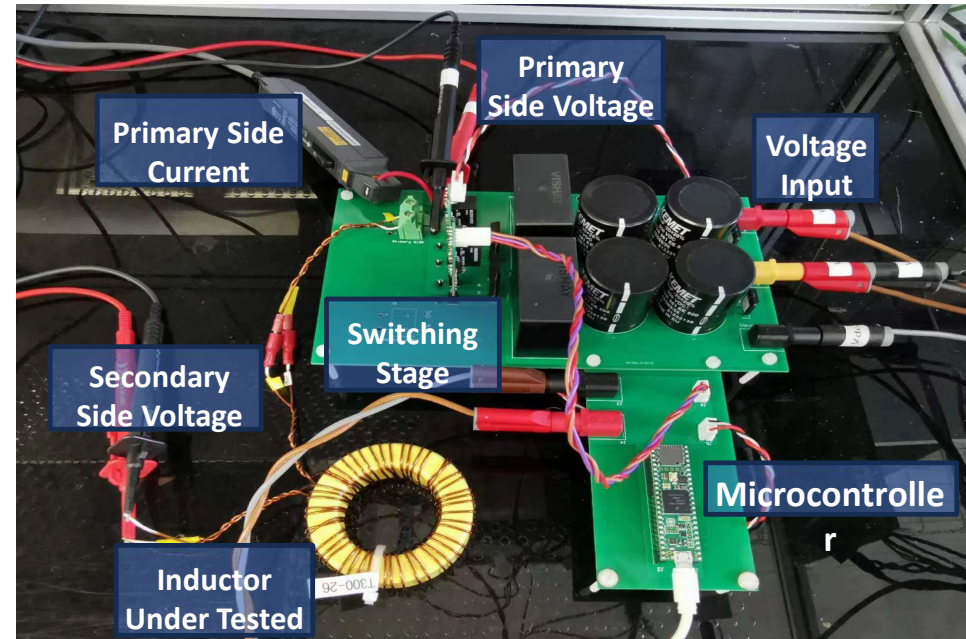
$$U_L = 25 \text{ V}$$

$$U_L T = 1250 \text{ V} \cdot \mu\text{s}$$

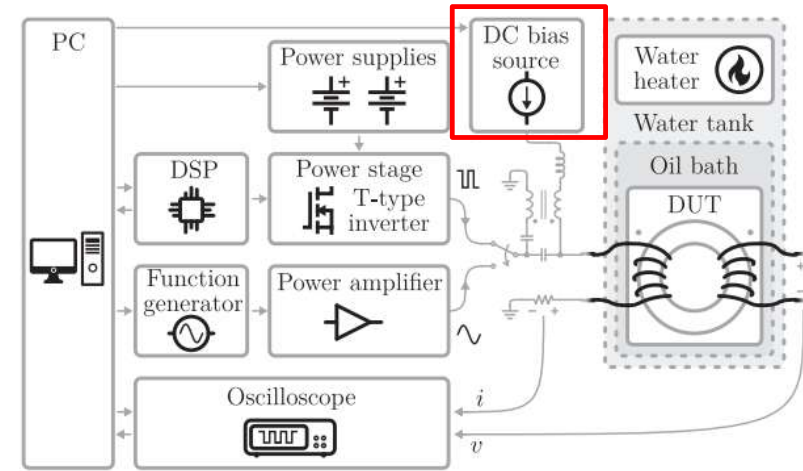


# Automated Triple Pulse Testbed (ATPT) 1.0

- Hardware-in-the-Loop
  - Automated testing procedure with safeguards
  - Self-correction mechanism
  - Approximate 6-8s per testing point
- Large-Signal
  - $\pm 400\text{V}$  60A power rating (Current version)
  - Power rating is independent from the power supply
  - Achieve dc-bias without additional power supply
  - Lower cost

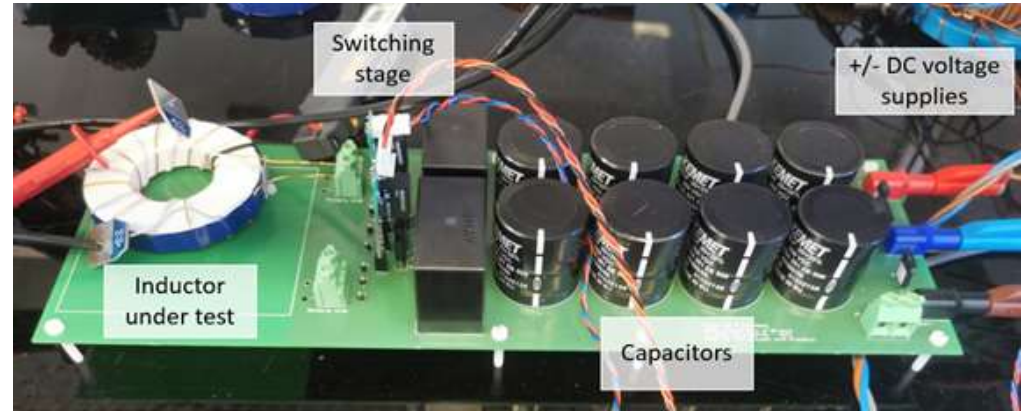
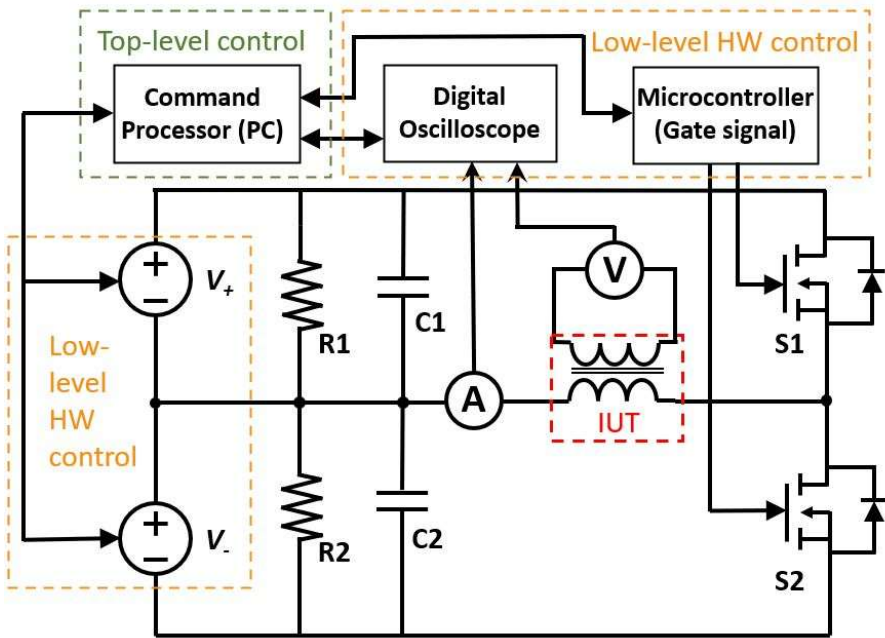


# Source of DC-bias in existing alternatives



- Large size and complicated set-up.
- Cost ineffective
- Power amplifier or external power supply is needed when measuring dc-bias operating points

# Circuit Schematic & Layout

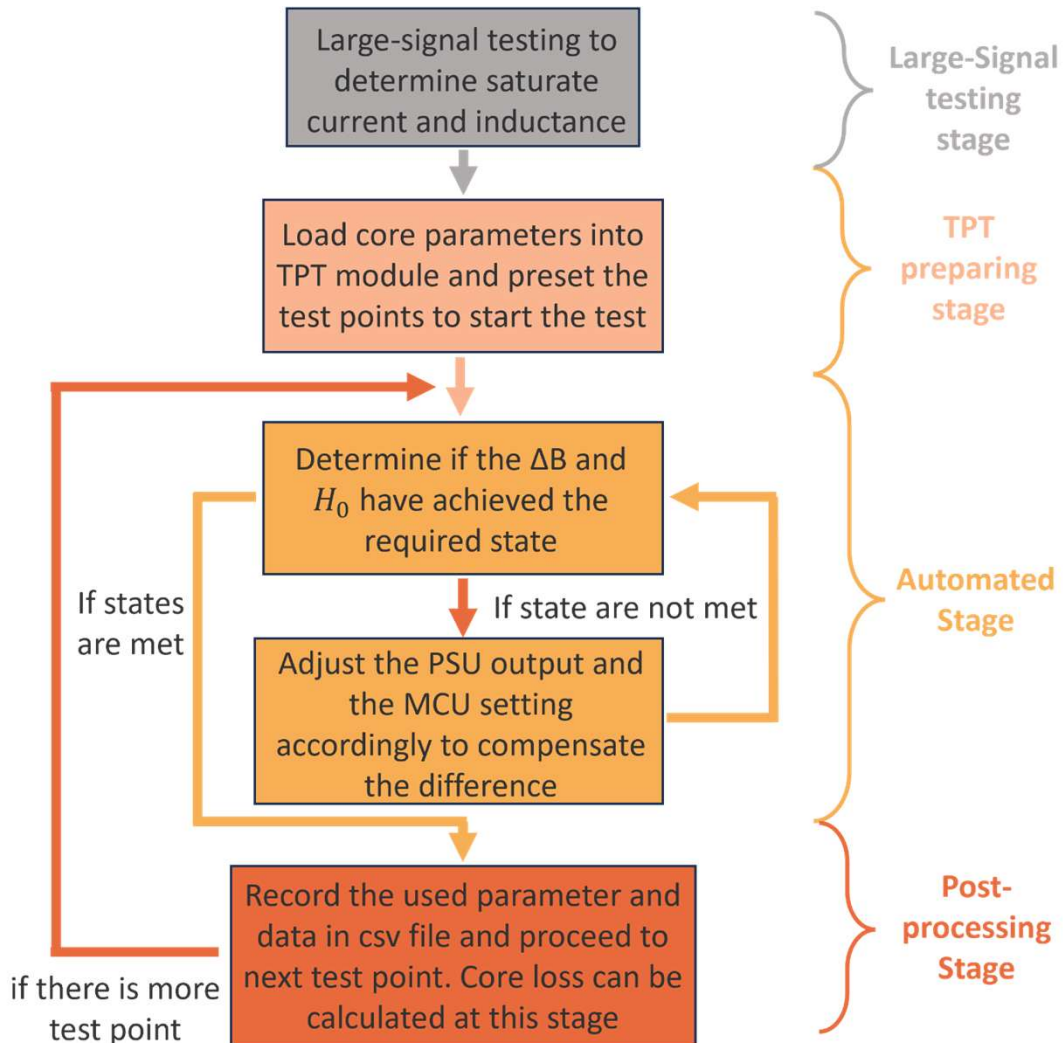


- PC distribute the command to all devices and receive data and responses from them
- Two-winding inductor is used
  - $V$  is measured from the second winding
  - $I$  is measured from the primary winding

- $\pm 400V$  60A power rating
- Frequency range from 3kHz to 300kHz
- The reservoir bank is 500uF which can survive an 80A rising current



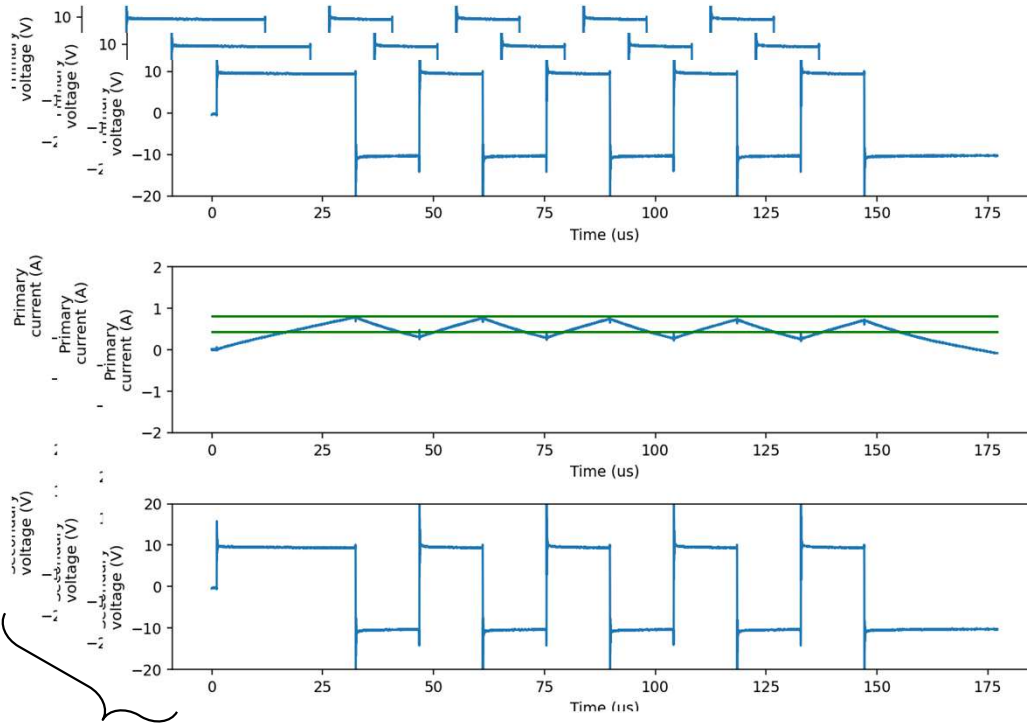
# HIL Software Architecture



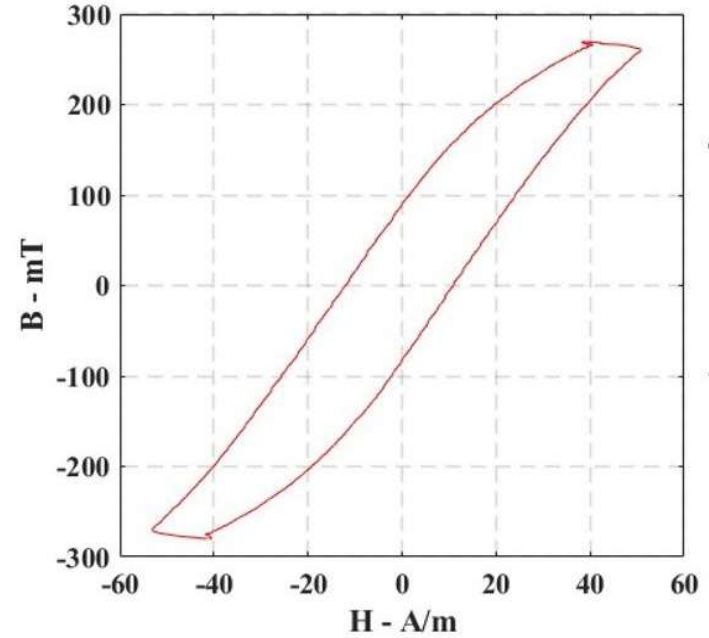
- Stage 1: The inductor under test (IOT) is characterised.
- Stage 2: Load the parameters and operating conditions.
- Stage 3: The ATPT will run the first test point.
- Stage 4: The programme will determine if all the conditions met their required state based on the acquired V-I waveform.
- Stage 5: Two power supply outputs and the microcontroller setting will be adjusted according to the difference in the response
- Stage 6: Repeat Stages 4 & 5 if states aren't met, record the desired data if all conditions are met.



# ATPT example results



N sets of datapoints with different operating conditions



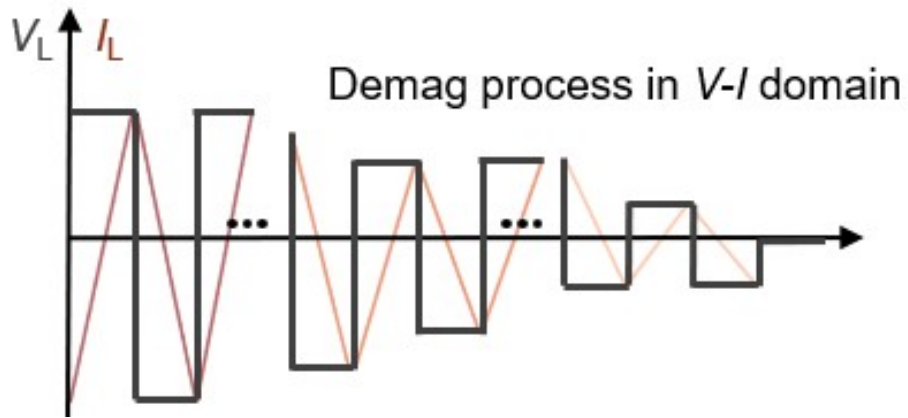
Each data point will cost the ATPT approximately **6-8 seconds** to finish the testing.



# Large-signal considerations

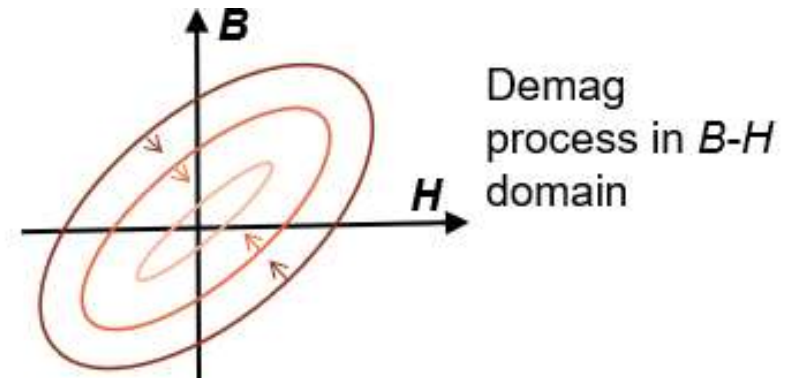
- Saturation & inductance

- Large-signal testing will risk saturate the inductor under test
- Saturating current limitation can be acquired by ATPT along with the inductance and safeguarded



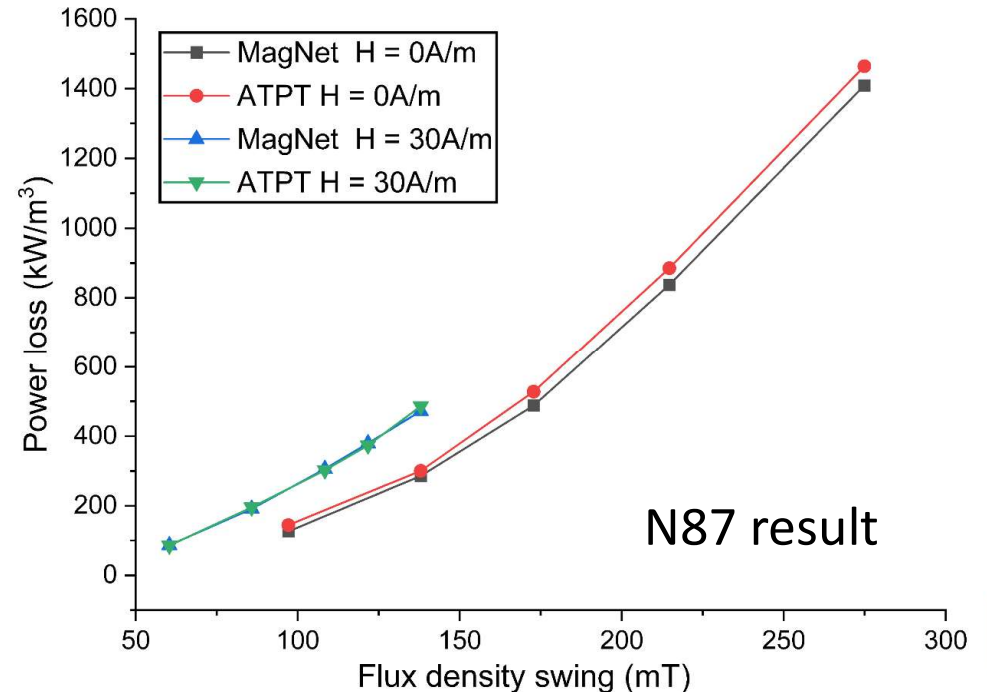
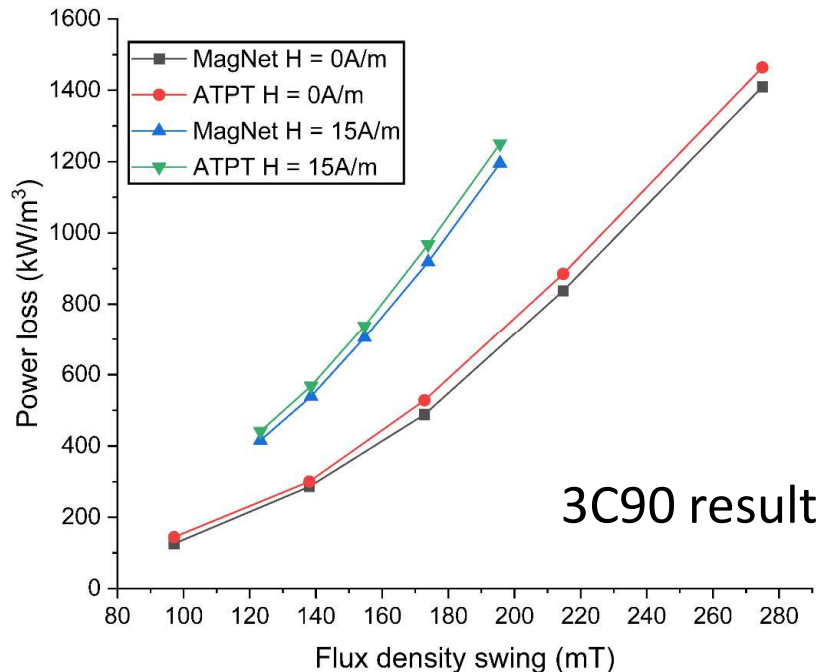
- Demagnetization

- Component under routine test may result having residual magnetism
- ATPT Demag process will eliminate this effect using gradually decreasing square waveform



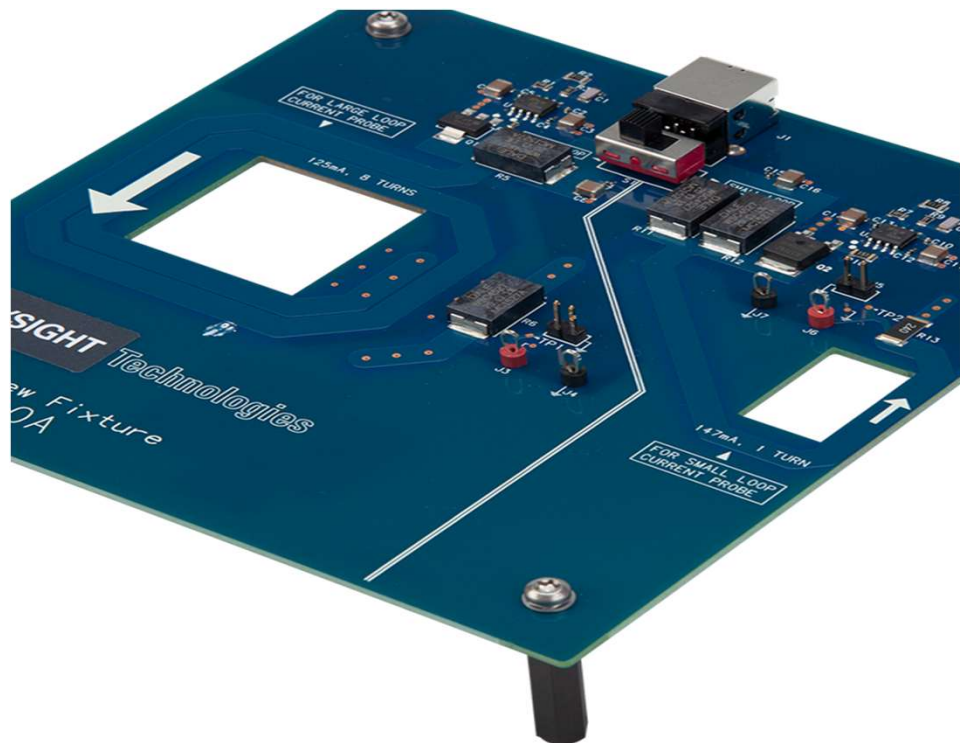
# Result Validation

- MagNet core loss database is used to verify the accuracy of the ATPT.
- A maximum of 4% error rate between ATPT and MagNet.
  - Batch-to-batch difference of cores
  - Difference in winding method; testing circuit; temperature

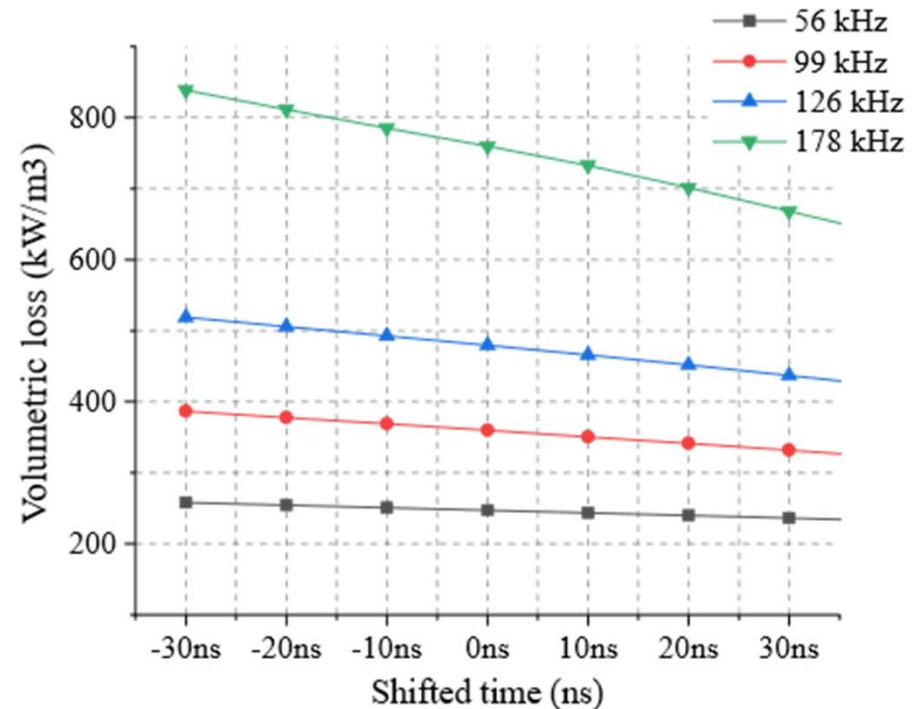


# Phase Skew Correction

- Hardware Calibration Tool
- Keysight U1880A

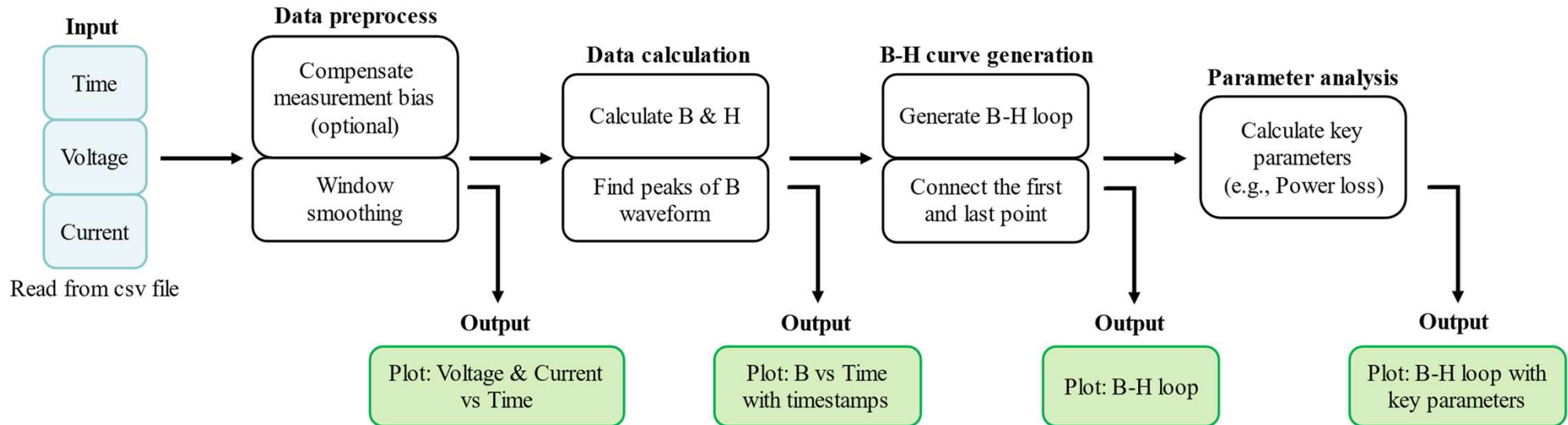
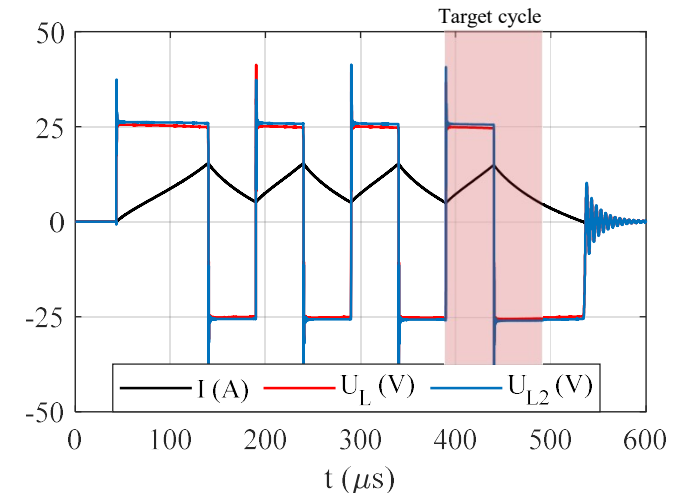


- Skew (ns) against Core Loss Measured - **Linear** relationship



# Data Post-processing

- Challenge – discontinuous waveform



# Conclusion

- Triple Pulse Test (TPT) is proposed for measuring core loss in floating dynamic BH loops from rectangular excitation voltages
  - Discontinuous procedure -> minimize testing efforts and setup requirements
  - Half bridge testing circuit -> compensate asymmetric voltage drops on power devices
  - Practical efforts to achieve closed BH loops
- TPT is analogous to the well-known Double Pulse Test (DPT) for power devices
- TPT is extended to include the copper loss for **component-based** testing concept
- An Automated Triple Pulse Testbed (ATPT) is demonstrated as an open-source, low-cost but large-signal testing tool



# THANK YOU

Questions?

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# References

- [1] T. Shimizu and S. Iyasu, “A practical iron loss calculation for AC filter inductors used in PWM inverters,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2600–2609, 2009.
- [2] J. Wang, K. J. Dagan, X. Yuan, W. Wang, and P. H. Mellor, “A practical approach for core loss estimation of a high-current gapped inductor in PWM converters with a user-friendly loss map,” *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5697–5710, Jun. 2019.
- [3] N. F. Oswald, “Towards an Improved Trade- Off Between Switching Losses and Radiated EMI Generation In Hard-Switched Power Converters,” PhD Thesis, University of Bristol, 2013.
- [4] C. R. Sullivan and J. H. Harris, “Testing core loss for rectangular waveforms,” 2010. [Online]. Available: <http://www.pσμα.com/coreloss/pilot.pdf>.
- [5] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, “Core losses under the DC bias condition based on steinmetz parameters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 953–963, 2012.

