High-Density Low-Profile Capacitors towards 3D Heterogeneous Integration

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About the Speaker

Associate Professor, FIU (in BME and ECE Departments)

Expertise in packaging and integration, power and RF components, wireless biosensors

340 publications, which include 8 patents.

More than 25 best-paper awards.

Co-advised ~40 MS and PhD students

Former Chair of Nanopackaging Technical Committee, Former EPS Representative of IEEE Nanotechnology Council, IEEE Distinguished Lecturer in Nanotechnology for 2020-2021, Associate Editor for IEEE Nanotechnology Magazine and Transactions of Components, Packaging and Manufacturing Technologies (T-CPMT).

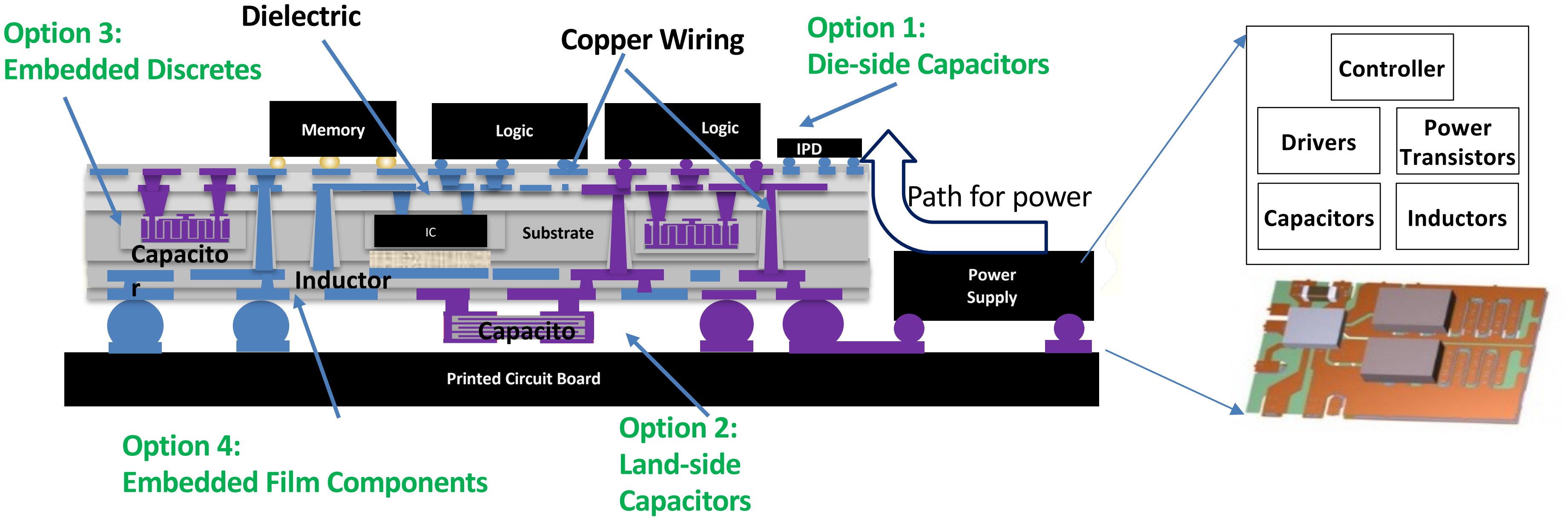
PhD from Rutgers University in 1999 in Ceramic Engineering, ME from the Indian Institute of Science, Bangalore and BS from the Indian Institute of Technology, Kanpur (1993)

Outline

1. System topologies, package integration architectures:
   - 1A)Power delivery for computing
   - 1B)Intermediate voltage WBG Power modules
   - 1C)High-voltage Power modules in electric vehicles

- Capacitor technologies in various WBG applications:
  - Capacitors in 1-3 V, 10-100 MHz Computing applications
  - Capacitors for 12-48 V WBG power modules:
  - Capacitors for 400V-1500V Power modules:

1A) Traditional Power Delivery for Computing



Option 3:
Embedded Discretes

Option 1:
Die-side Capacitors

Option 4:
Embedded Film Components

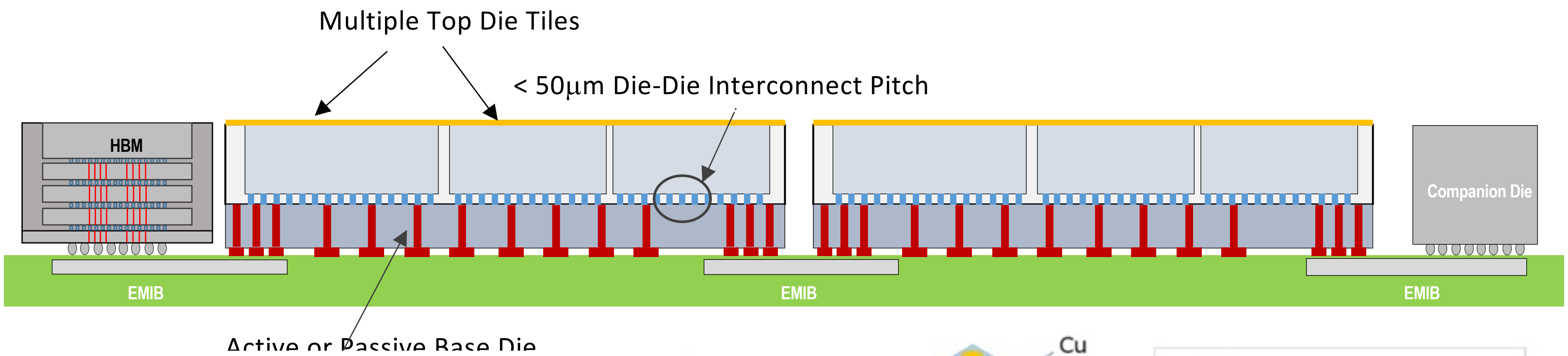
Option 2:
Land-side
Capacitors

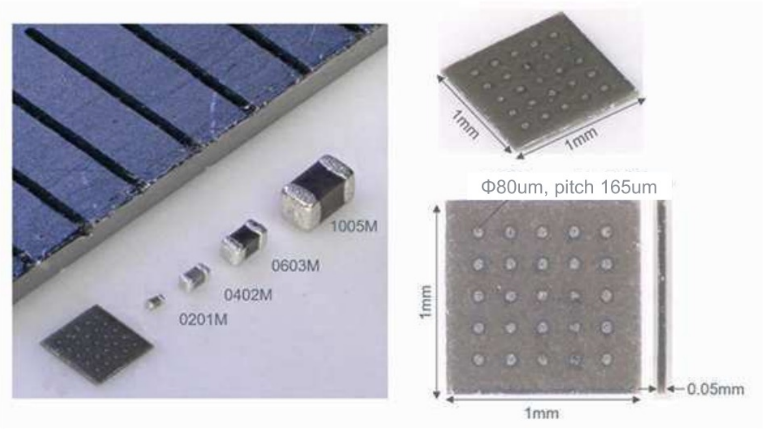
PCB: voltage step-down: *For systems with >3-5V system bus*

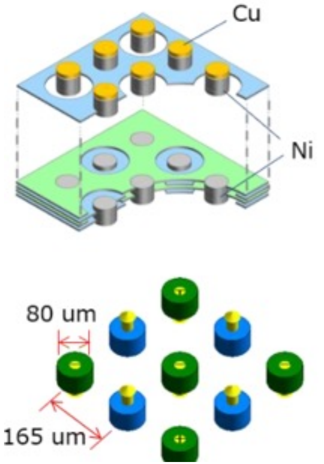
SiP: IVRs: *Significantly improve performance-per-watt,* Bypass majority of PDN, Fine-grain power management

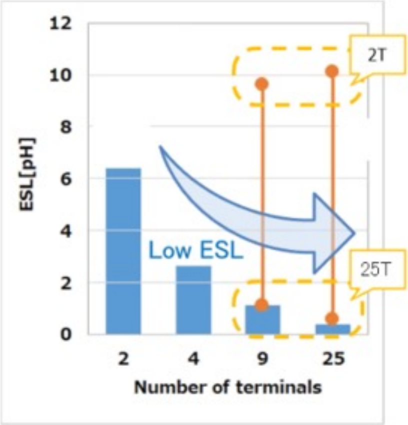
Load die: LDOs: *Optionally provides additional voltage regulation*

1A) Capacitors in Computing









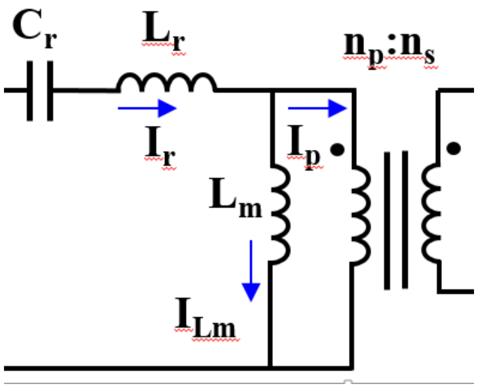
Trench capacitors are key to lowering the loop inductance and produce best electrical performance

Source: Ravi Mahajan, Intel and ASME Fellow

Source: Shinsuke Abe, Murata

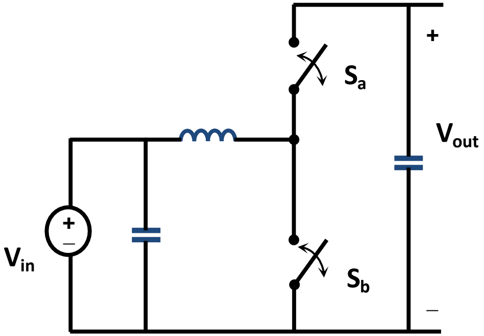
1B) Trend to Capacitor-Centric Power Conversion

Transformer-based



- Low storage density magnetics
- Large and bulky components
- Limited integration opportunities
- EMI issues

Switch tank capacitor



- High energy density capacitors
- Major opportunities to further enhance densities
- Simpler wafer and package integration
- No EMI issues

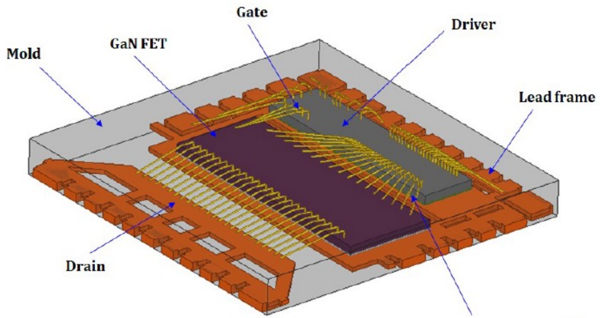
Multilevel switch-tank capacitors:

Divide the voltage into series modules

Resonant converters:

LC resonance – the impedance is high, current is very low: so, you switch at that point (ZCS)

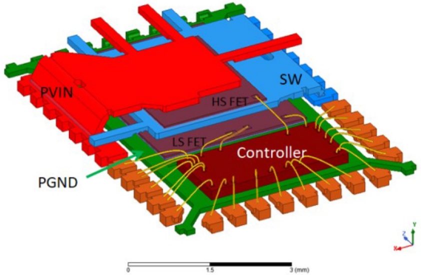
1B)Discrete WBG Power Modules with Integrated Passives



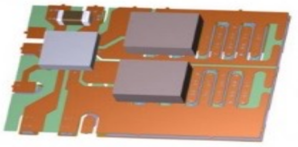
Why:

- Miniaturize footprint and thickness
- Eliminate Bill-of-Material burden for the customer
- Reduce parasitic inductances from 10s of nH to sub-5 nH
- Reduce thermal resistance (>30 C/W to 10-20 C/W to <1 C/W)
- Integrated other functions:
  - Gate driver isolation, sensors, EMI isolation

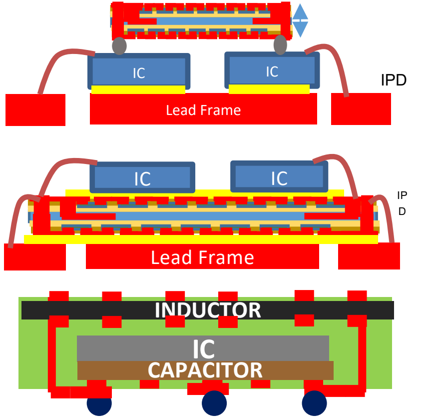
Texas Instruments,
Rajen Murugan et al.,



As topologies migrate from switching regulator to resonant/hybrid with multilevel and multiphase conversion: more passives are needed



Texas Instruments,
Mishra et al.,

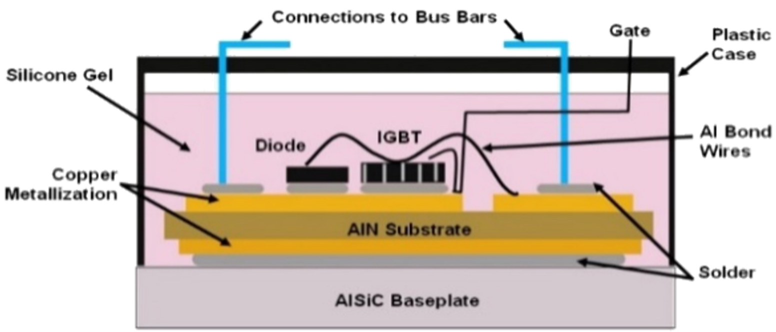


Power modules with passive-active integration

What causes delays:

- Need system co-design for thermal, mechanical, electromagnetic and material considerations
- Supply-chain and manufacturing readiness
- Market pull

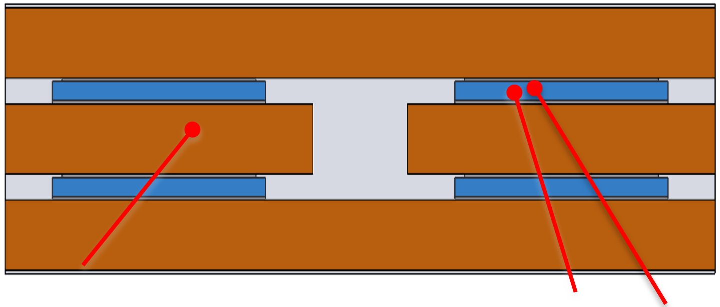
1C) 3D Power Packaging with Capacitor Integration



- Large electrical inductance and high thermal resistance
- Reliability challenges with nanocopper and nanosilver
- Thick packages

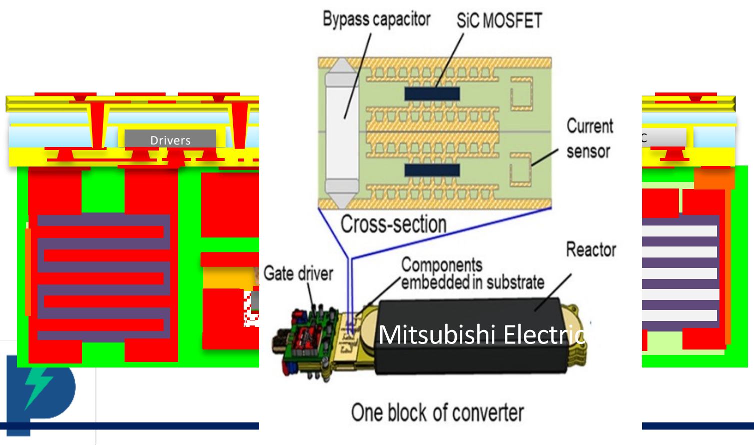
Leadframe Fan-Out Packaging

- **No reliability challenges with nanocopper**
- **(Bonding layers are in compression)**
- **Thin packages**
- **Lower electrical inductance and thermal resistance**



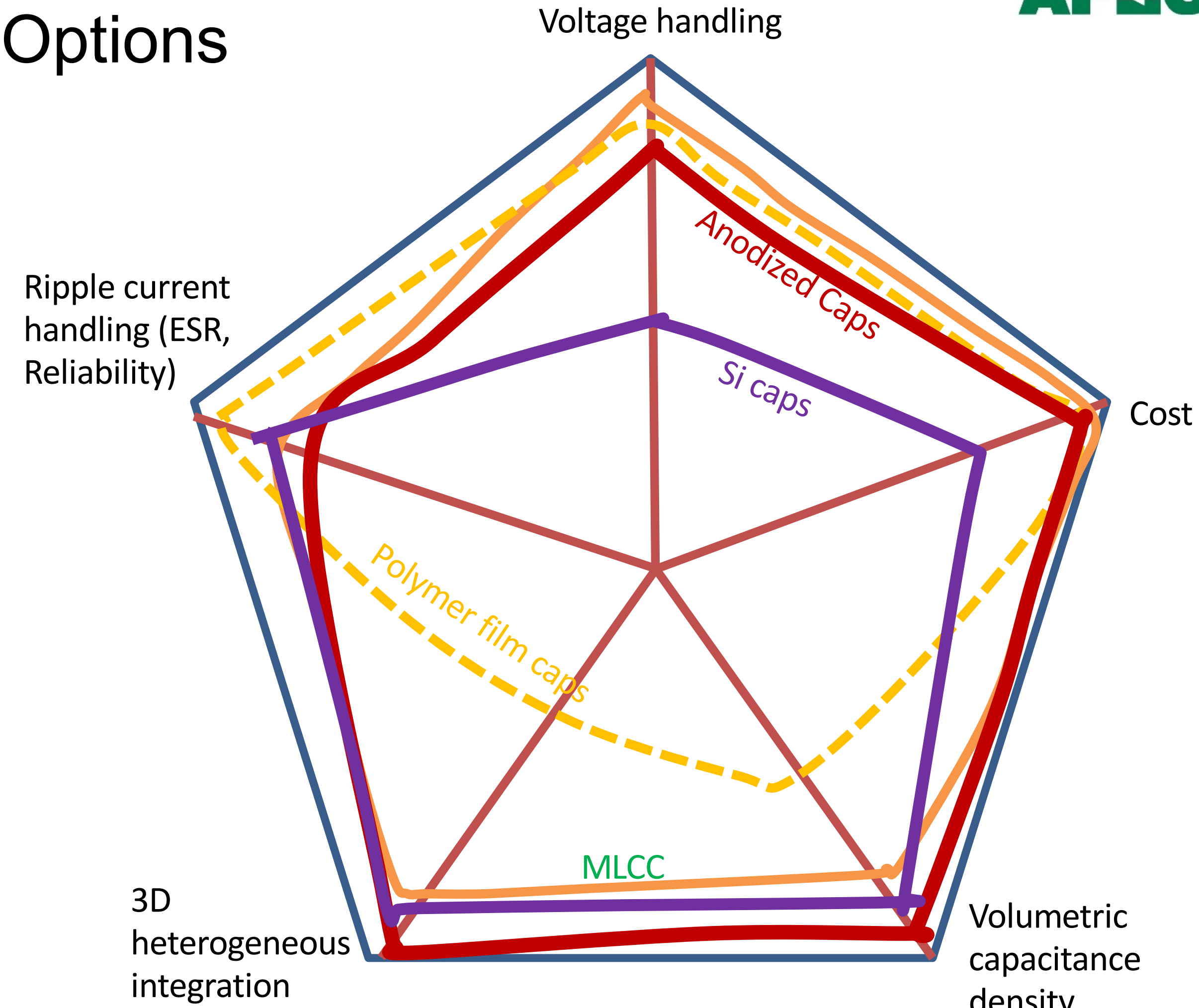
Heat generation 100 W

Heat transfer coefficient 10,000~50,000 W/m^{2}K



2. Key Capacitor Options

- MLCC
- Si trench
- Solid electrolytic caps
- Polymer film capacitors

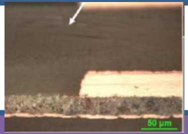


2A) Embedded Capacitors Evolution for Computing

2000 2008 2016 2020 2025

Board or package embedding; I/O decoupling; 100 MHz

Embedded polymer laminate and dielectrics



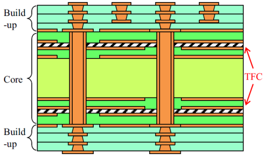
0.1 nF/mm^2
Polymer laminate dielectrics

0.5 nF/mm^2
Polymer film dielectrics

1 nF/mm^2

Embedded ceramic film

2-3 nF/mm^2
Thin oxides



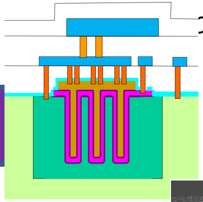
20-30 nF/mm^2
BaTiO3 film

30-50 nF/mm2 enabled by new multicomponent oxides

Package embedding;
Core and I/O decoupling; 100-500 MHz

Wafer-integrated capacitors

Silicon capacitors Deep trench
0.08 µF/mm^2 0.25 µF/mm^2 0.5 µF/mm^2



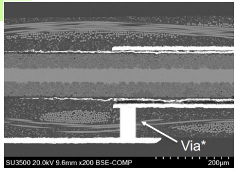
Ultra-high surface area silicon
1-2 µF/mm^2

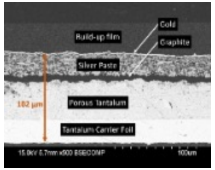
Multilayered dielectrics on deep trench

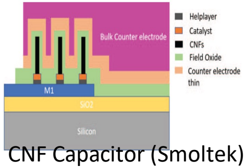
Adv. Nanotech.
>3 µF/mm^2

IVR; Embedded PoL 1-20 MHz

Embedded capacitors Panel





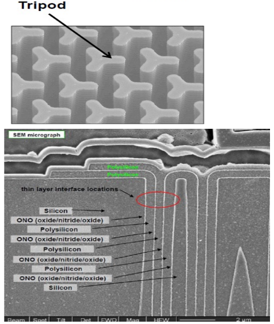


CNF Capacitor (Smoltek)

2A) Deep Trench Land-Side Inserted Si Capacitors

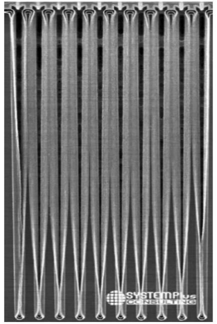
Land-side on-Si capacitors for integrated fan-out packaging

High-density Silicon Trench

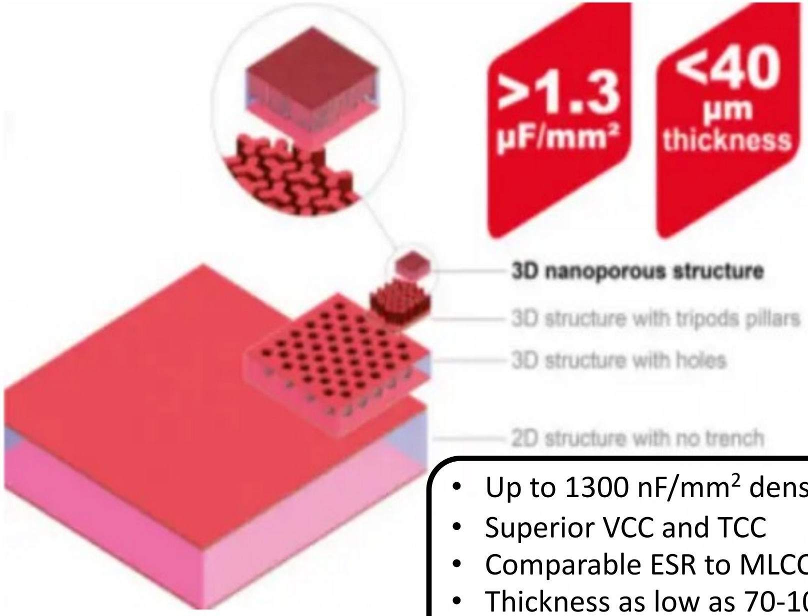


MIMIM silicon trench capacitor with Tripod structure and ONO dielectric [3]

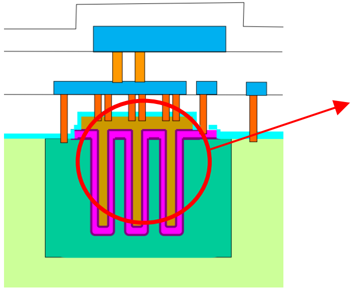
Deep Trench Capacitors



High-aspect ratio deep trench capacitors in silicon [4]



- Up to 1300 nF/mm^2 density
- Superior VCC and TCC
- Comparable ESR to MLCCs
- Thickness as low as 70-100 µm



- Cost of process
- Density still limited without high-k materials

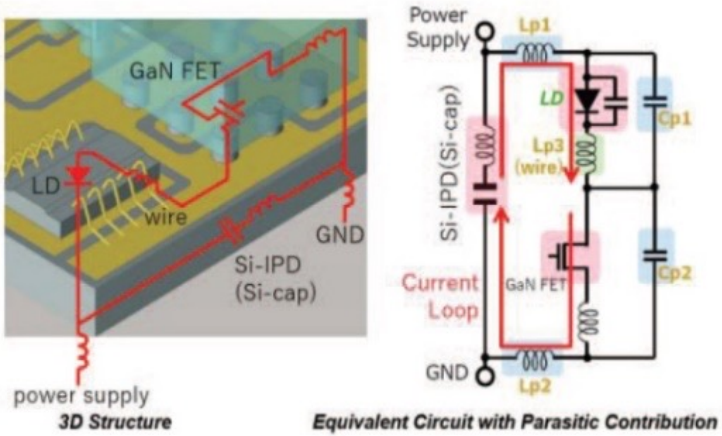
Deep trench capacitor structure

Density, nF/mm2	Breakdown Voltage, V	TDDB, V	Max Voltage rating, V
180	16.1	7.0	4.5
250	14.3	6.8	4.2
500	6.5	4.5	3.2
600-700	4.0	3.8	2.5-1.2

Source: Shinsuke Abe, Murata

2A)Trench Capacitors in WBG Modules

- Performance stability at high temperature (up to 105 °C).
- Scalability to high voltage with high stability (>100 V).
- Low self-inductance (<10 pH).
- Compliant with the automotive quality standard (AECQ100).
- Flexible design and placement to minimize the loop inductance:
    - (100 pH for the whole circuit).

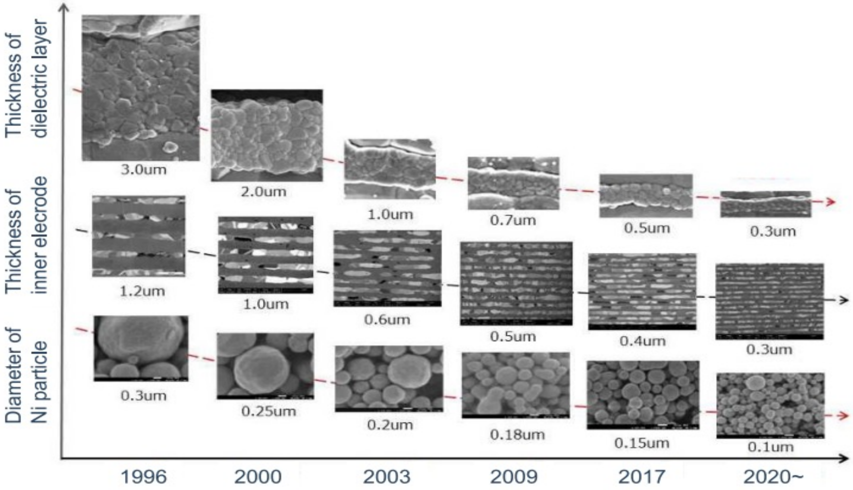


3D Structure

Equivalent Circuit with Parasitic Contribution

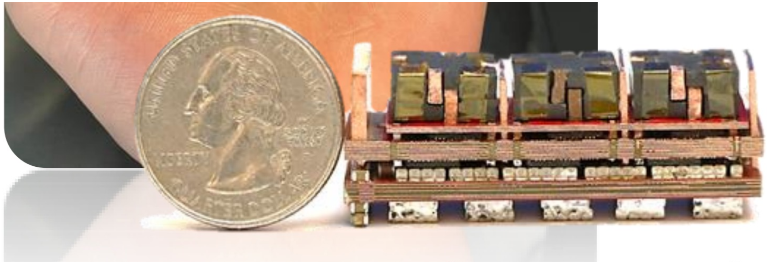
Modules on silicon capacitor substrates
Murata’s LIDAR modules

2B)MLCCs in WBG Power Modules



- 10 nF/mm^2 per layer per micron;
- 1 μF/mm^2 for 100 microns
- 5-10 milliohms x microfarad

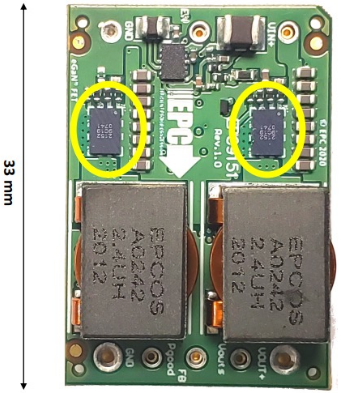
- 2 μF/mm2 (1-3 V) for 225 microns:
- 0.44 (4-5 V) – 1 (1-3 V) μF/mm^2 for 110 microns:
- 0.2 (4-5 V) μF/mm^2 for 50 microns



780 A, 1 V, 1 A/mm^2, 1,000 W/in^3

Chen, Princeton Univ

300 W
96% Efficiency
Bidirectional 48-12 V



Setup	Setup 1	Setup 2
		
PWM Frequency	20 kHz	100 kHz
Dead time	500 ns	21 ns
Input Caps	2 x 330 μF electrolytic	2 x 22 μF ceramic X7R
Input inductor	1 x 2.7 μH	None

Lidow, EPC

2B) Challenges in Capacitors for WBG Modules

- MLCCs:
  - 2 μF/mm^2 for 100 mm thickness for 1-3V
  - Qualified for 85-105 C;
    - Reliability concerns for higher temperatures;

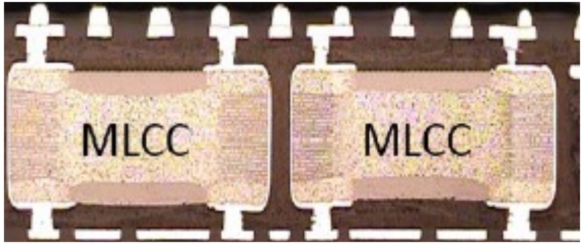
Capacitor inside the package:

- Thermal stresses can cause failures in the MLCC
  - Delamination within the capacitor, or cracking in the ceramic component have been observed during long-term temperature, humidity and bias testing.
  - Double-side cooling to lower the junction temperature

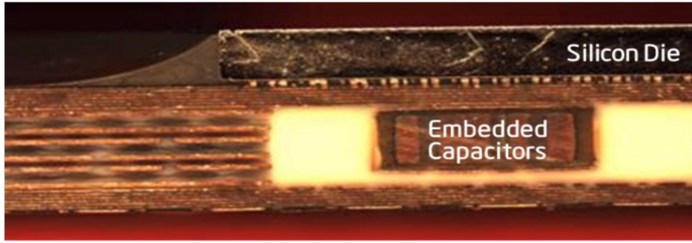
- Mechanical stresses;
  - Such failures are predominant in larger-size, lidded-packages that contain an array of capacitors on the top side of the package substrate

Electrolytic capacitors

- Current-handling :



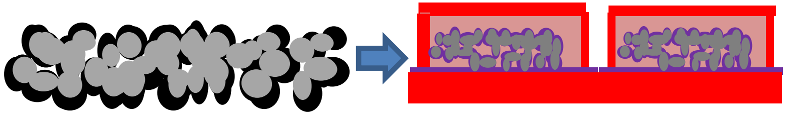
(Source: Unimicron)



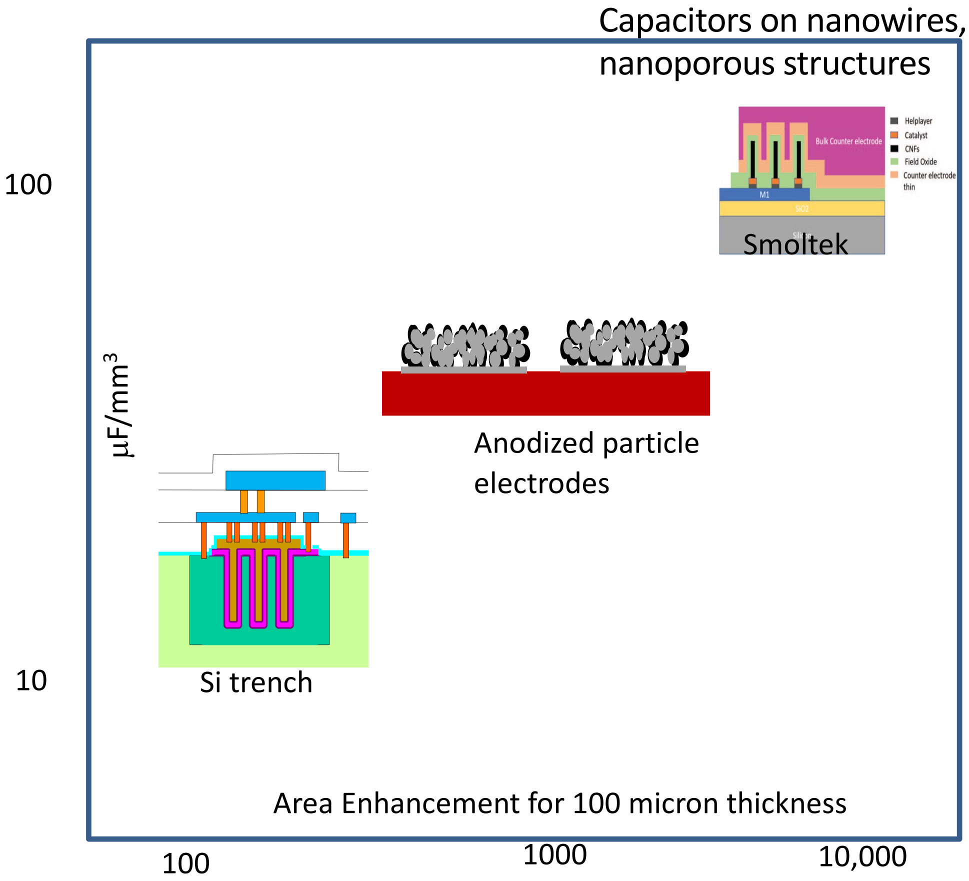
(Min et al., Intel, ECTC 2013)

2B)High Surface Area Capacitors:

Sintered Ta Particulate Electrodes



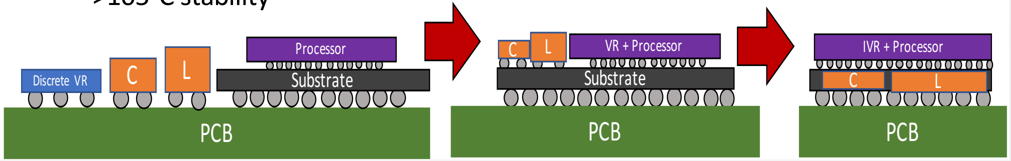
- Higher volumetric densities
- Thinner profiles
- Multi-terminal arrays – eliminate pick-and-place and keep-out zones
- 3D package compatible
- Integrated with copper



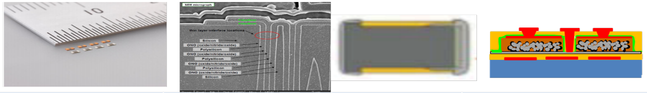
2B) High-Density Anodized Film Capacitors

Objectives

- Ultra-high density capacitors:
  - >1 µF/mm^2 at 1 MHz,3-48 V, & 50 mΩ ESR
  - 1 nA/µF leakage current
  - Simpler processing on wafer or package
  - 100 µm thickness
  - >105°C stability

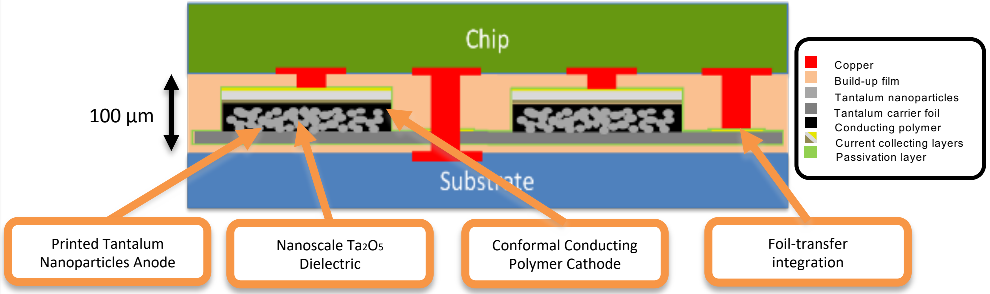


Prior Art



	MLCC	Trench Caps	Ta Chip	Emerging Need
Volumetric Density	20 µF/mm^3	1 µF/mm^3	~10 µF/mm^3	50-100 µF/mm^3
Thickness	100 µm	100 µm	600 µm	50-100 µm
Freq. Stability	10-100 MHz	>1-10 MHz	0.2 -1 MHz	>10 MHz
ESR	~10 mΩ	50 mΩ x µF	>100 mΩ x µF	~50 mΩ x µF
% ΔC/V	-13 % to -70% (1 to 4 V)	~ 0 %	~ 0 %	~ 0 %
Max. Temp	85° C	150° C	125° C	>125° C
	PICK AND PLACE			FILM EMBEDDING WAFER OR PANEL INTERCONNECTS

Unique Approach



Printed Tantalum Nanoparticles Anode

- High-surface area at ultra-thin form-factor
- Scalable to any design need

Nanoscale Ta$_2$O$_5$ Dielectric

- Paraelectric for DC bias and temperature stability
- Amorphous for low leakage current

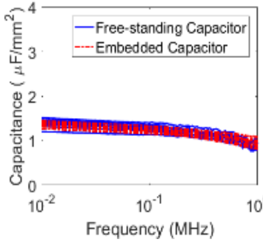
Conformal Conducting Polymer Cathode

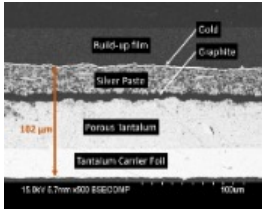
- Low-resistivity and thick coating for low ESR
- Self-healing for low leakage current

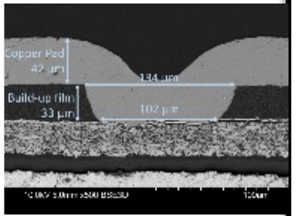
Foil-transfer integration

- Thin-film lamination
- Ultra-short copper interconnections for reduced impedance
- Low-cost, panel-scale, 3D approach

Major Accomplishments

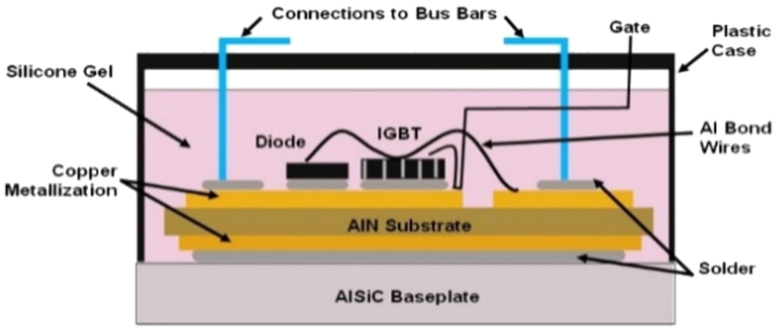






>1µ F/mm^2 up to 1 MHz at 5 V with low ESR, low leakage current, and 100 µm component thickness

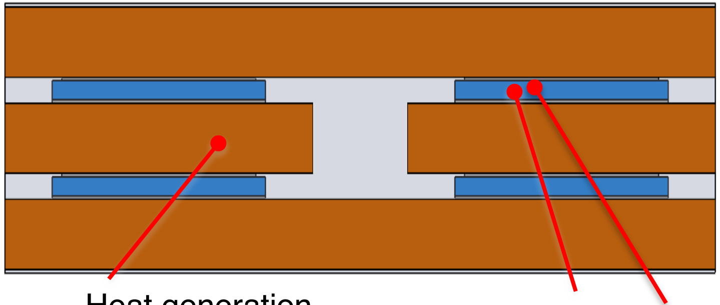
1C) 3D Power Packaging with Capacitor Integration



- Large electrical inductance and high thermal resistance
- Reliability challenges with nanocopper and nanosilver
- Thick packages

Leadframe Fan-Out Packaging

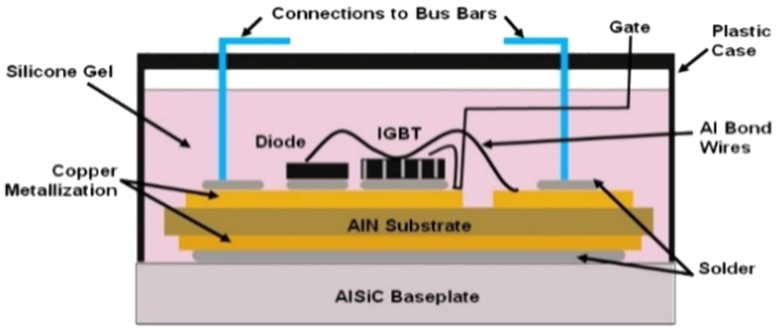
- **No reliability challenges with nanocopper**
- **(Bonding layers are in compression)**
- **Thin packages**
- **Lower electrical inductance and thermal resistance**



Heat generation
100 W

Heat transfer coefficient
10,000~50,000 W/m^{2}K

1C) 3D Power Packaging with Capacitor Integration



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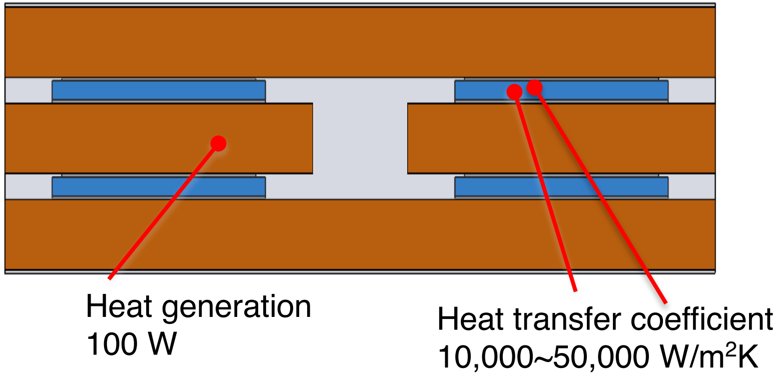
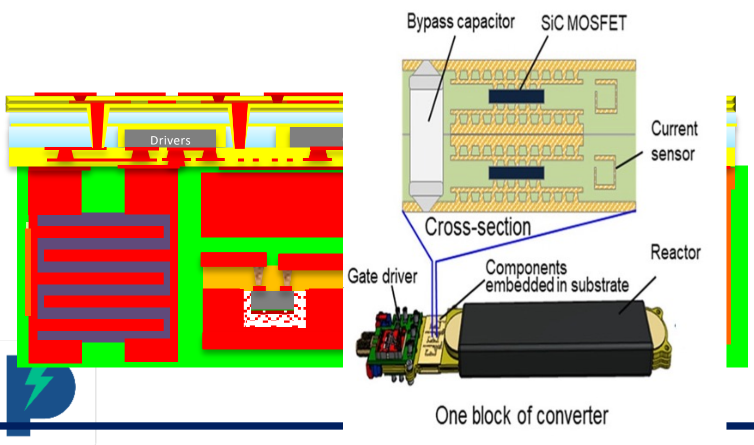
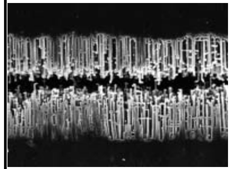
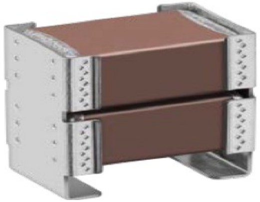




2C) High-Voltage Capacitors

	Polymer film caps 		Aluminum foil Caps 	Ceramic paraelectric (KEMET, $CaZrO_3$) 		TDK CeraLink® PLZT Ceramic 		High surface area electrodes and dielectrics
µF/cc	0.7	0.085	>6	1	0.6-0.012	5.5	5.5-2	10
V	400	600-2400	200-500	500	1000-3000	400	500-900	400
ESR mΩ x µF		60	100-228	<1	<1	10-12	10-12	5
Irms A/ µF	1	5.2	5-31	50		12	12.5	
Temp		125-150 C	105	125	125	150		105

Summary

- Emerging WBG-enabled power modules rely lot more on capacitors
- High volumetric density, power handling, ripple current-handling and 3D integration are the key metrics
- MLCCs tend to dominate most applications
- Trench capacitors will benefit from smaller footprint and easy heterogeneous integration
- Electrolytic capacitors offer higher volumetric density
- Nanoscale capacitors will dominate future systems if all the performance metrics need to be met