New failure mechanisms relevant for SiC power devices - background and how to tackle them

Peter Friedrichs, VP SiC

Infineon Technologies AG

Outline

- Introduction into SiC specific failure modes
- Procedures for the qualification of silicon power devices and their applicability to SiC
- Focus humidity testing
  - DC tests
  - AC tests
- Power cycling behavior of SiC
- Summary

Outline

- Introduction into SiC specific failure modes
- Procedures for the qualification silicon power devices and their applicability to SiC
- Focus humidity testing
  - DC tests
  - AC tests
- Power cycling behavior of SiC
- Summary

What are reasons for SiC specific failure modes

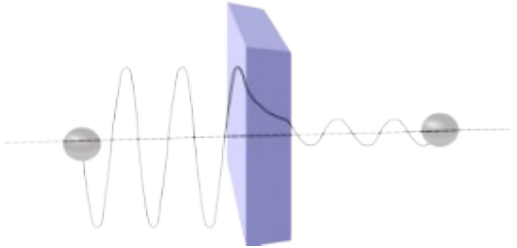
- Compared to silicon the electric fields in the chips and mainly at its periphery are substantially higher
- Mainly for gate oxides the larger bandgap, different tunneling barriers and carbon related oxidation products can influence reliability
- Certain material properties like material stiffness (E-modulus) influence the cycling stability of chips in its package
- New operating modes, e.g. very fast switching at high dv/dt rates and at high DC bus voltages might trigger new failure modes since those conditions are not possible with silicon

Dedicated quality assurance program needed to guarantee field stability

Example : Gate oxide (GOX) in SiC MOSFETs

SiC has a larger bandgap

(1.1 eV Si vs. 3.2 eV SiC)

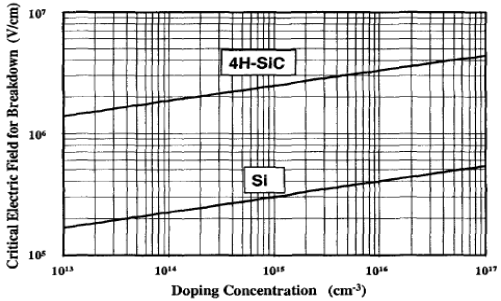


Enhanced tunneling

Less relevant for FIT rates under nominal operating conditions

SiC has higher blocking capability

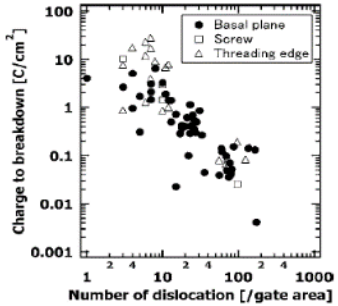
(0.3 MV/cm Si vs. 3.0 MV/cm SiC)



Higher fields in blocking state

GOX stress induced by V_{DS} in blocking mode as well

SiC has higher defect density in substrate and in GOX



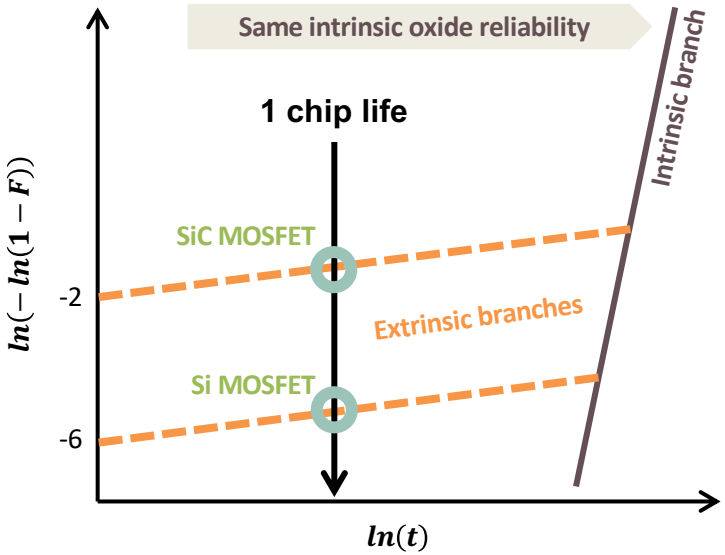
Higher risk of early GOX breakdown

Measures to sort out affected devices required to meet FIT rates

Effect of high gate oxide defect density on SiC MOSFETs' stability: Analyzing failure statistics

How does Weibull Plot look like for SiC and Si MOSFETs?

(same area and gate oxide thickness)



At the end of processing (EOP):

SiC MOSFETs → much larger extrinsic defect density

Failure probability: up to 4 orders of magnitude higher

Many decades of development away to **drop extrinsic GOX defect density below 1% at EOP** in modern SiC MOSFETs

< 0.001% (10 ppm) or < 0.0001% (1 ppm) is needed!

How can we get rid of devices with critical extrinsics?

Devices are “aged” by an electric screen pattern at the gate

Devices with **critical extrinsics fail/degrade**

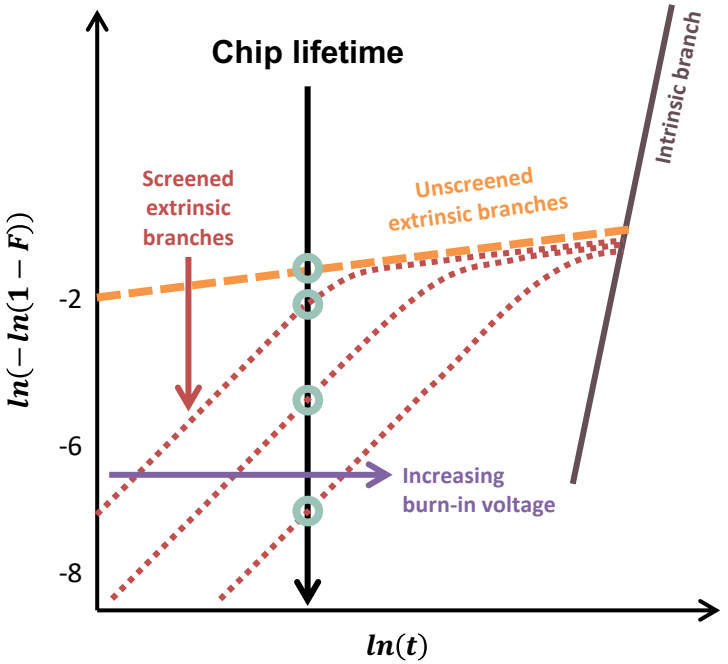
Devices **without critical extrinsics pass**
(small amount of lifetime taken)

Screening more efficient
→ **if ratio between screen bias* and use bias** is high**

Screen bias level
must not degrade device performance

Conclusion : Thicker oxides enable lower FIT rates:
1 FIT = 1 Failure In Time = $\frac{1\ fail}{10^9 hours}$

* Screen bias: bias for the test
** Use bias: recommended value for the gate bias based on datasheet



How can we get rid of devices with critical extrinsics?

Devices are "aged" by an electric screen pattern at the gate

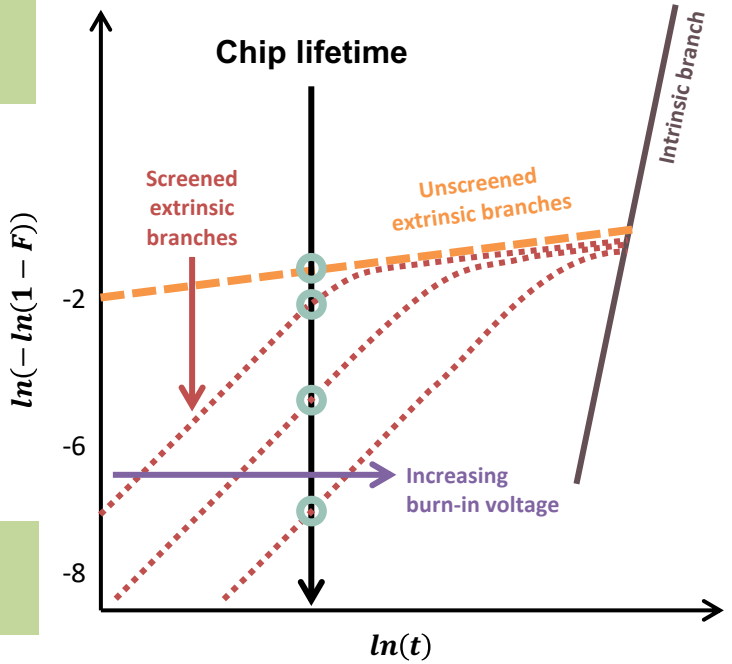
Challenge : Thicker gate oxides increase the R_{on}

Reliability increases **exponentially** with GOX thickness

and

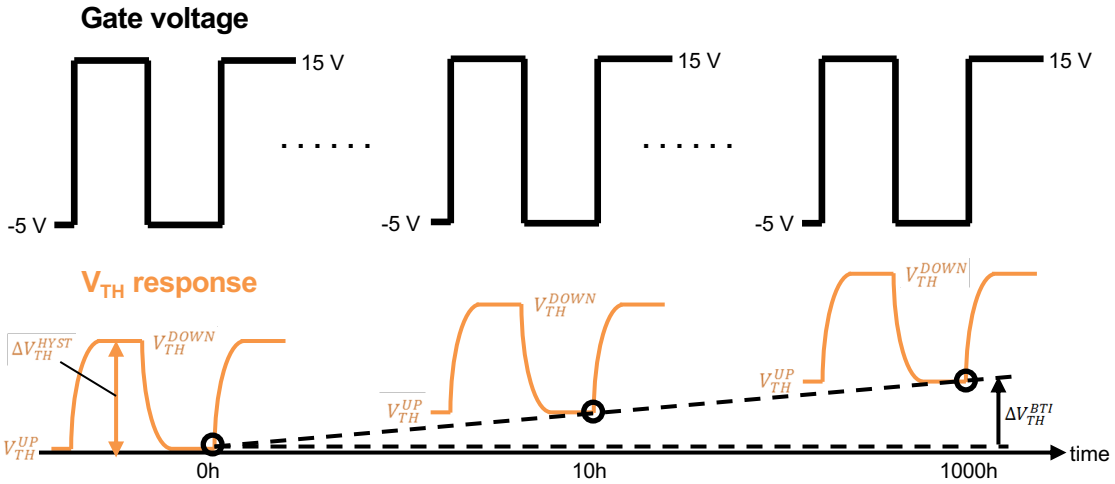
R_{ON} increases only **linearly** with GOX thickness

Over-proportional benefit for reliability



Example : Drift of the threshold voltage in SiC MOSFETs: Static contribution

2 quasi-static Bias Temperature Instability (BTI) components exist



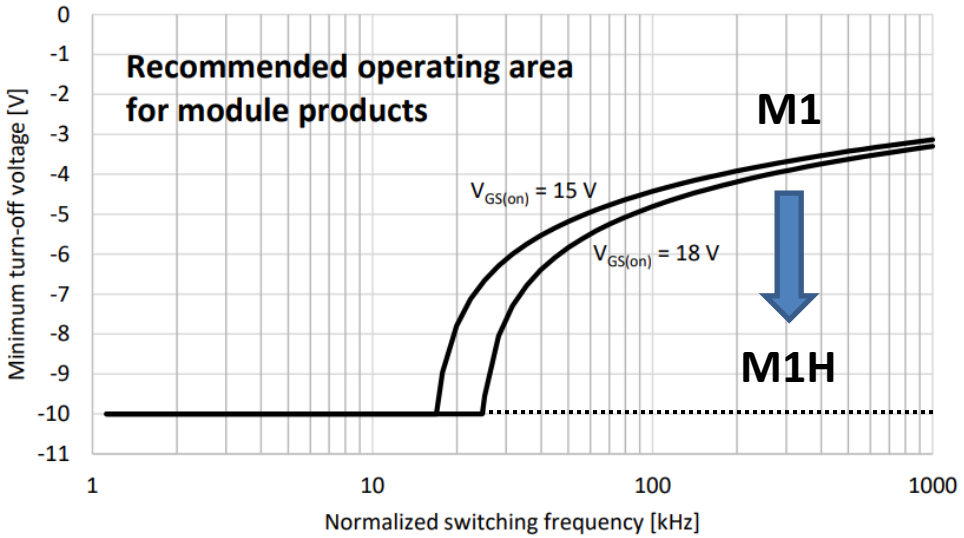
Fully reversible threshold voltage hysteresis $(\Delta V_{TH}{}^{HYST})$

More permanent threshold drift $(\Delta V_{TH}{}^{BTI})$

Special pre-conditioning sequence proposed e.g. in JEDEC JEP 183

Example : Drift of the threshold voltage in SiC MOSFETs: Dynamic contribution*

By switching triggered, a 3rd Bias Temperature Instability (BTI) components exist



*H. Jiang, X. Zhong, G. Qiu, L. Tang, X. Qi and L. Ran, "Dynamic Gate Stress Induced Threshold Voltage Drift of Silicon Carbide MOSFET" IEEE Electron Device Letters, vol. 41, no. 9, pp. 1284-1287, Sept. 2020

Triggered by switching device, a **third effect needs to be taken into account** when V_{TH} effects are quantified

Amount of V_{TH} drift mostly **influenced by switching frequency** and **chosen bias for turning off the MOSFET**, partially also by turn-on bias at the gate

Infineon provides an Application Note (AN2018-19) that describes how to make sure to **stay within the safe operating area.**

Magnitude of the effect needs to assessed for a certain technology and is in the focus of optimization targets ➔ in M1H version strongly suppressed

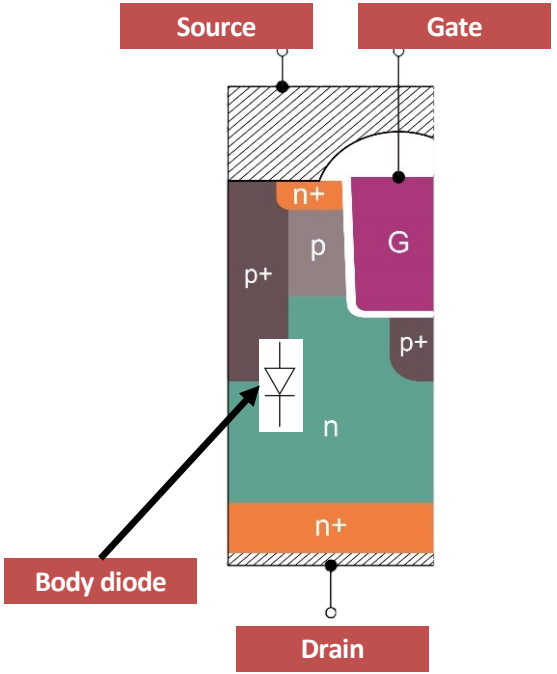
MOSFET body diodes: Structure and requirements

Vertical power MOSFETs (planar and trench types)

These contain a diode that allows conduction in the 3rd quadrant and can be used as freewheeling diode – **body diode**

Since V_F of pn-based diodes in SiC is high
→ **It is recommended to use synchronous rectification**

Turn on the channel after a short dead time
In this mode, channel carries most of the current and low losses (comparable to the 1st quadrant) are secured



The potential degradation in bipolar elements in SiC components: Recombination induced increase of $R_{DS(on)}$ and V_{SD}

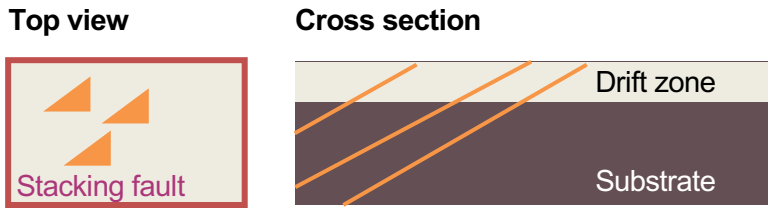
Bipolar degradation might **affect all SiC MOSFET** technologies

Effect is defect-driven and related to defects of **substrate material**

Statistical effect: **devices without these defects will not have bipolar degradation effect**

Effect **only triggered by bipolar operation** (body diode conducting) **and saturates** after limited time

Driven by electron hole recombination, **stacking faults grow in the drift zone and act as a barrier for current**



What is the impact of bipolar degradation in application?

Drift of $R_{DS(on)}$ and diode V_{SD} over operation time due to reduction of effective active area of the device

No other properties will change (e.g. V_{br}, $V_{GS(th)}$, …)

Bipolar degradation: Countermeasures

Infineon's strategy to tackle the effect

Dropping down defect density to avoid stacking fault growth

Avoiding recombination at stacking faults

Applying screening approach (as for gate oxide extrinsics)
as long as defect density is above a critical threshold

Outline

- Introduction into SiC specific failure modes
- Procedures for the qualification silicon power devices and their applicability to SiC
- Focus humidity testing
  - DC tests
  - AC tests
- Power cycling behavior of SiC
- Summary

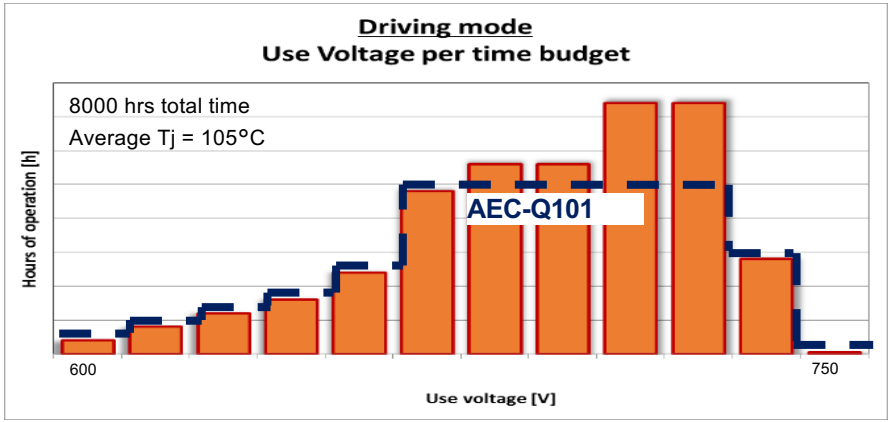
Robustness validation for Infineon's power modules

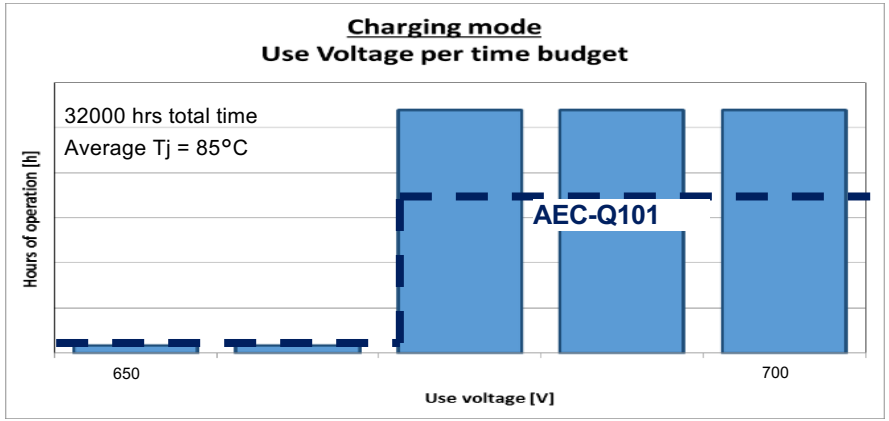
Test	Test conditions	Serial release: stress time	Robustness validation: stress time
HTRB	V_{DS} = 1080 V T = 150°C	1000h	+4000h
HTGS	V_{DS} = 0 V V_{GS} = +20 V/-20 V T = 150°C	1000h	+4000h
H3TRB	V_{DS} = 80 V T = 85°C rH = 85%	1000h	+2000h
HV-H3TRB	V_{DS} = 960 V T = 85°C rH = 85%	1000h	1000h +2000h
AC HTC	T_{cycle} = -20°C/85 °C rH = 93% V_{DS} = typ. (AC) f = typ. kHz	21d (only SiC)	120d

Robustness validation for Infineon's discrete devices

Stress test	Test conditions	Duration	
HTRB	V_{DS} = 1200 V; T_{vj} = 175°C; V_{GS} = 0 V	2000 h	Extended HTRB section
HTRB w/ negative voltage (blocking state)	V_{DS} = 1200 V; T_{vj} = 175°C; V_{GS} = -10 V	2000 h	
HTRB w/ negative voltage (blocking state)	V_{DS} = 1100 V; T_{vj} = 175°C; V_{GS} = -15 V	1000 h	
HTRB w/ pre-stressed parts	V_{DS} = 960 V; T_{vj} = 175°C; V_{GS} = 0 V w/ initial 0x and 10x short-circuit stressed parts	1500 h	
HTGS	V_{GS} = +20/-20 V constant; T_{vj} = 175°C	2000 h	Extended HTGS section
HTGS w/ pre-stressed parts	V_{GS} = +20/-20 V constant; T_{vj} = 175°C w/ initial 0x and 10x short-circuit stressed parts	1000 h	
HV-H3TRB	V_{DS} = 1200 V; T_a = 85°C; rH = 85%	2000 h	Humidity section
Dynamic H3TRB	T_a = 85ºC; rH = 85%; $V_{DC\ link}$ = 960 V; V_{GS} = +15 V/0 V; IL peak = 16 A; f_{SW} = 25 kHz; dv/dt = 70 V/ns	1000 h	
Dynamic Reverse Bias (DRB)	T_a = 25ºC; $V_{DC\ link}$ = 960 V; V_{GS} = +15 V/-5 V; dv/dt ~ 200 V/ns; f_{SW} = 100 kHz	1000 h	

Example from the car world - How xEV mission profiles impact qualification beyond standard





More operating modes in the same mission profile for the same product

Each mode operated at different voltages and temperatures

Compared to AEC-Q101 standard profile:

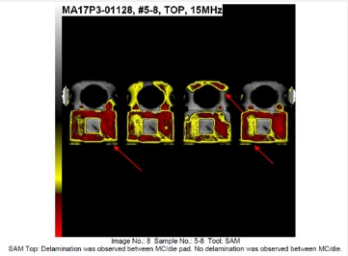
- More temperature cycles
- Longer HTRB hours
- High voltages, transients, overshooting
- New scenarios for climatic tests

AEC-Q101 is still necessary but no longer sufficient

Package test under standard and application relevant stress ➔ additional measures required to secure field stability

Temperature cycling

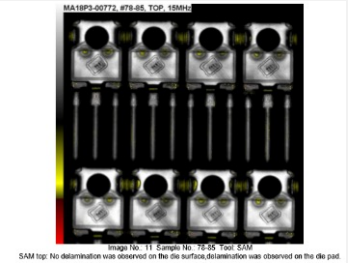
- 3rd party device rated with T_{jmax} = 200°C



1000 x TC 55°C … 150°C:

delamination between die pad and mold compound

- IFXdevice, rated at 175°C

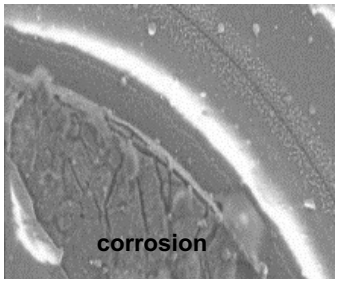


1000 x TC 55°C … 150°C

No delamination between die pad and mold compound

AEC Q101 qualified SiC 3rd party device

H3TRB AEC-Q101	PASS
High Voltage H3TRB	FAIL



Infineon part with special chip protection technology

H3TRB AEC-Q101	PASS
HV-H3TRB	PASS
Dyn-H3TRB	PASS

Outline

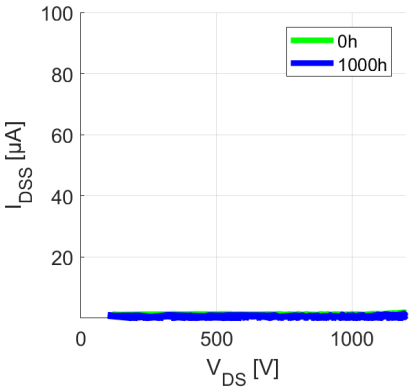
- Introduction into SiC specific failure modes
- Procedures for the qualification silicon power devices and their applicability to SiC
- Focus humidity testing
  - DC tests
  - AC tests
- Power cycling behavior of SiC
- Summary

DC tests under humidity stress - HV-H3TRB

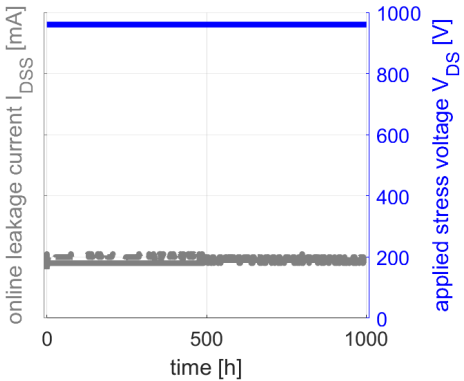
- based on field experience and acceleration models, 1000h of HV-H3TRB are more then enough to secure operation e.g. in Solar applications

Test	No. of DUT	Test conditions	stress time – serial release
HV-H3TRB	72 (std.) 700 (RV)	V_{DS}= 960 V, T= 85°C, rH= 85%	1000h

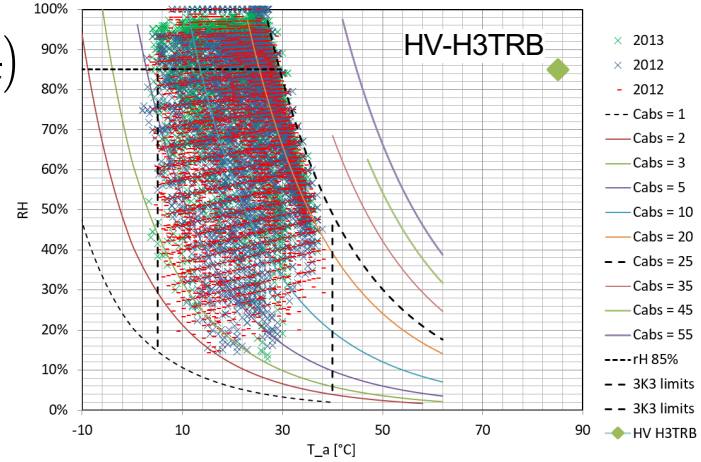
- Acceleration factor as known from Si: $k = \left(\frac{RH}{RH_{ref}}\right)^{-4.2} e^{\frac{Ea}{kB}\left(\frac{1}{T}-\frac{1}{T_{ref}}\right)}$
- No fails discovered during qualification, leakage currents are highly stable over stress time



Leakage current curves before and after stress



Monitoring of online parameters during stress.

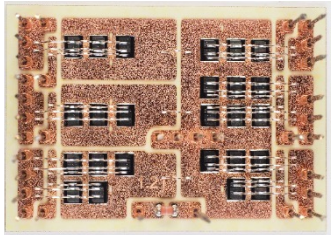


Climate data from Chenai Airport

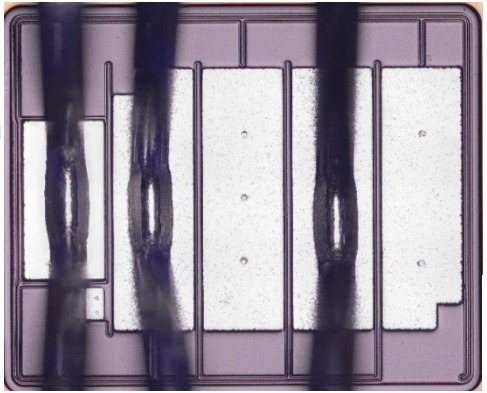
DC tests under humidity stress - HV-H3TRB

Test	Chips in test	Test conditions	stress time – Serienfreigabe	Robustness validation
HV-H3TRB	72 (std.) 700 (RV)	V_{DS}= 960 V, T= 85°C, rH= 85%	1000h	1000h +2000h

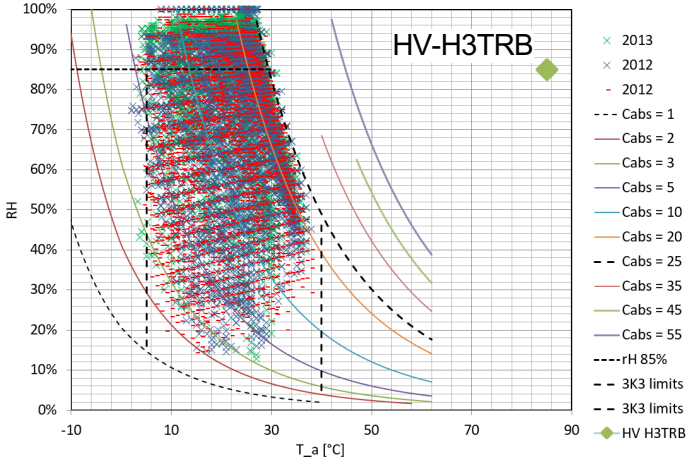
- Stress-setup for robustness validation:
  - special module design to enable testing of a complete wafer
  - a productive wafer was assembled into 28 Easy2B modules
- Result
  - no fails until 1000h (700 chips!)
  - 325 chips prolonged until 3000h
    - no systematic EoL mechanism
    - no signs of degradation visible after 3000h of stress



Specially designed mass test module



CoolSiC™ MOSFET after 3000h HV-H3TRB



Climate data from Chenai Airport

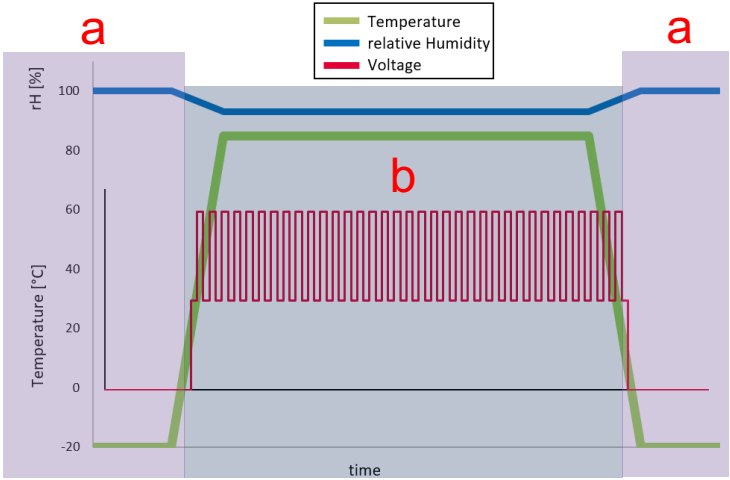
Summary

No EoL mechanism in HV-H3TRB found even with long stress and high statistics

How to verify SiC devices against corrosion effects in high humidity environment? – AC testing required

- New, material specific failure mode which is sensitive to condensation on the chips surface
  - Discrete parts
    - slow permeation of humidity through mold compound, no special precaution needed
  - Modules
    - The silica gel is very permeable to humidity
    - edge termination of chip has to be protected additionally to allow operation even under environmental conditions causing bedewing
  - ➔ Solution: thick HP layer in edge termination area
  - ➔ Rolled out in all relevant SiC technologies from Infineon

- Passivation is assessed with the AC-HTC (**a**lternating
- **c**urrent – **h**umidity and **t**emperature **c**ycles) consisting of two different phases:
  a. T_a<0°C & high humidity: aims to trigger condensation on the chip surface is triggered
  b. T_a>0°C: device under stress is actively switched with frequencies and voltages similar application conditions.
- Std. duration of 21d, extend to 120d for robustness validation.
- Even after 120d, there are no signs of degradation visible



Outline

- Introduction into SiC specific failure modes
- Procedures for the qualification silicon power devices and their applicability to SiC
- Focus humidity testing
  - DC tests
  - AC tests
- Power cycling behavior of SiC
- Summary

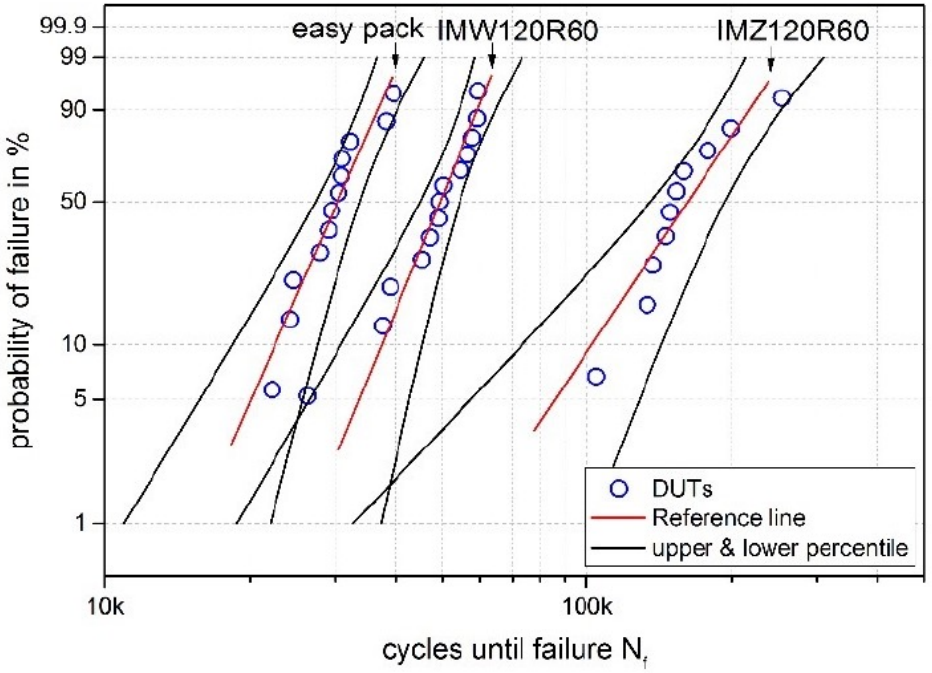
What are the major findings regarding power cycling of SiC power devices

- Under identical assembly conditions SiC chips in power modules show inferior cycling stability compared to silicon
  - Failure mode in modules mostly die attach delamination due to the E-modulus of SiC
- Known technologies to improve power cycling like sintering and copper wire bonds work accordingly for SiC as well
- In discrete devices preliminary studies show that bond wire degradation is the major failure mode
  - Typically much higher cycling stabilities compared to modules are obtained
  - Cycling stability can be influenced by a proper bond wire strategy

Power cycling as lifetime limiting mechanism is very relevant for SiC, in contrast to IGBT's it can be improved also by chip area considerations

Most recent results regarding power cycling of SiC chips

- Source : Schwabe et al. “Reliability investigation of SiC MOSFETs under switching operation in various packages TU Chemnitz, presented at CIPS 2022
- Devices under test (chips always identical)
  - Baseplate free module, standard solder technology (easy pack)
  - Discrete device in TO247-3, standard die attach, 2 thick wires for source bond (IMW120R60)
  - Discrete device in TO247-4, 3 thin wires for source bond (IMZ120R60
- Results for discrete devices need more statistics and deeper analysis



Outline

- Introduction into SiC specific failure modes
- Procedures for the qualification silicon power devices and their applicability to SiC
- Focus humidity testing
  - DC tests
  - AC tests
- Power cycling behavior of SiC
- Summary

Reliability is crucial for the roll-out of WBG power devices

- Experience with the first WBG devices in the field revealed several WBG-specific failure modes
- Early device generations showed several weak points with respect to stability → customers are concerned
- Today's used standards for reliability testing are based on silicon models and experience → impact of the different material aspects need to be addressed
- The general maturity of the technology and the used material is by far not at the level of silicon → additional measures needed to secure adequate field reliability

Dedicated quality assurance program needed to guarantee field stability, standardization needs to be accelerated

Thank you very much for your kind attention !

Questions ?