Transient-voltage specification and reliability for GaN power devices

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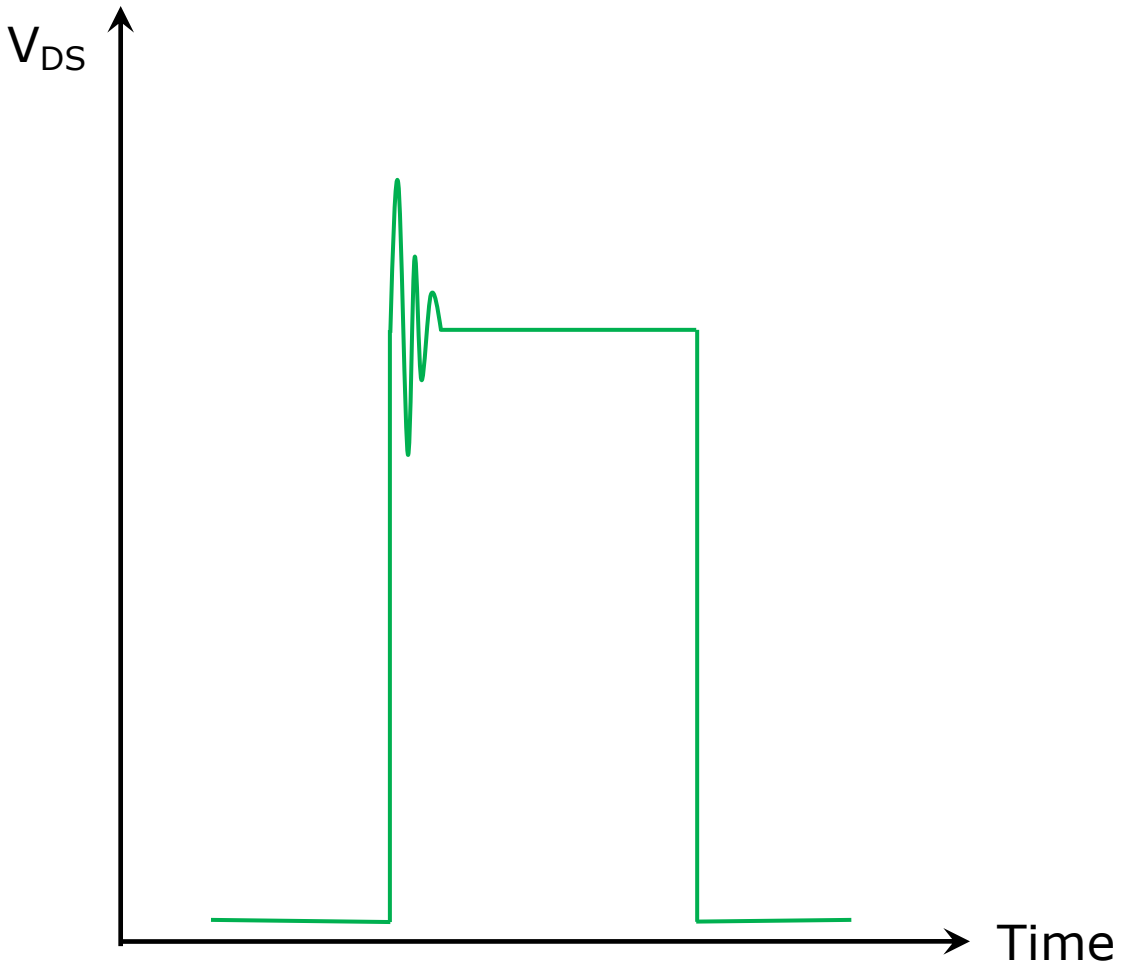
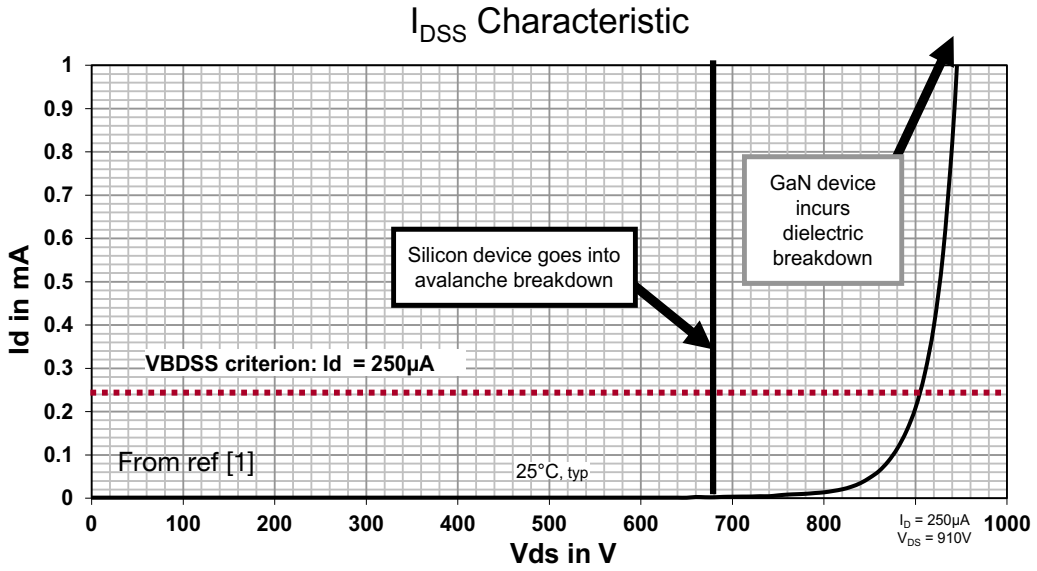
Topics addressed



- Background
  - Transient ability of GaN
  - Importance of specifying
  - Common traits of transients
- Datasheet specification
  - New JEDEC guideline JEP186
  - Specifying transients
- Reliable transient operation
  - Failure Mechanisms
  - Switching stresses
  - Transient every cycle (LMG3410R150)
  - Occasional line-voltage surge

GaN opens up transient withstand ability for power converters



Further reading

[1] T. McDonald and S. W. Butler, "Progress and Current Topics of JEDEC JC-70.1 Power GaN Device Quality and Reliability Standards Activity: Or: What is the Avalanche capability of your GaN Transistor?," *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021

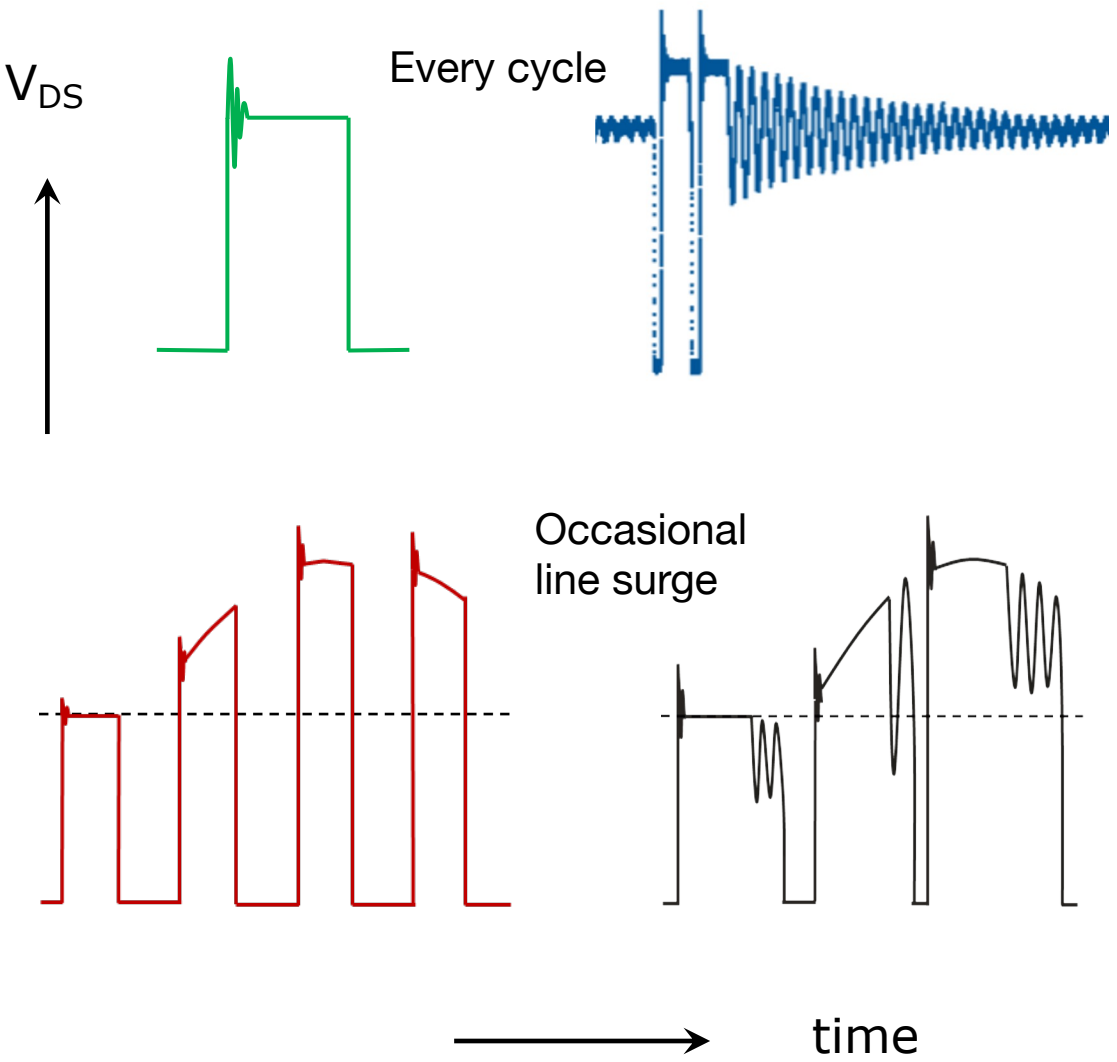
[2] S. R. Bahl and P. Brohlin, "A New Approach to Validate GaN FET Reliability to Power-Line Surges Under Use-Conditions," 2019 IEEE International Reliability Physics Symposium (IRPS), 2019, pp. 1-4, doi: 10.1109/IRPS.2019.8720479.

[3] R. Zhang, J. Kozak, Q. Song, M. Xiao, J. Liu and Y. Zhang, "Dynamic Breakdown Voltage of GaN Power HEMTs", 2020 66th IEEE International Electron Devices Meeting (IEDM), pp. 23.3.1-23.3.4, Dec. 2020.

[4] J. P. Kozak, Q. Song, R. Zhang, J. Liu and Y. Zhang, "Robustness of GaN Gate Injection Transistors under Repetitive Surge Energy and Overvoltage," 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, pp. 1-5, doi: 10.1109/IRPS46558.2021.9405173.

- Silicon Power Vertical FET
  - Maximum blocking voltage is Avalanche Limited
- Lateral GaN HEMT [1-4]
  - Today, none have avalanche capability
  - Instead, withstand voltage (V_{DS})
    - Typically much less than voltage at which irreversible failure occurs
  - Also, displays a transient withstand voltage, $V_{DS(tr)}$, whereby GaN withstands a higher voltage for short durations
- This talk will examine how to specify a transient withstand voltage.
- A transient reliability methodology will then be examined using the TI GaN LMG3410R150

Importance of specifying transients



- Transients (ringing) are common in switching power supplies
  - Every cycle: parasitics in the system layout causing transient for FET turn-off
  - Occasional: power line surges causing transient for both FET turn-on and off
- Concept of design margin and robustness also can be based on increased capability for short periods
- Designing a FET to handle the maximum transient blocking value all the time could result in over-specifying and over-paying for the FET

JEDEC: Addressing breadth of mechanisms & specifications with one Datasheet Guideline

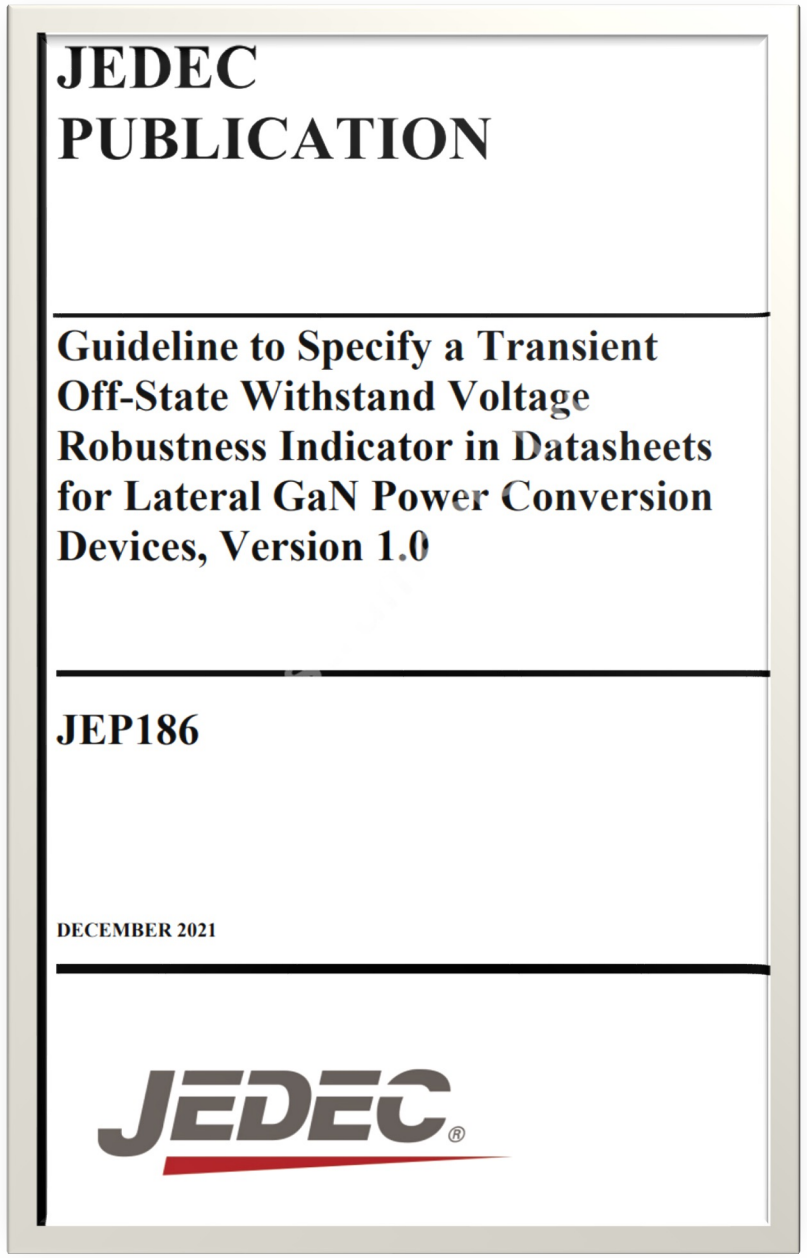
Where to begin?

- Different possible specification techniques for capturing the transient nature exist
  - Opinions vary on what is most *useful to user*
  - Several already in use in existing datasheets
  - Independent of the specific lateral power HEMT architecture
- Need a guideline for different specification techniques that are all equally valid for providing a robustness indicator for a transient off-state withstand voltage parameter ($V_{DS(tr)}$) in datasheets.

How did the JEDEC JC-70.1 committee go about it?

- Different possible specification techniques for capturing the transient nature were identified.
- All possess the following traits
  - Maximum transient drain-source blocking voltage
  - a pulse width in time or damping time
  - number of pulses, damping time behavior, or imply rare event or atypical occurrence
  - temperature

First Transient Document



- JEDEC JC-70.1 recently released a new guideline consistent with their guiding principle:
  - Guidelines document intended to be flexible, while being useful
  - Consider as a minimum best practices guideline
  - Shouldn't constrain further best practices
- For datasheets
- Off-state
- Transient Withstand Voltage ($V_{DS(tr)}$)
- Robustness indicator
- Lateral GaN Power Conversion Devices
- https://www.jedec.org/standards-documents/docs/jep186
  - Free Download
  - Must Register (for free)

Examples from JEP186

3.3 Examples of Transient Specifications

The following examples demonstrate different ways to specify the four traits specified in 3.1. The examples also show different ways of using clauses, footnotes, and references to provide details. The use of footnotes, figures, and references are not constrained to only the type of Examples provided below. Example 2 and Example 3 specify the same information, but Example 2 uses only line wording while Example 3 uses a footnote.

Example 8 demonstrates how to use a figure (see Figure 1) to specify the information of 3.1 in a graphical form. Example 1 and Example 8 provide the same information, but one is in tabular form and one is in graphical form. For damping types, the details for the damping may be in a clause, a footnote, part of the datasheet line item, or in a figure or graph as demonstrated below, or in a reference.

Example 1: Specified with damping and use of a footnote to provide further details

$V_{DS(tr)}$	800V (1)

(1) Voltage must be damped to less than 720V in 1µsec, 25 °C

Example 2: Non-repetitive pulse

$V_{DS(tr)}$	750V Not-repetitive Pulse for ≤1us at 25 °C 650V Non-repetitive Pulse for ≤1us at 125 °C

Example 3: Non-repetitive pulse with use of a footnote

$V_{DS(tr)}$ (1)	750V at 25 °C 650V at 125 °C

(1) Non-repetitive Pulse for < 1us

Example 4: Total # of Pulses

$V_{DS(tr)}$	800V for 10,000 5ms pulses at 150 °C

Example 5: Total Pulse time with use of a clause in a footnote

$V_{DS(tr)}$	800V for ≤1 hour total time at 25 °C (1)

(1) Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation

Example 6: Specified using a rare event clause in Footnote; Temperature specified in Footnote

$V_{DS(tr)}$	800V (1)

(1) Considered a rare event occurrence; 25 °C

- Table Examples
- Can use clauses, footnotes, or references to provide user more details

Graphical Example

3.3 Examples of Transient Specifications (cont'd)

Example 7: Details provided in an App Note

$V_{DS(tr)}$	800V (1)

(1) For further details, see App Note APN1234

Example 8: Example of specifying $V_{DS(tr)}$ with damped oscillations in a Figure (see Figure 1)

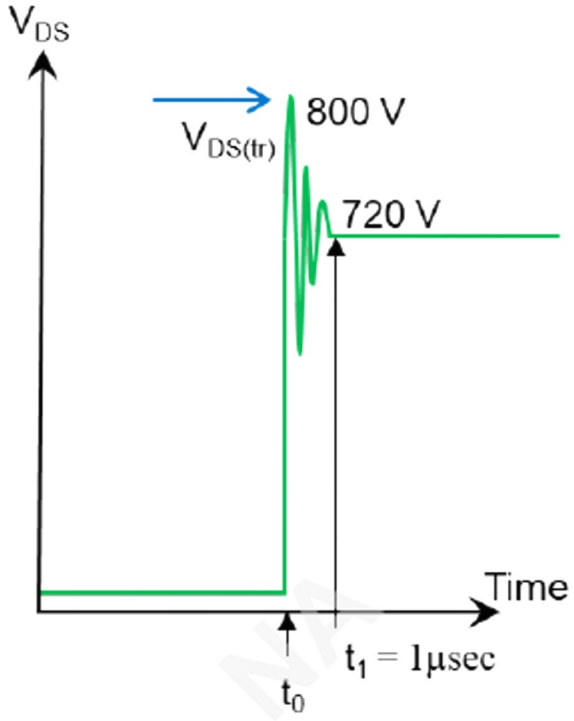


Figure 1 — Voltage must be damped to less than 720V in 1 µsec

- Can use a Graphic
- Can specify damping
- Example use of reference to an application note

JEP186 Scope (What is and is not; In-Bounds and Out-of-Bounds)

This guideline describes different techniques for specifying a Transient Off-state Withstand Voltage Robustness Indicator in datasheets for lateral GaN power conversion devices. This guideline does not convey preferences for any of the specification types presented, nor does the guideline address formatting of datasheets. This guideline does not indicate nor require that the datasheet parameters are used in production tests, nor specify how the values were obtained.

This guideline is not intended to provide a methodology to convert between the different specification types, nor imply any of the robustness indicators in this guideline are used to calculate lifetimes. This guideline is not meant to imply the robustness indicators are for unlimited pulses or cycle-by-cycle transient withstand voltage excursions. This guideline applies only to off-state, and does not apply to other operating modes, such as hard switching, which may place a different type of stress on the device.

However, this guideline **does not preclude** the specification of a transient withstand voltage for unlimited pulses or cycle-by-cycle. This guideline also does not preclude specifying a transient voltage for other operating modes, such as hard switching or line surge operation. This guideline also **does not prevent** having a transient voltage parameter on a datasheet which is tied to detailed lifetime and reliability models.

From specification to reliability

JEP186 does not preclude transient reliability, e.g.

- Ringing on every cycle for the lifetime
- Hard-switching operation under occasional extreme conditions, e.g. to line voltage surges from lightning strikes.

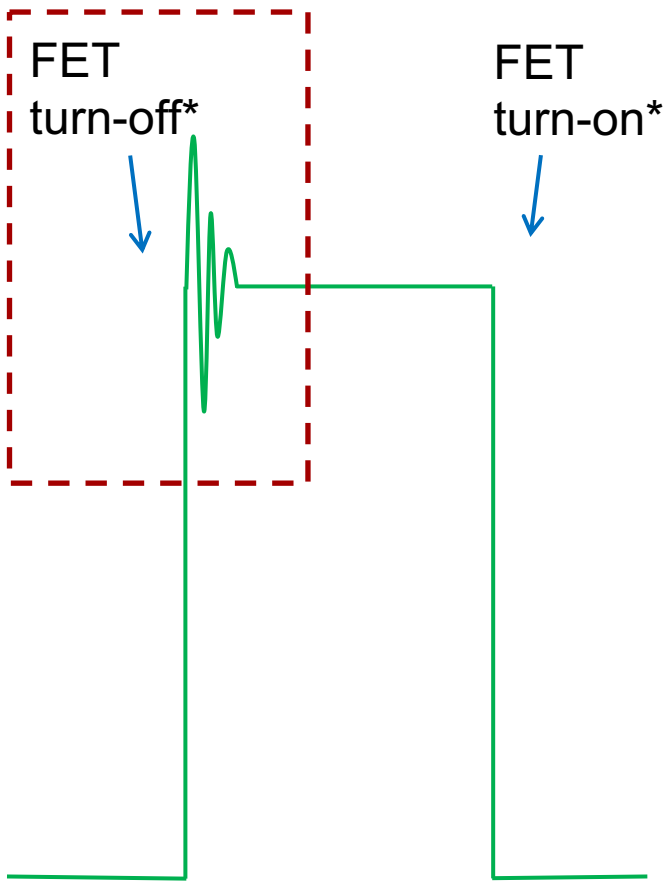
We now show a methodology to evaluate the reliability for transient operation, presenting some examples for TI GaN

We also show an example of how to specify hard-switching capability for occasional line surges

A failure mechanisms-based approach

GaN failure mechanisms (off-state ringing)

- Time-dependent breakdown (TDB)
- Charge trapping
  - Increase in dynamic $R_{DS(ON)}$ (leading to lower efficiency)
- Hot-carrier wearout
  - Is important for hard turn-on, which is not where this ringing occurs
  - Not significant for the turn-off transition or for soft-switching
  - Hot-carrier wearout is treated separately in [1,2]

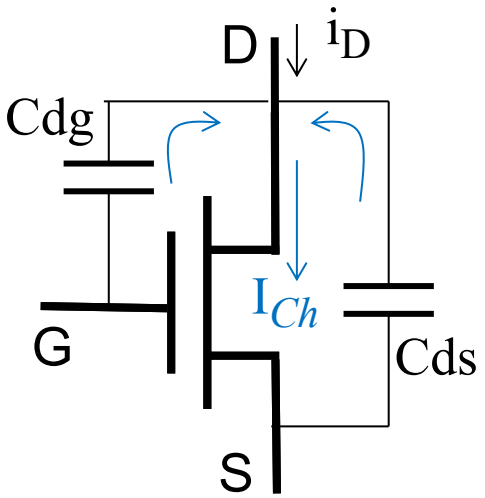


*Sequencing shown for the low-side FET in a boost converter. It can be different for other topologies.

[1] A. Ikoshi et al., "Lifetime Evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under Practical Switching Operations", *IEEE IRPS*, p. 4E-2.1, 2018.
[2] S. R. Bahl et al., "*A Generalized Approach to Determine the Switching Lifetime of a GaN FET*", IEEE IRPS 2020, available at www.ti.com/lit/ml/slyy196/slyy196.pdf

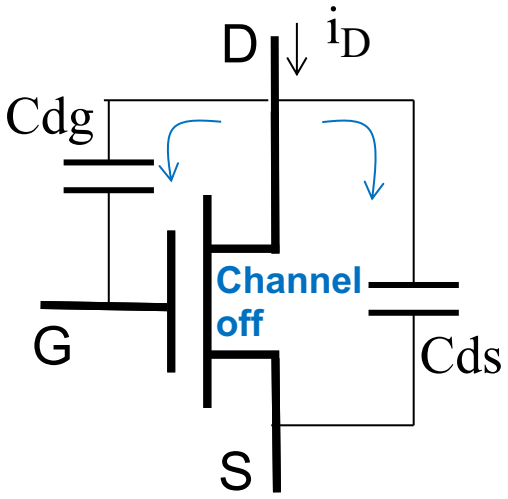
Hot-carrier wearout is not significant for turn-off

Hard turn-on
Coss discharges and Id flows through the channel, increasing hot-carrier wearout

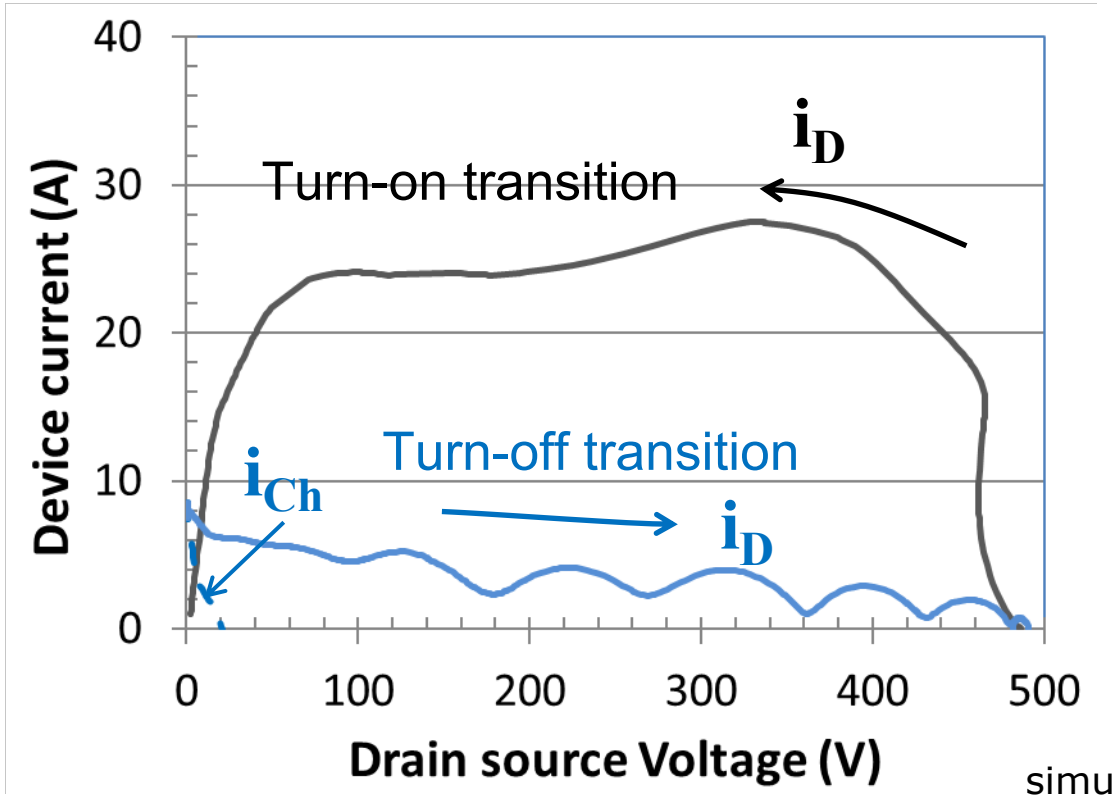


Hard turn-off
Channel turns off, then Id charges Coss

Soft turn-off
Channel is already off, then Vds is raised by the circuit



LMG3410R070, 480V, 8A, 125C, 100 kHz, 100 V/ns



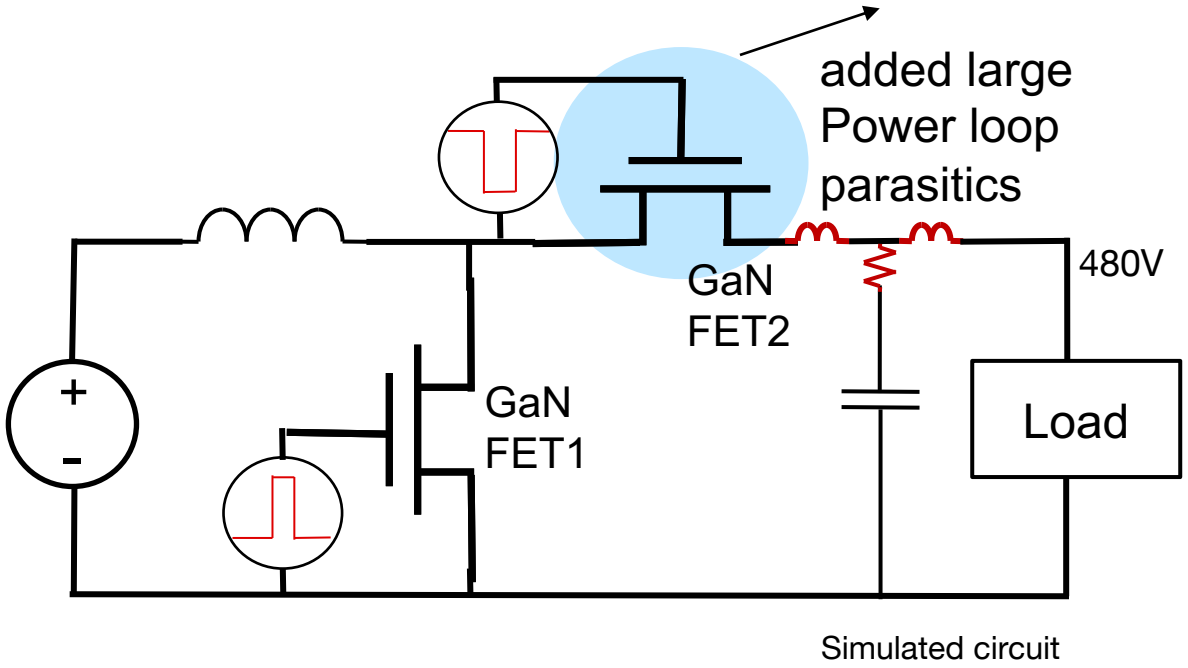
simulation

Hot-carrier wearout model [2] for above:
MTTF hard-turn on transition: 8.1 x 10^5 yrs
MTTF turn-off transition: 7.3 x 10^{20} yrs

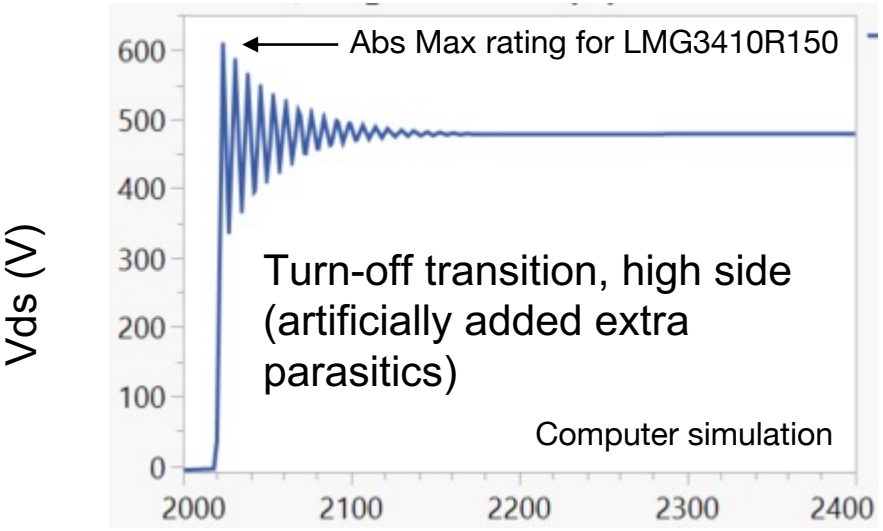
[2] "*A Generalized Approach to Determine the Switching Lifetime of a GaN FET*", IEEE IRPS 2020, available at www.ti.com/lit/ml/slyy196/slyy196.pdf

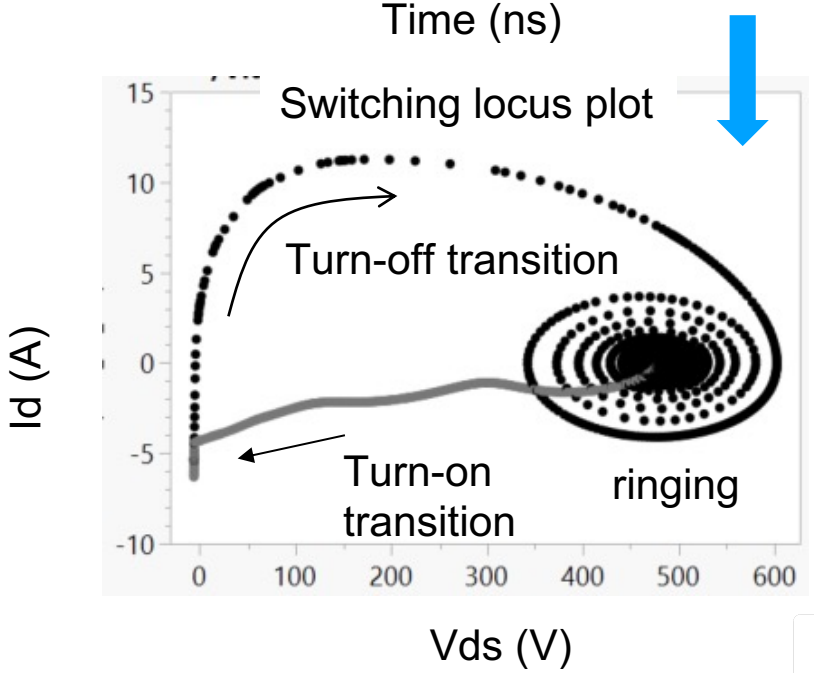
Creating additional ringing in a circuit

- Use large values of parasitic elements
- Tuned the parasitics to obtain a 600V ring, damped in tens of ns.
- The ringing shown is artificially created for the purpose of providing an example

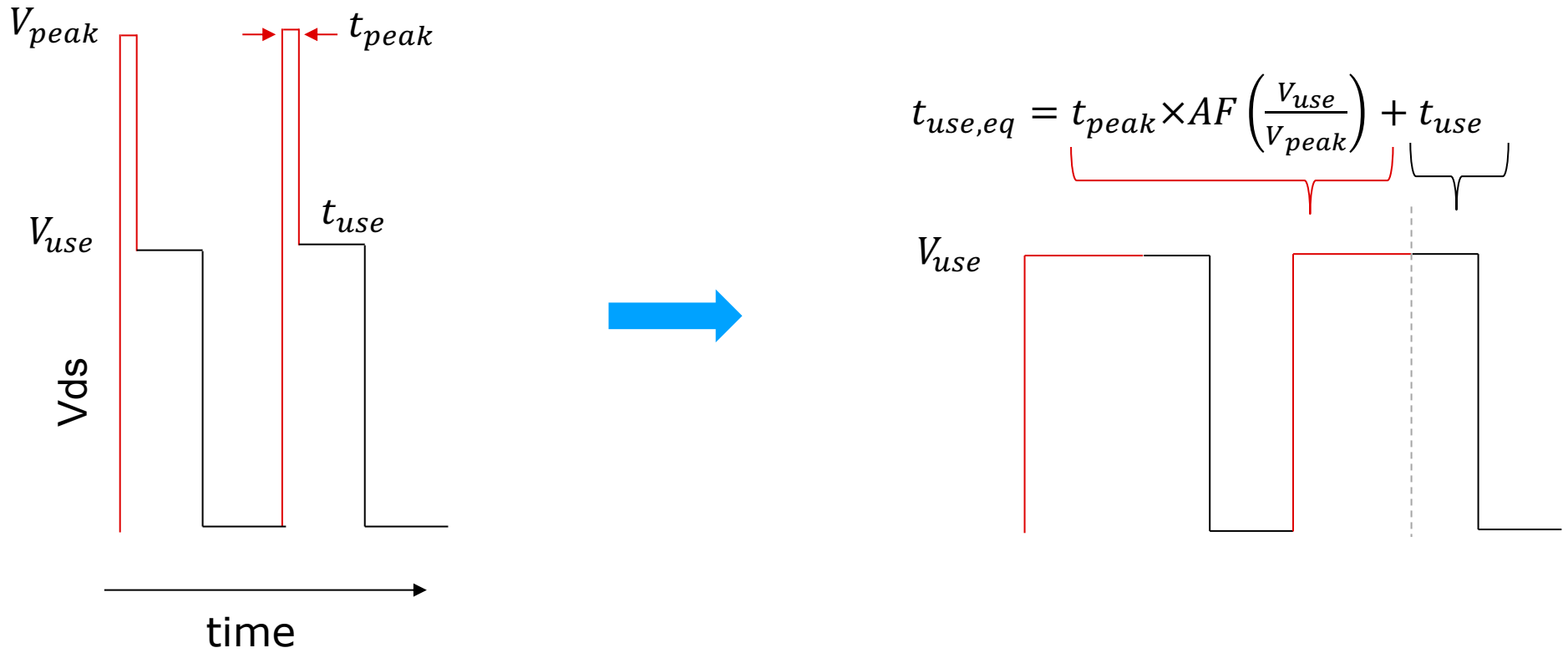


Simulated circuit





Treating Time Dependent Breakdown during off-state ringing

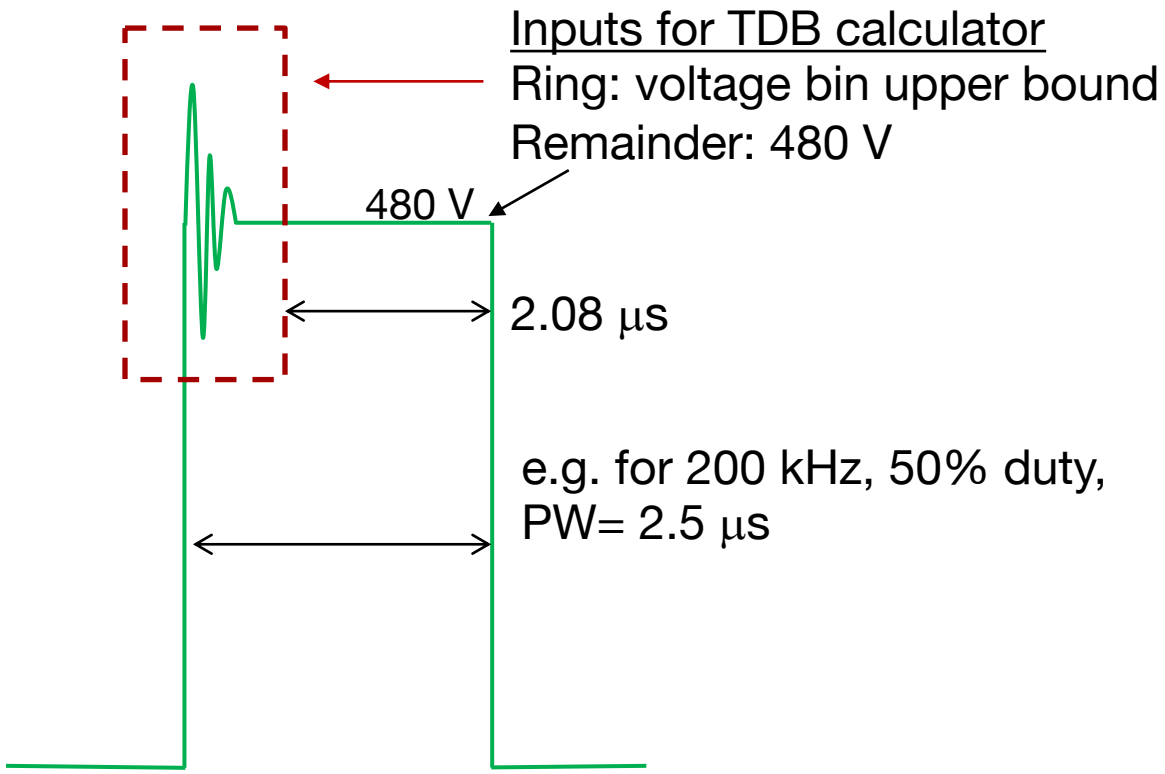


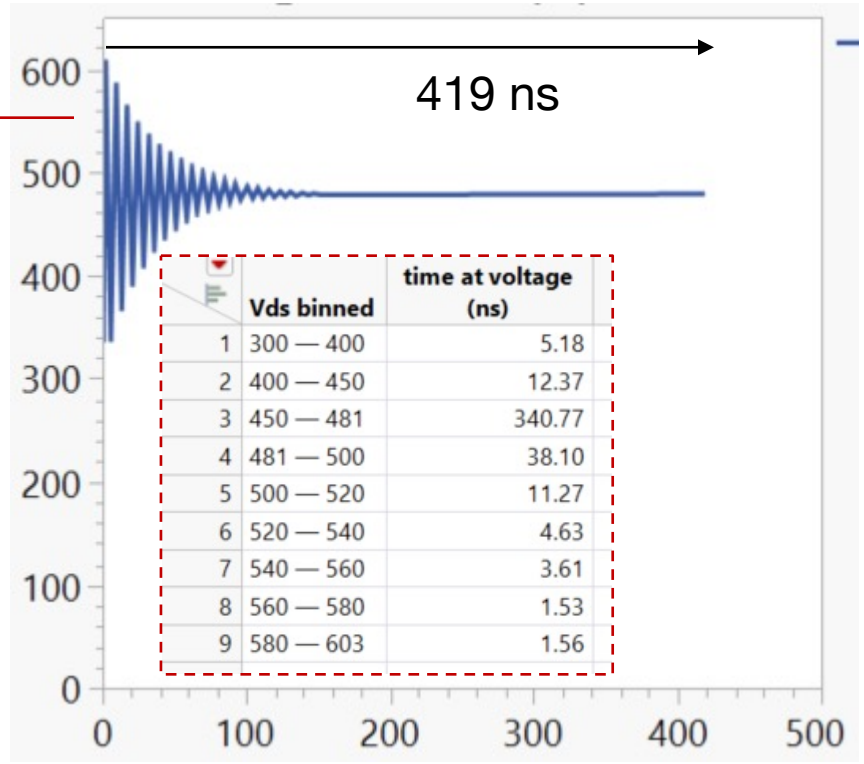
Prior art [3]:

- Modeled as Time Dependent Dielectric Breakdown (TDDB) using the V-model
- TDDB V model is per JEP122G, eq. 5.1.4: $TTF = A_o * \exp(-\beta V) * \exp(E_{aa} / kT)$
- TDDB calculation based upon the equivalent time at use voltage

[3] C. S. Whitman, "*Methodology for predicting off-state reliability in GaN power transistors*", Microelectronics Reliability, v54, p. 354, 2014

Off-state wearout (Time Dependent Breakdown) calculation





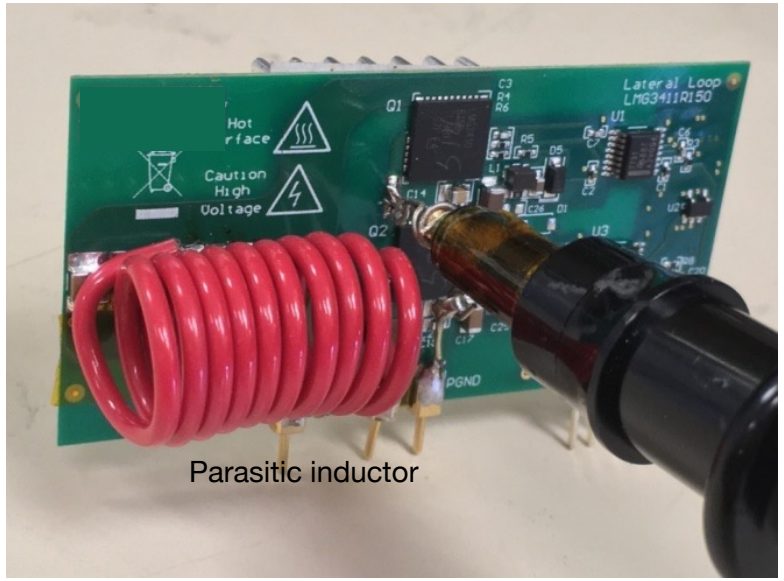
	Vds binned	time at voltage (ns)
1	300 — 400	5.18
2	400 — 450	12.37
3	450 — 481	340.77
4	481 — 500	38.10
5	500 — 520	11.27
6	520 — 540	4.63
7	540 — 560	3.61
8	560 — 580	1.53
9	580 — 603	1.56

TDB FIT rate calculation for LMG3410R150: 10 yrs, 480V, 125C, 200 kHz, 50% duty

- With severe ring: 6.55 x 10^{-2} FIT
- With no ring: 6.41 x 10^{-2} FIT

→ Ringing has minor effect on TDB FIT rate (1 FIT = 1 fail in 10^9 hrs)

Creating a dynamic HTOL (DHTOL) test with ring

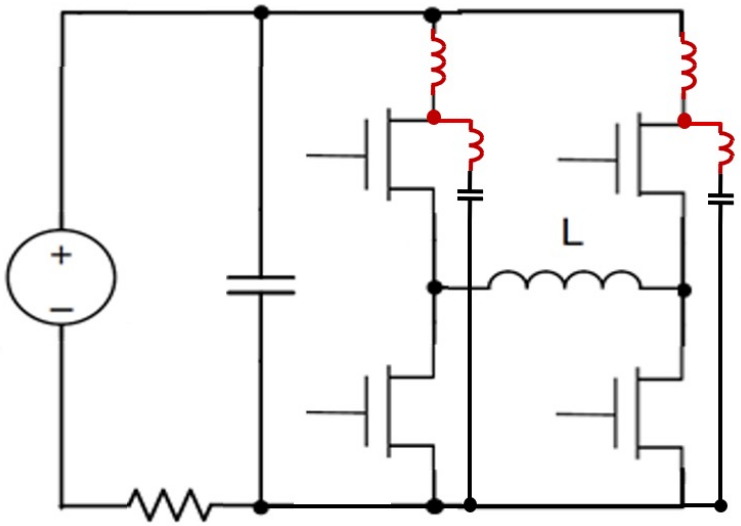


Parasitic inductor

Parasitics were added to a half-bridge card to create additional ringing

- Added inductance to the power loop
- Added inductance to the decoupling capacitors

2 half-bridge cards run in an H-bridge configuration with both hard and soft switching



Decoupling capacitor

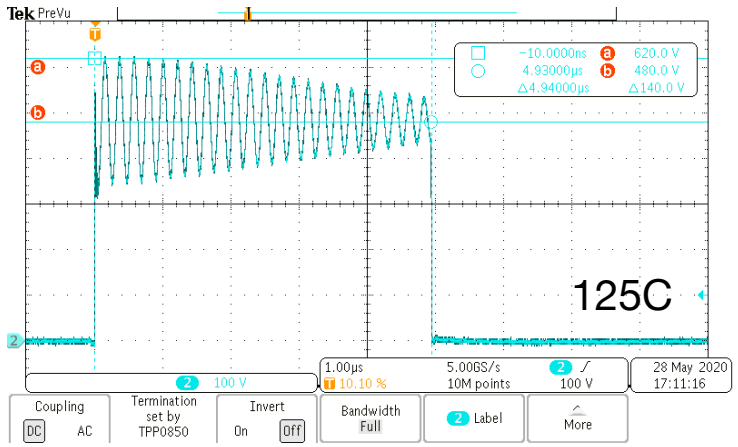
Loss sensing resistor

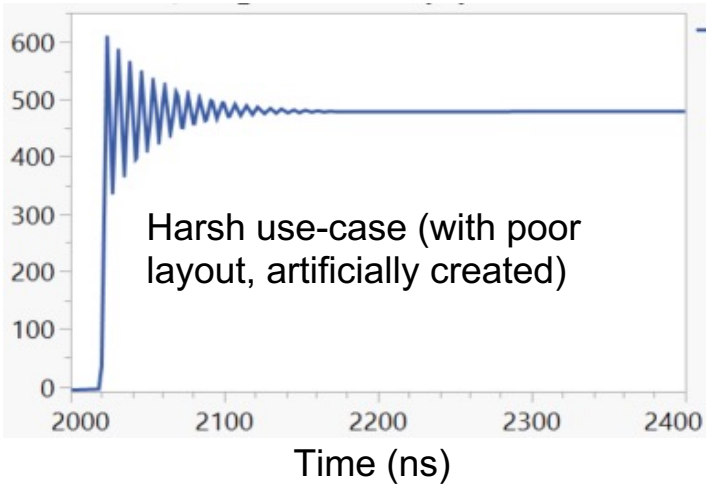

H-bridge rack

Note: shown for demonstration purposes, not as a recommendation or best practice of how to add parasitic elements

DHTOL ring covers the harsh use-case ring

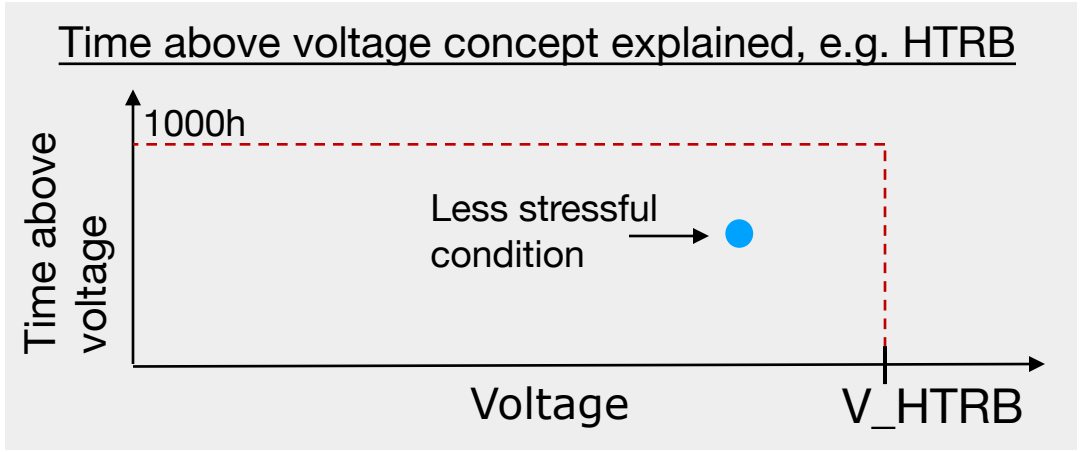
H-bridge board DHTOL: 480V, 5.4A, slew rate 136 V/ns (LMG3410R150)



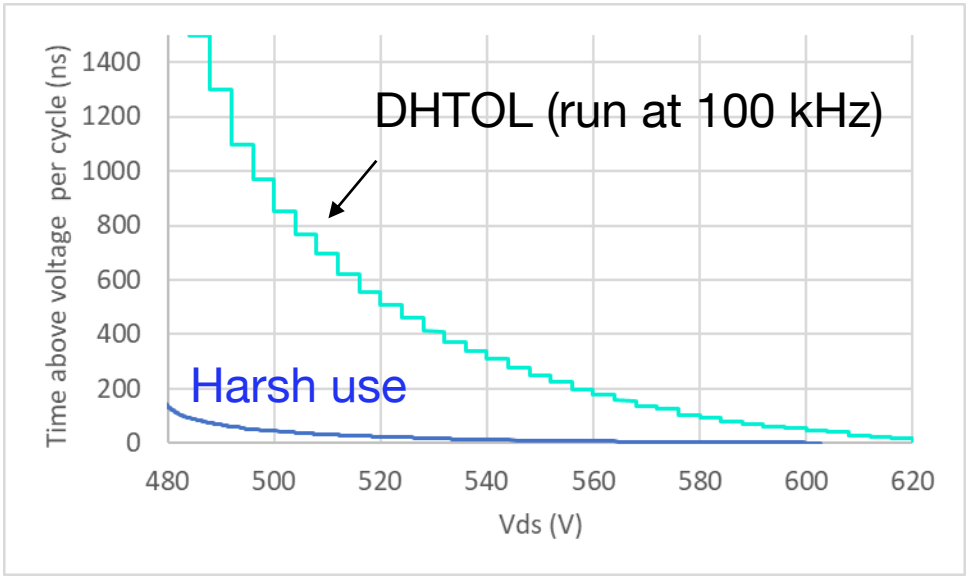


Time above voltage plot

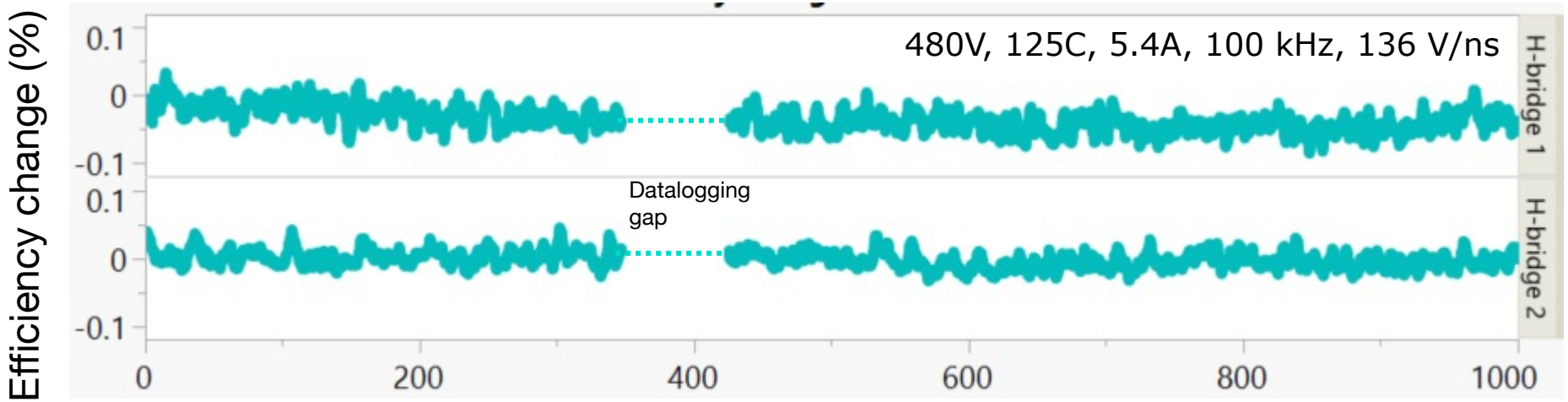
2X for 200 kHz = 2 ring cycles at 100 kHz



DHTOL test is more stressful



DHTOL results



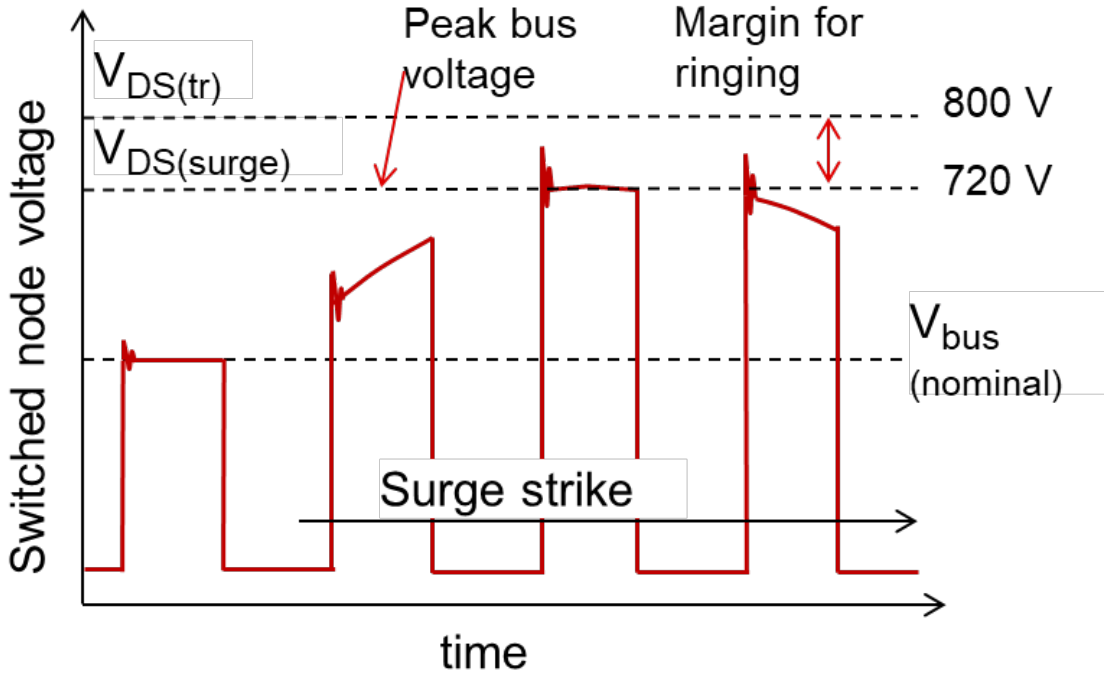
4 devices per H-bridge

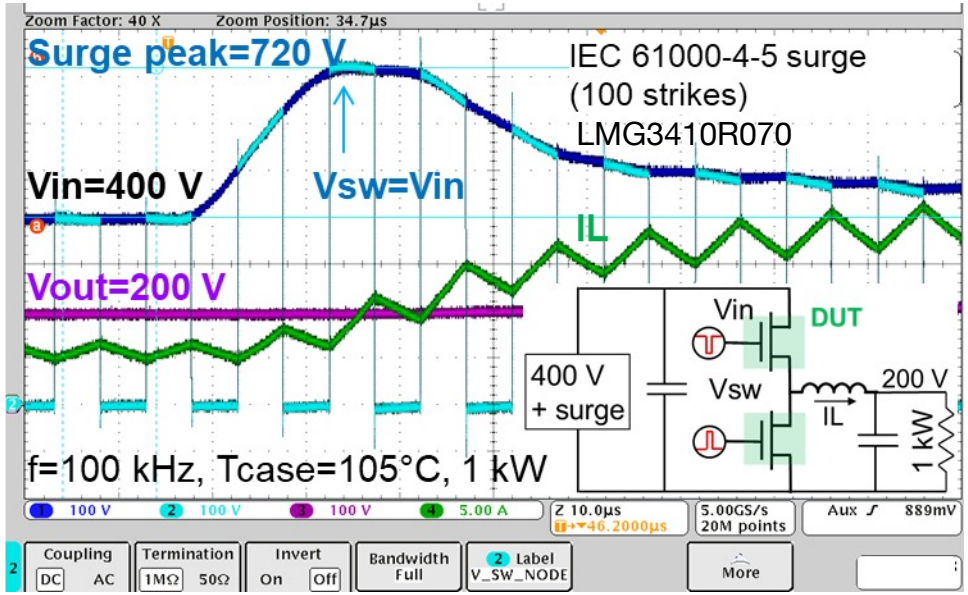
Stable DHTOL efficiency demonstrates reliability at power supply level in the presence of ringing

- No increase in dynamic Rds-on from the repetitive (every-cycle) transient
- Stable third quadrant operation
- No hard-commutation (reverse-recovery) issue
- No Miller shoot-through from high slew rate
- No adverse interaction with other power supply components

Specification of line surge in TI datasheet

- JEP186 does not preclude specifying a transient voltage "*… for other operating modes, such as hard switching or line surge operation*"
- TI datasheet specifies $V_{DS(surge)}$ for hard-switching turn-on and $V_{DS(tr)}$ for turn-off ring during line surge, making it straightforward to design surge-robust power supplies
- TI GaN is rated to hard-switch through bus surge voltages upto 720 V.





"A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions", IEEE IRPS 2019, at www.ti.com/lit/ml/slyy162/slyy162.pdf

Summary: GaN enables transient ability in systems

- Transient voltages occur in switching power systems
- GaN FETs have transient voltage withstand ability which can allow more flexibility (and lower cost) in system design.
- Industry GaN datasheets include transient specifications
- The GaN industry has recently released a guideline, JEP186, on specifying a transient off state withstand voltage robustness indicator in datasheets
- A ring (voltage transient) on every cycle has reliability implications
- A methodology is introduced to validate reliability for ringing on every cycle: the part needs to have the desired lifetime to the failure mechanisms, and needs to pass dynamic HTOL.
- LMG3410R150 TI GaN parts are reliable to ringing – they have good TDB lifetime for ringing, and pass DHTOL testing to a ring that is harsher than will be seen in operation. Harshness was shown using a time-above-voltage concept.
- Transient operation for occasional extreme voltage line-surges was also reviewed, demonstrating the ability of GaN to switch through these events.