Getting the most performance out of the latest generation SiC cascode FETs

Pete Losee

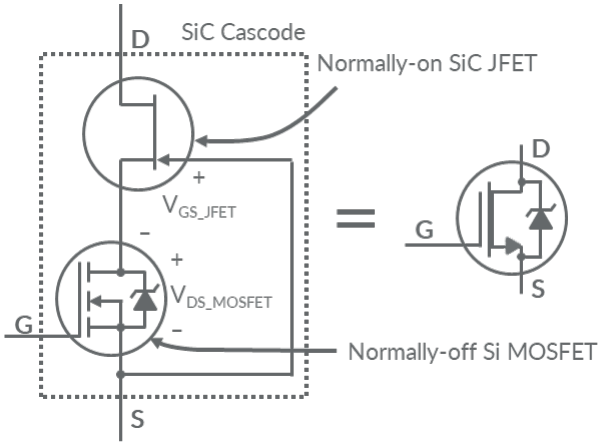
(UnitedSiC is now) Qorvo

Outline

- SiC cascode introduction
- Gen 4 SiC FETs set new performance benchmarks
- Design examples with new 750V SiC FETs, TPPFC, LLC

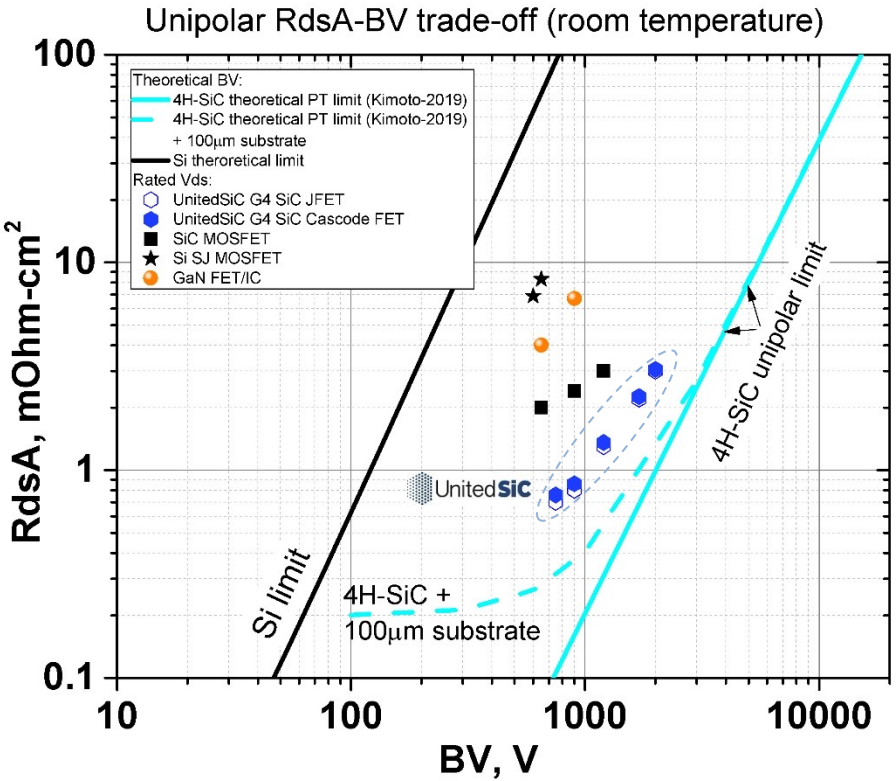
SiC cascode FET

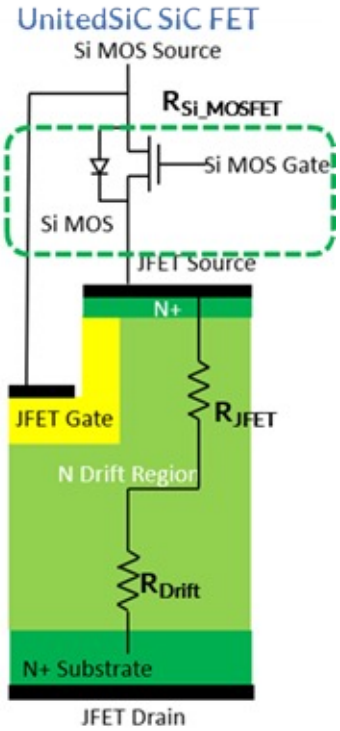
- Cascode is a source-switched SiC JFET
  - Inverse of the MOSFET drain-source voltage across the JFET gate-source
  - Blocks forward current when MOSFET gate is off
- JFET is fully on with its $V_{GS} \approx 0$
  - When MOSFET is on
  - When reverse current flows, regardless of MOSFET gate voltage
- Low voltage (20-30V) Si MOSFET Rds is <10% of the JFET resistance



- Lowest R_{On} x A
- Compatible with Si or SiC gate drive, 0-12V, 0-15V etc. drive, V_{th}=5V
- Reduced die size, low E_{oss}, C_{oss}
- Excellent integral diode with low V_F (1.0-1.5V typical) and low Q_{rr}

Qorvo/UnitedSiC technology approaching "unipolar limit"





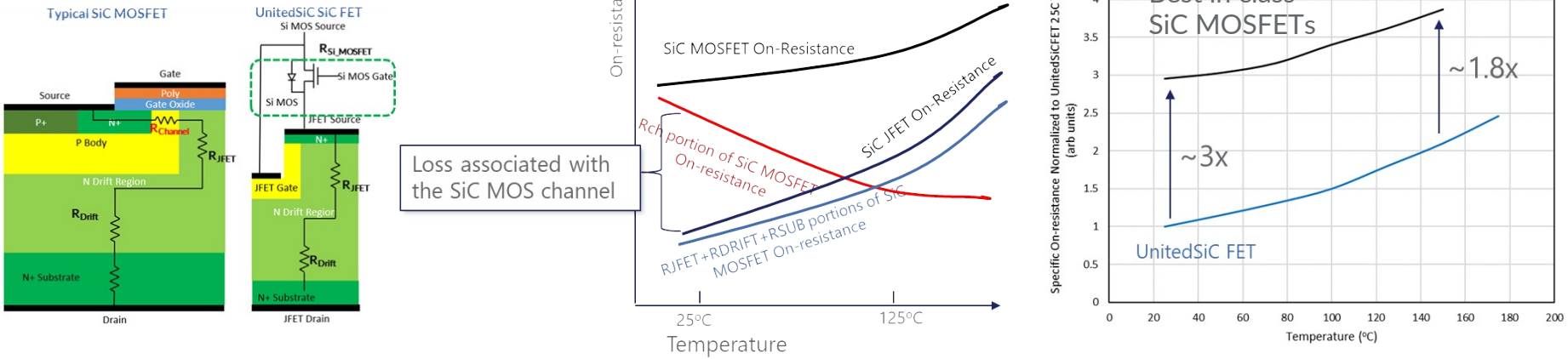
Gen 4 JFETs

- Trench structure with reduced cell pitch
- Optimized drift/spreading layers
- Reduced substrate thickness

750V SiC JFET:

$R_{On,sp}$ = 0.7mOhm-cm^2

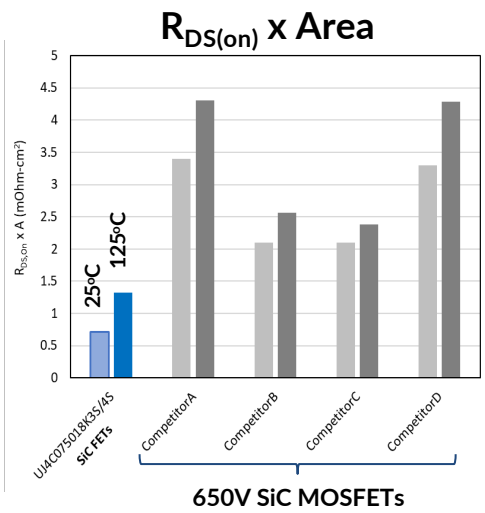
Gen 4 750V SiC FETs
Best in class $R_{On,sp}$ across temperature



650V SiC MOSFETs vs. 750V UnitedSiC UJ4C FETs

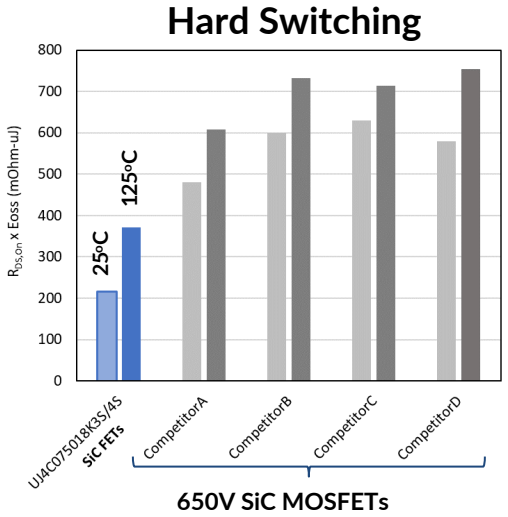
- Gen 4 FETs exhibit stronger positive temperature coefficient (TC) vs. SiC MOSFET competitors but offer lower $R_{DS,On}$ per unit area across useful temperature range
- Smaller SiC die size for given on-resistance -> Lower Q_{oss}

Gen 4 750V SiC FETs - Figures of Merit



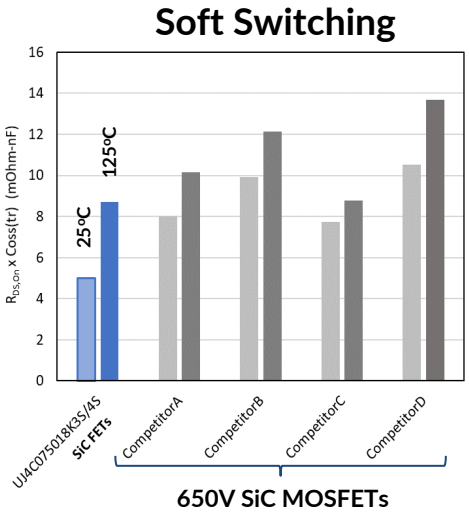
Benefit

- **Lowest conduction losses** across useful temperature range, for a given footprint or package type



Benefit

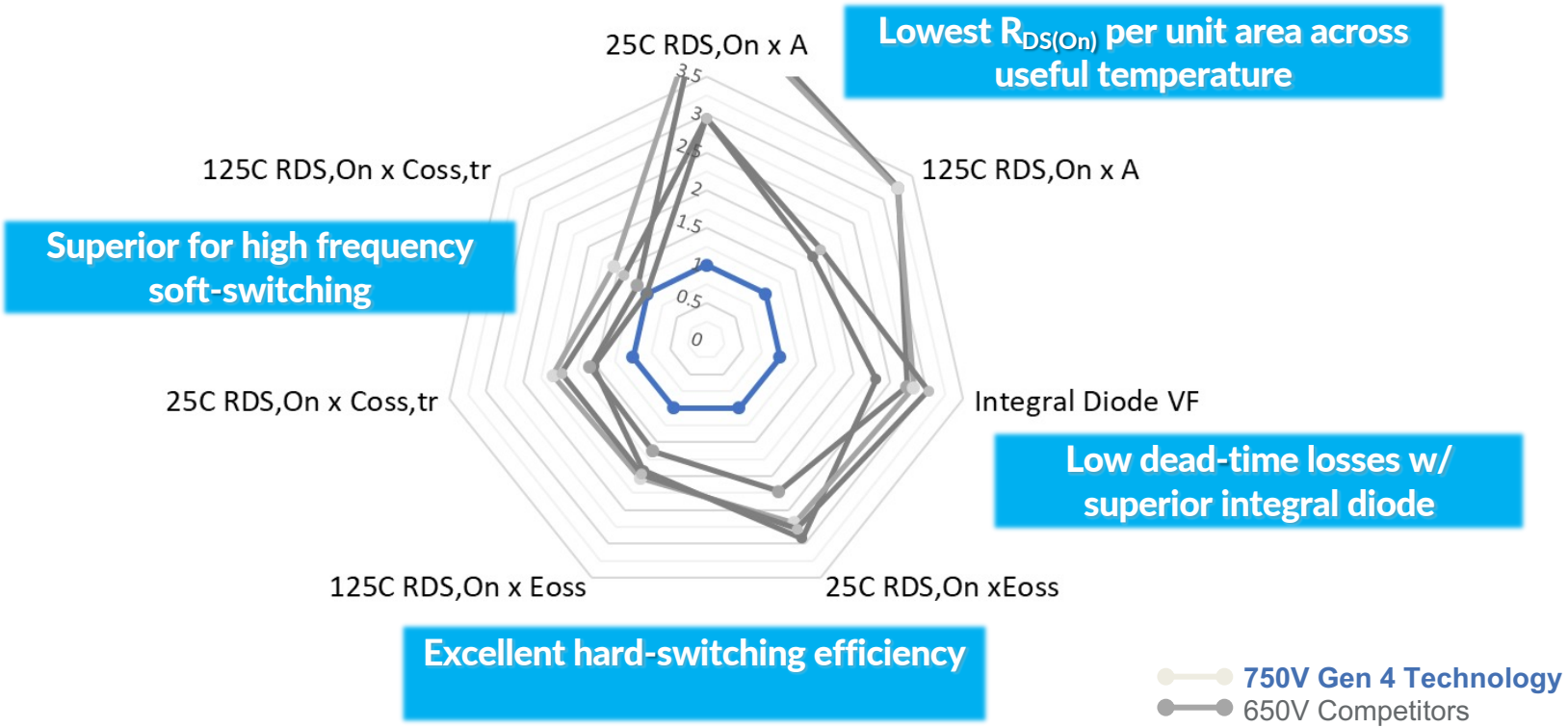
- **Lowest total** E_{oss} / Q_{oss} x $R_{DS(on)}$ FoM
- **Nearly 2X better** than competitors



Benefit

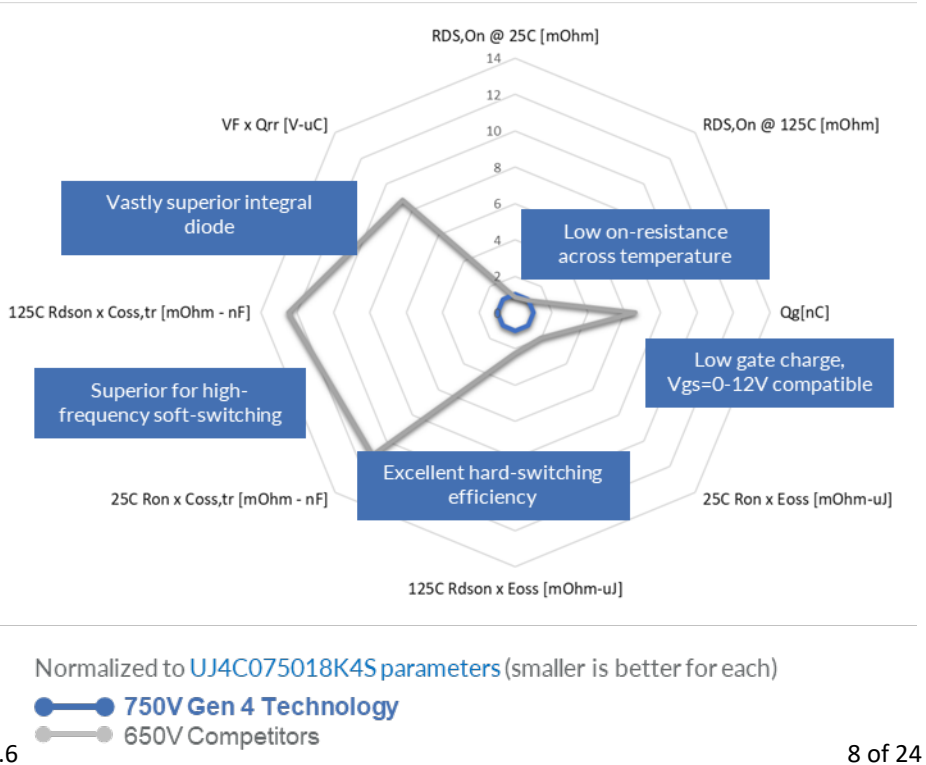
- Maintaining low $R_{DS(on)}$ x $C_{oss,tr}$ enables **higher power density** in soft-switched applications
- **5-10X** lower gate drive losses by Q_g x V_{Drive}
- Excellent body diode enables **reliable operation** out of resonance

Gen 4 SiC FETs - Industry's best Figures of Merit



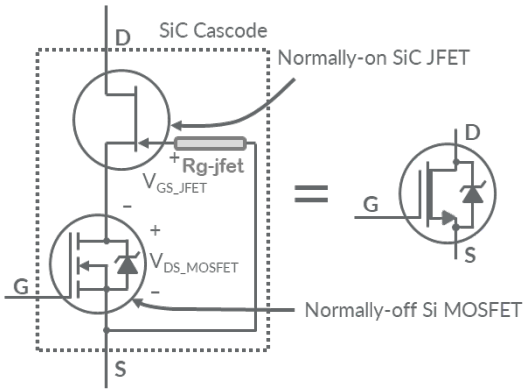
Gen 4 750V SiC FETs vs Si superjunction

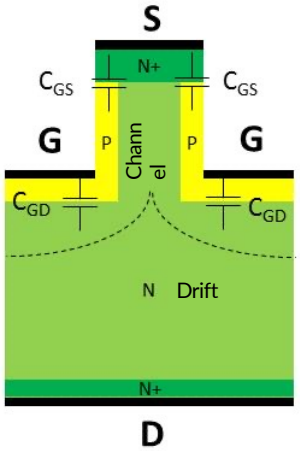
Specification	Fast Diode SJ	SJ Best-in-class	UJ4C075018K4S
Irated_Tc100 [A]	64	62	60
Voltage Rating [V]	600	650	750
RDS,On @ 25C [mOhm]	15.0	17	18
RDS,On @ 125C [mOhm]	29.0	33.5	31
Tj,max [C]	150.0	150	175
Rth,j-c(max) [C/W]	0.3	0.28	0.39
Qg[nC]	251	215	38
Qrr [nC]	1560	20000	102
VFSD@25C [V]	1.0	0.9	1.7
125C Rdson x Eoss [mOhm-uJ]	826.5	911.2	372.0
125C Rdson x Coss,tr [mOhm - nF]	108.2	111.2	8.7
VF x Qrr [V-uC]	1.6	18	0.18



SiC cascode FET: Low C_{rss}

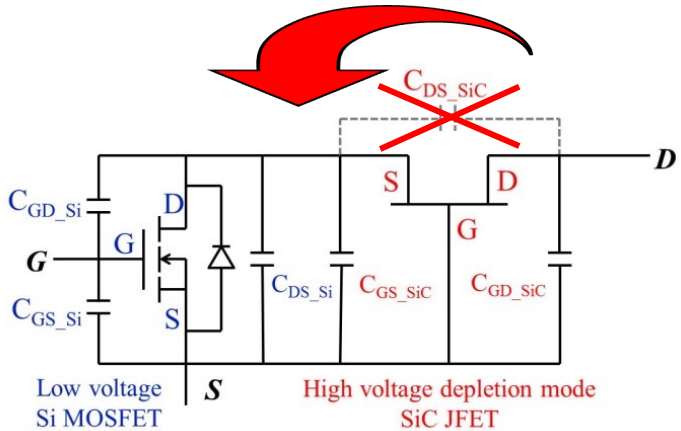
Good for fast switching, low losses, immune to dv/dt induced shoot through in bridge circuits….





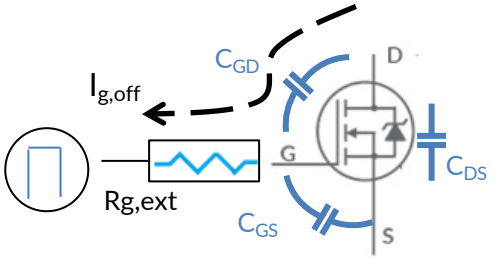
SiC Vertical JFET is "0" C_{DS} structure, formed with PN Junctions from G-S and G-D JFET: C_{GS} and C_{GD}

No C_{DS} JFET -> No C_{rss} of Cascode FET



SiC cascode FET: Low C_{rss}

But turn-off is not set by Rg_ext alone....



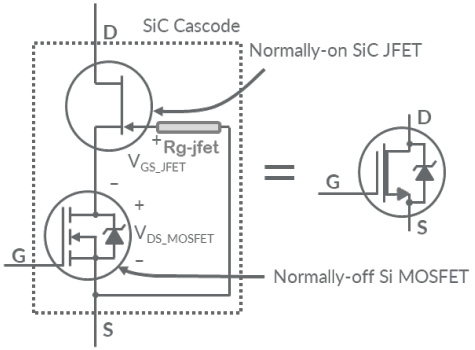
Turn-Off Voltage Transition of Conventional MOSFET

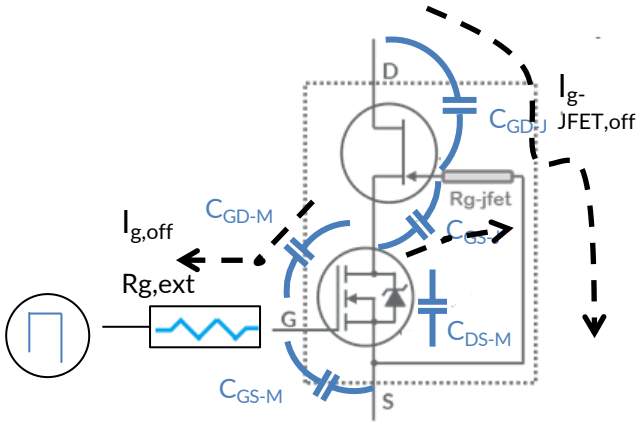
V_g in plateau region

$I_{g,off} = I_{C,GD}$ α $C_{GD}\, dV_D/dt$

$I_{g,off}$ varied easily via:

$[V_{g,plateau} - V_{g,off}] / R_{g,ext}$





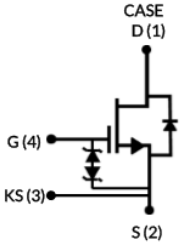
In Cascode, $R_{g,ext}$ alone does not limit the turn-off voltage transition dV/dt..... voltage transition is also dictated by (I_{g-JFET}) Rg-jfet once JFET Vgs is in its plateau region... this is built into JFET.

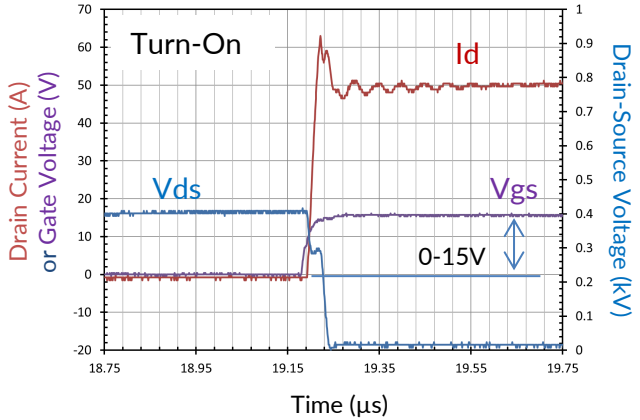
Small RsCs or Cs device snubbers are ***EFFECTIVE*** method to manage fast switching waveforms, minimize delay times and maintain low switching losses

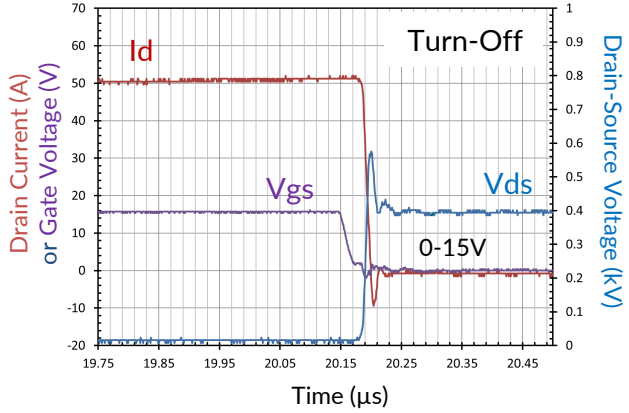
See "Minimizing EMI and Switching Loss for SiC FETs" at www.unitedsic.com

Gen 4 SiC FETs in kelvin-source packages

TO-247-4L







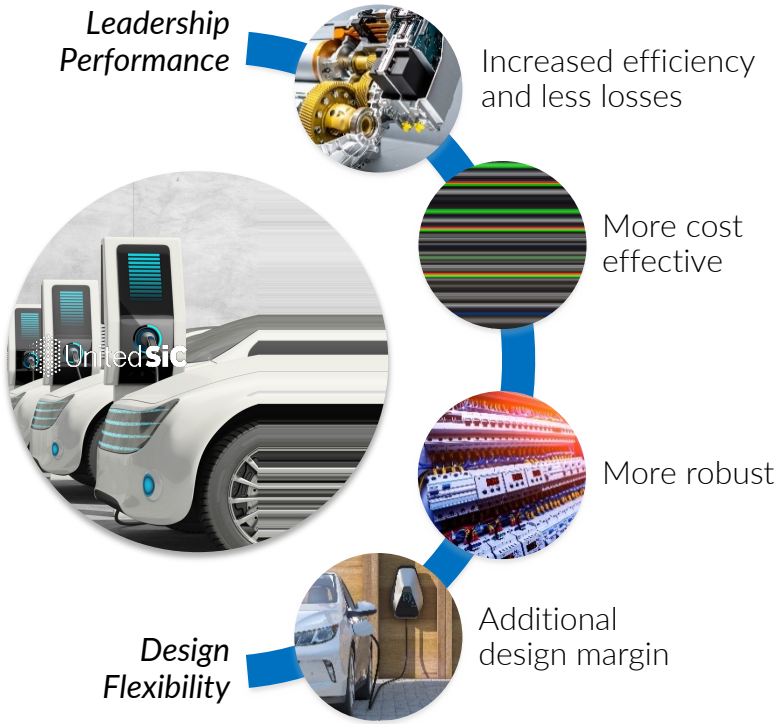
T=150°C, Rg_{On}/Rg_{Off}=1W, ***Rs=10ohm***, ***Cs=300pF***, Vgs=0V to 15V

- High performance Gen 4 UnitedSiC FETs offered in kelvin-source connected TO247-4L and D2PAK-7L (coming soon)
- Lower switching losses
- Cleaner gate waveforms with kelvin-source connected packages

Spec	UJ4C075018K4S	UJ4C075018K3S
Qrr	109nC	109nC
Eon	467uJ	744uJ
Eoff	58uJ	229uJ
Etotal	525uJ	973uJ

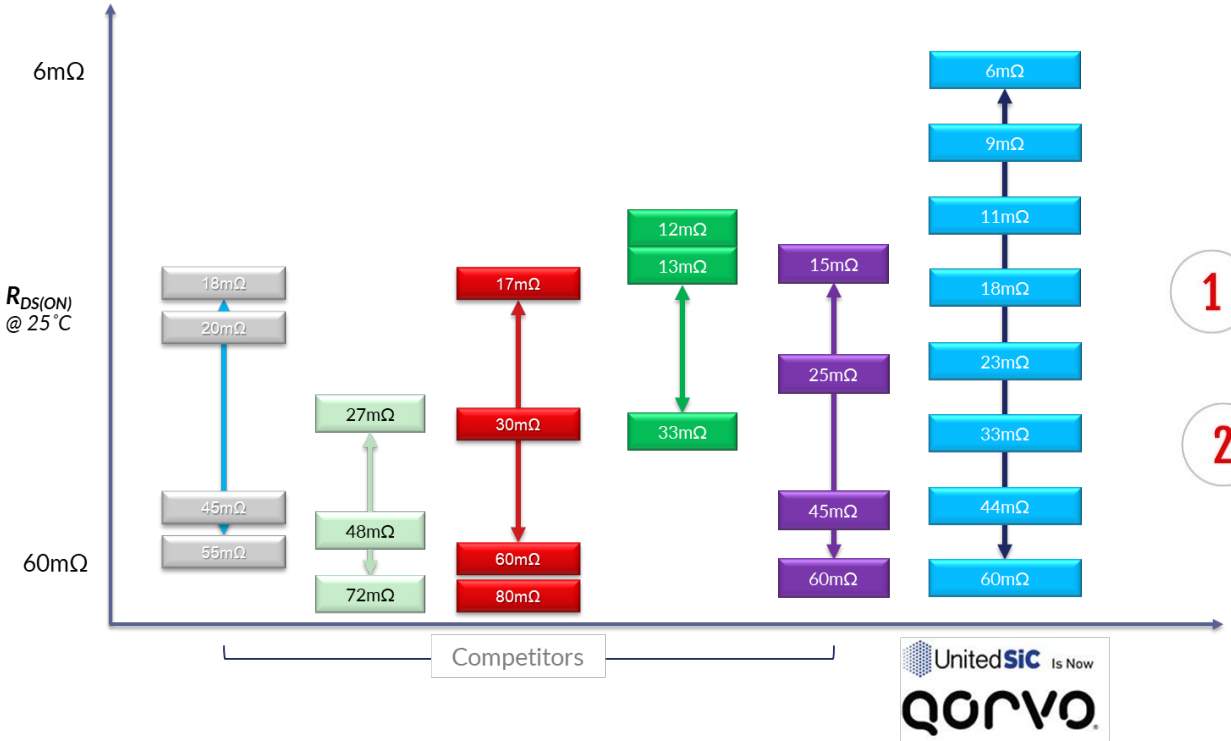
E_{snub} = 10-12uJ at 50A/400V switching with Rg=1ohm

SiC: More applications, more design considerations



UJ4C/SC
750V SiC FET Series

SiC FET options enable more design flexibility



UJ4C/SC
SiC FET Series

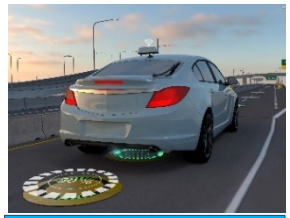
1. Determine your desired power level
2. Select optimal device
   - Efficiency
   - Cost
   - Thermal

Gen 4 SiC FETs - Design Flexibility in Automotive

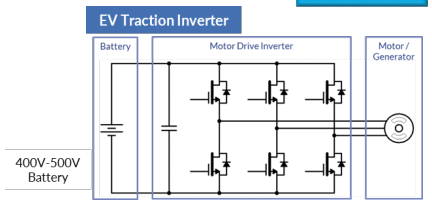
KEY FEATURES

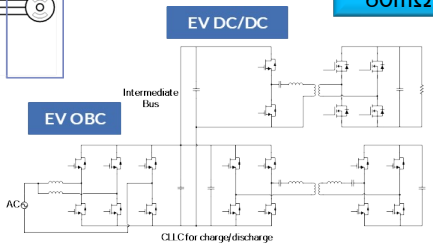
- Lowest $R_{DS(on)}$ die
- Low $R_{DS(on)}$ x E_{oss}
- Low $R_{DS(on)}$ x C_{oss}
- Simple gate drive (0-12V)
- Low V_f diode
- 5µs short circuit current (6mΩ)

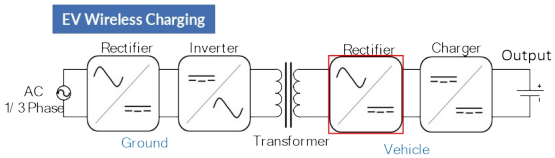
Automotive



400/500V Bus Traction Inverter	On-Board Chargers DC/DC Converters	400/500V Bus Wireless Charger
6mΩ	11mΩ	6mΩ
9mΩ	18mΩ	9mΩ
11mΩ	23mΩ	11mΩ
	33mΩ	18mΩ
	44mΩ	
	60mΩ	







Design Flexibility in IT infrastructure

IT Infrastructure

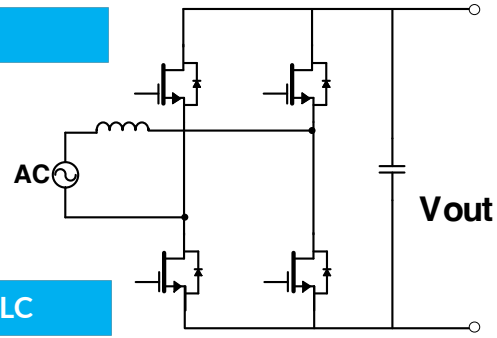
Power Factor Correction

DC/DC Converters

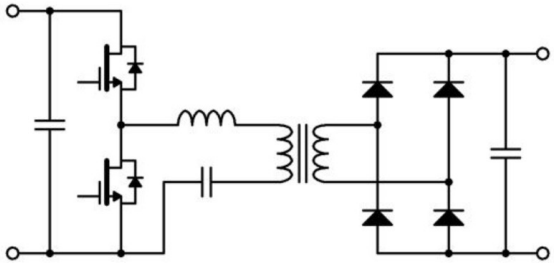
KEY FEATURES

- Low $R_{DS(on)}$ x E_{oss}
- Low $R_{DS(on)}$ x C_{oss}
- Simple gate drive (0-12V)
- Low V_f diode

TPPFC



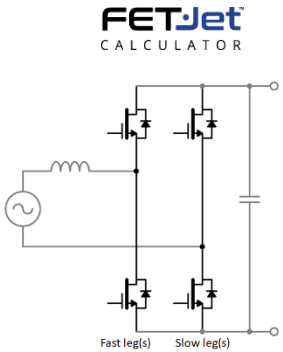
DC/DC LLC

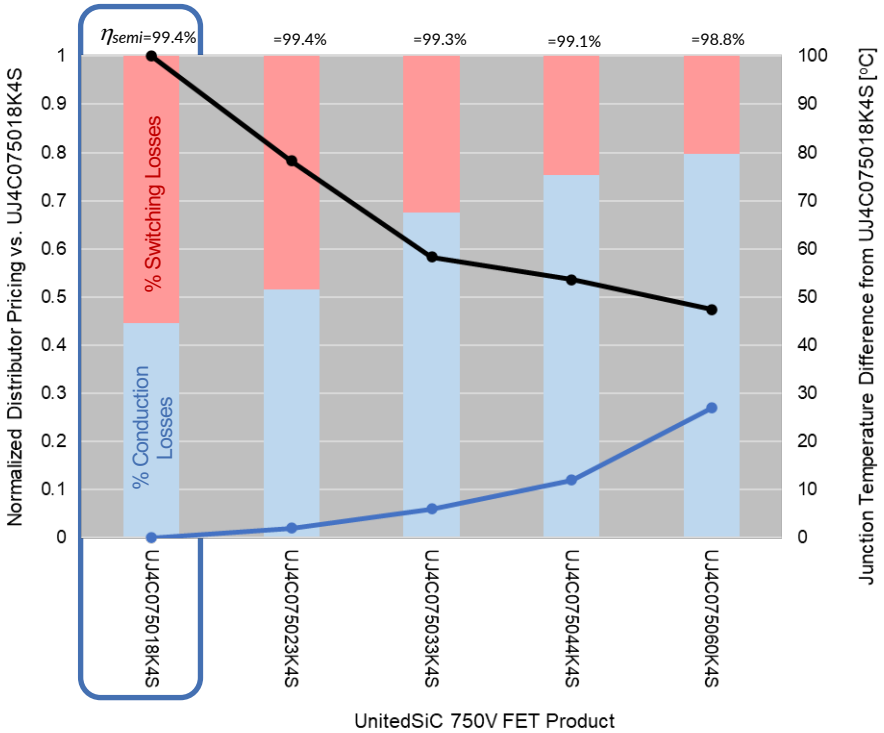


18mΩ
23mΩ
33mΩ
44mΩ
60mΩ

SiC FET options enable more design flexibility

TPPFC Fast Leg Switch Design – 3.6kW





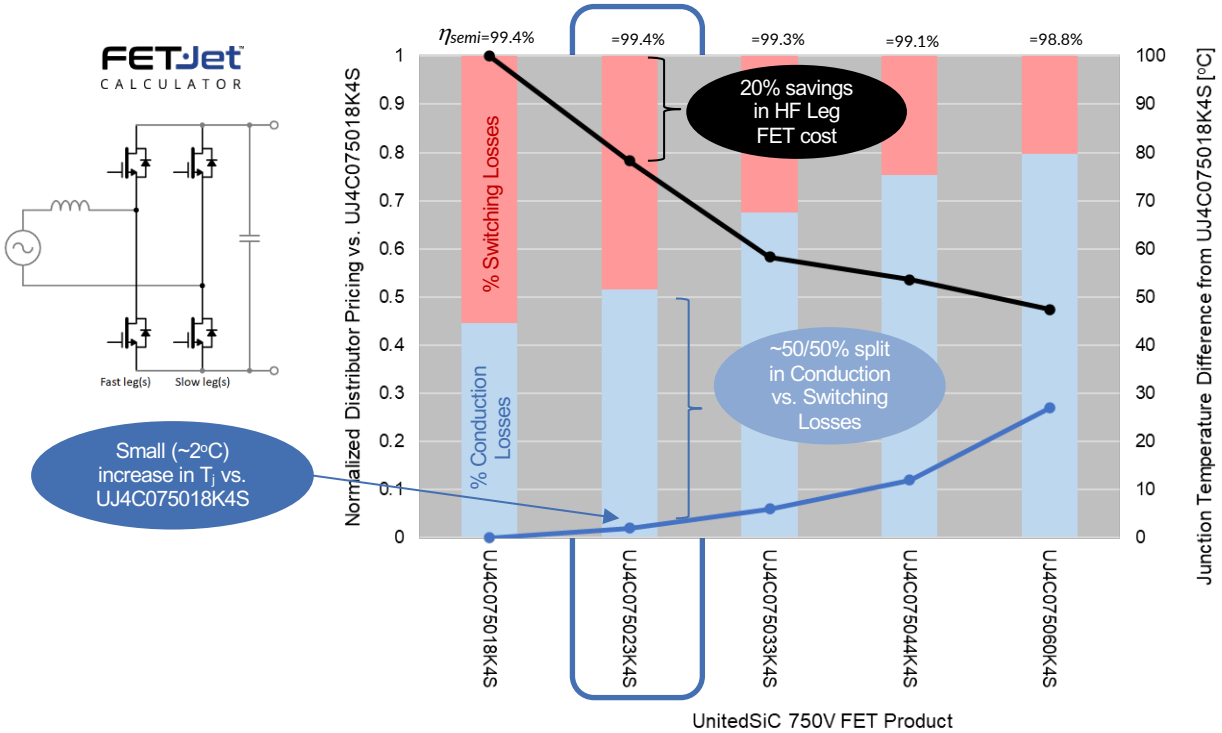
UJ4C075018K4S:

- Highest performance at full and 50%-load, semiconductor efficiency = 99.4%
- Low Rthjc + Low Losses yield a low temperature rise, T_j=96°C @ full load

*230Vin, 400VDC, 65kHz, 20% inductor ripple current, HS=85°C ,CCM

SiC FET options enable more design flexibility

TPPFC Fast Leg Switch Design – 3.6kW



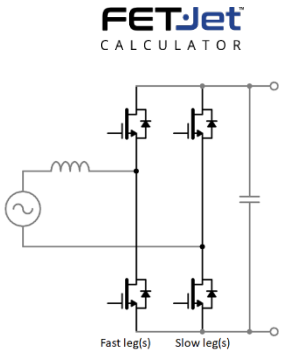
UJ4C075023K4S:

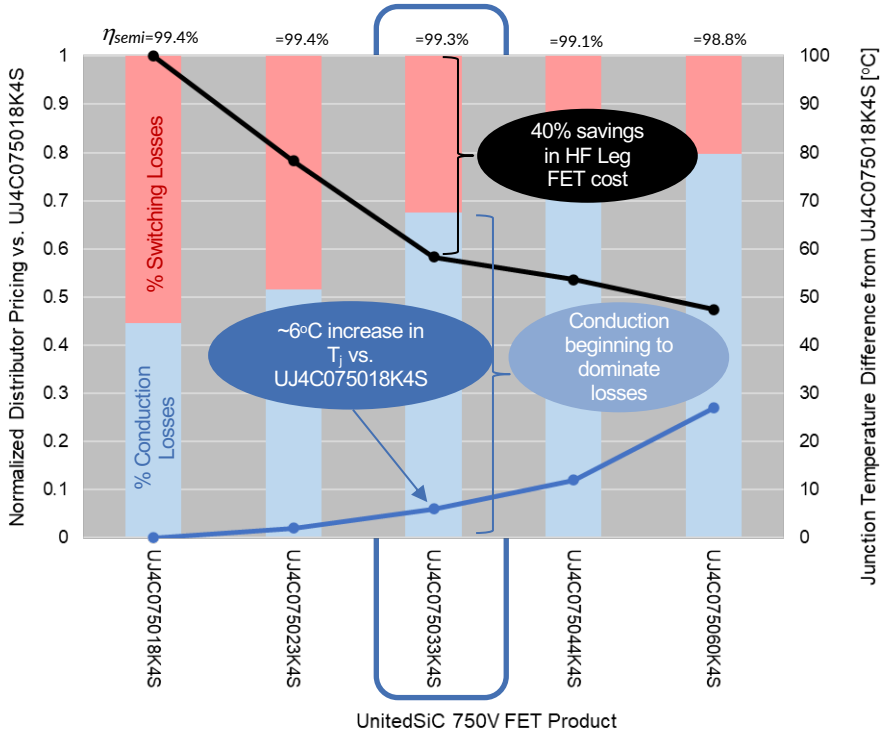
- Excellent Cost/Performance tradeoff
- Low R_{thjc} + Low Losses yield a low temperature rise, T_j=98°C @ full load

*230Vin, 400VDC, 65kHz, 20% inductor ripple current, HS=85°C ,CCM

SiC FET options enable more design flexibility

TPPFC Fast Leg Switch Design – 3.6kW





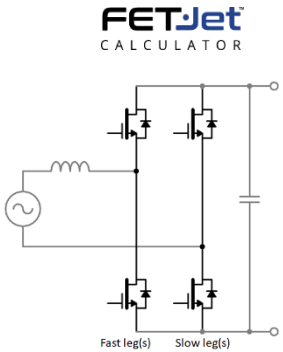
UJ4C075033K4S:

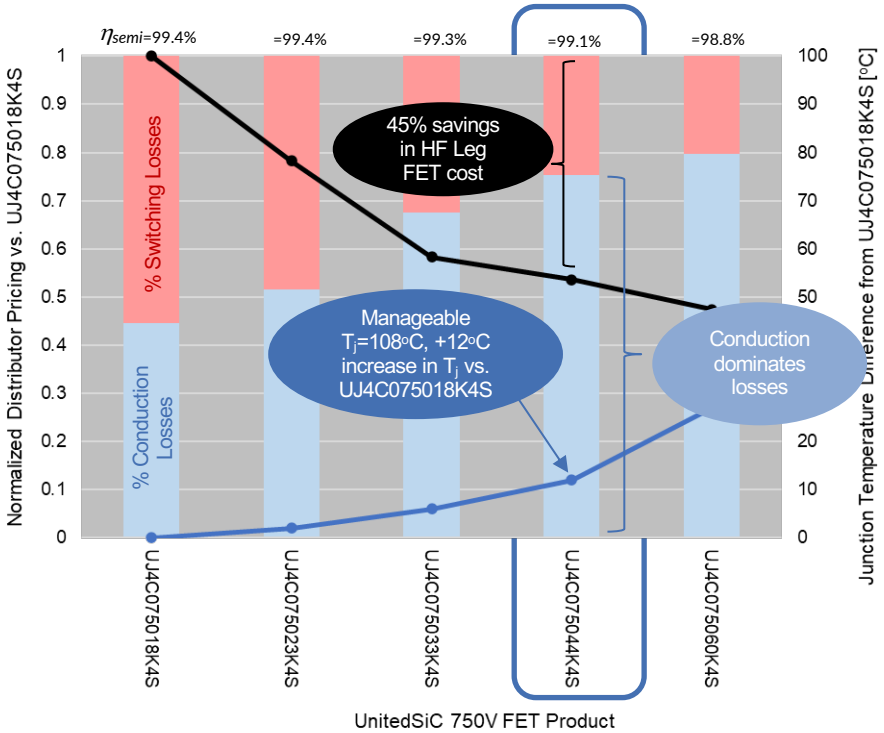
- Excellent Cost/Performance tradeoff
- Good performance, semiconductor efficiency 99.3%
- Conduction dominates losses at full load, 67%

*230Vin, 400VDC, 65kHz, 20% inductor ripple current, HS=85°C ,CCM

SiC FET options enable more design flexibility

TPPFC Fast Leg Switch Design – 3.6kW





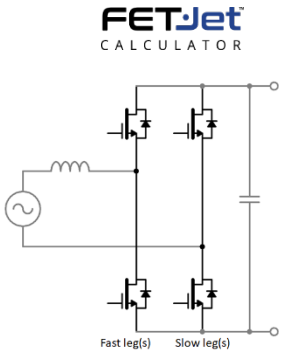
UJ4C075044K4S:

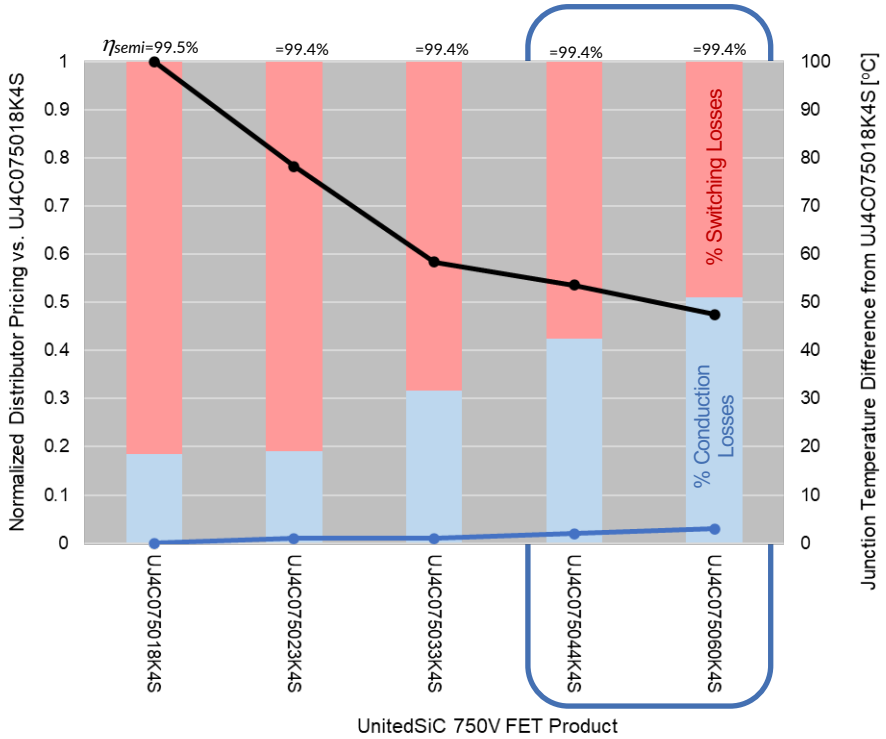
- Good choice where partial-load efficiency is important, 99.1% @ 3.6kW, 99.4% @ 1.5kW
- Conduction dominates losses at full load, 75%
- +12°C Tj compared to UJ4C075018K4S

*230Vin, 400VDC, 65kHz, 20% inductor ripple current, HS=85°C ,CCM

SiC FET options enable more design flexibility

TPPFC Fast Leg Switch Design – 1.5kW





UJ4C075044K4S & UJ4C075060K4S

Offer Excellent Options at 1.5kW:

- Comparable semiconductor efficiency (99.4%) as the lower on-resistance parts, despite ~47-53% of FET cost
- Balanced conduction & switching losses with low T_j rise (93°C, within 3°C of UJ4C075018K4S)

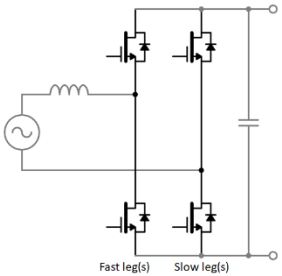
Full portfolio offers designers new choices allowing better system optimization

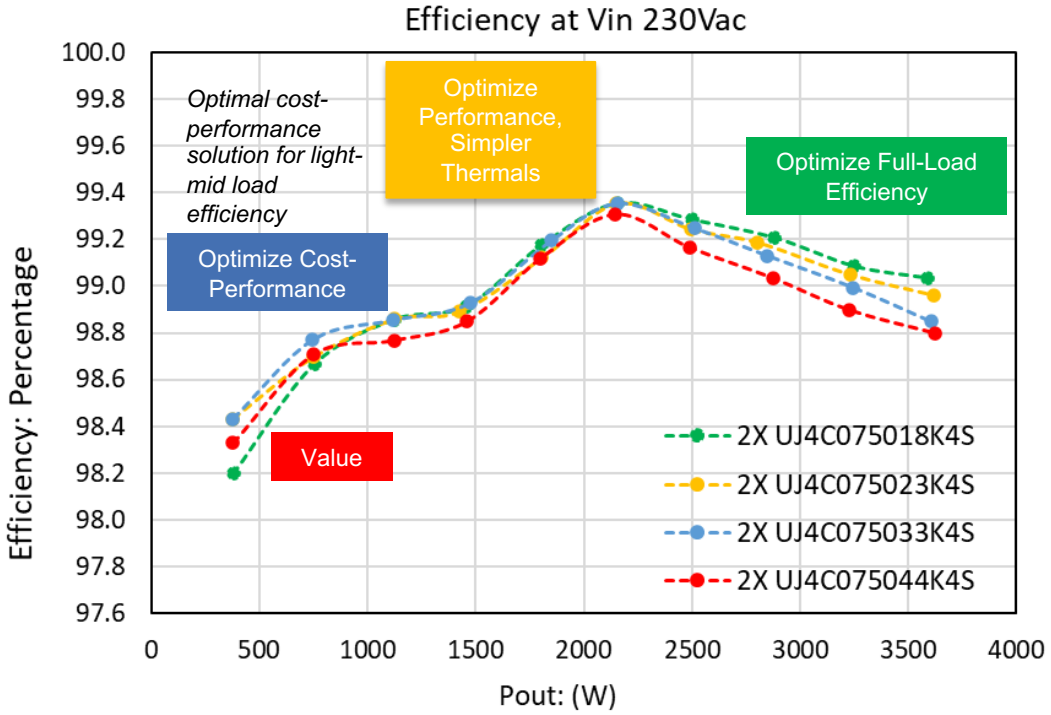
*230Vin, 400VDC, 65kHz, 20% inductor ripple current, HS=85°C ,CCM

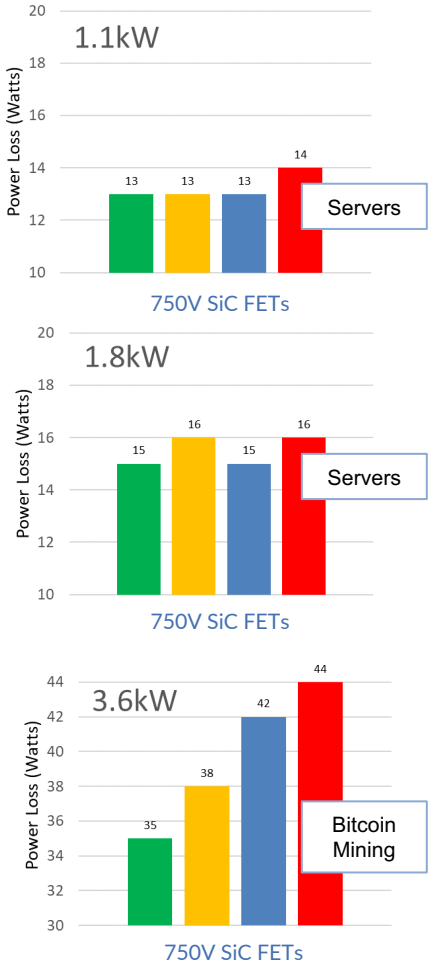
Flexibility in TPPFC

IT Infrastructure

- Power Factor Correction
- DC/DC Converters



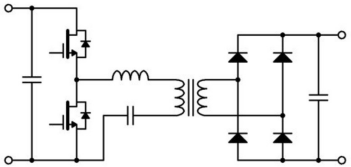




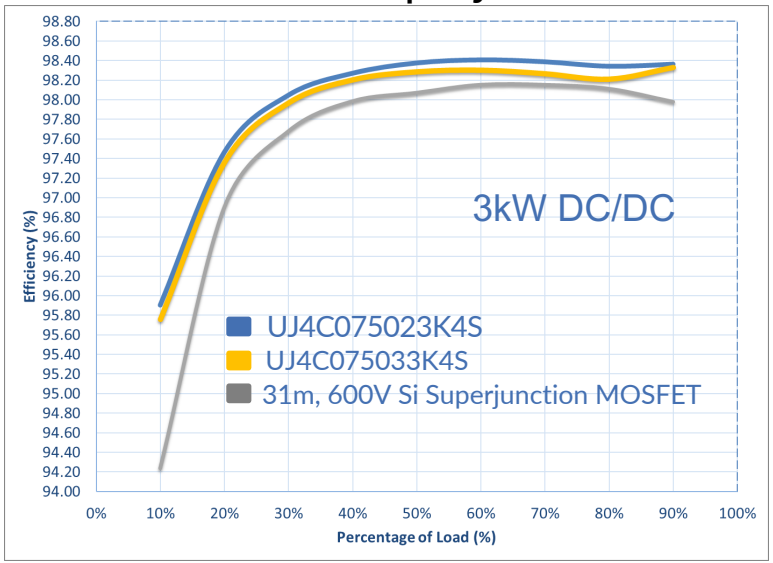
Flexibility in LLC

IT Infrastructure

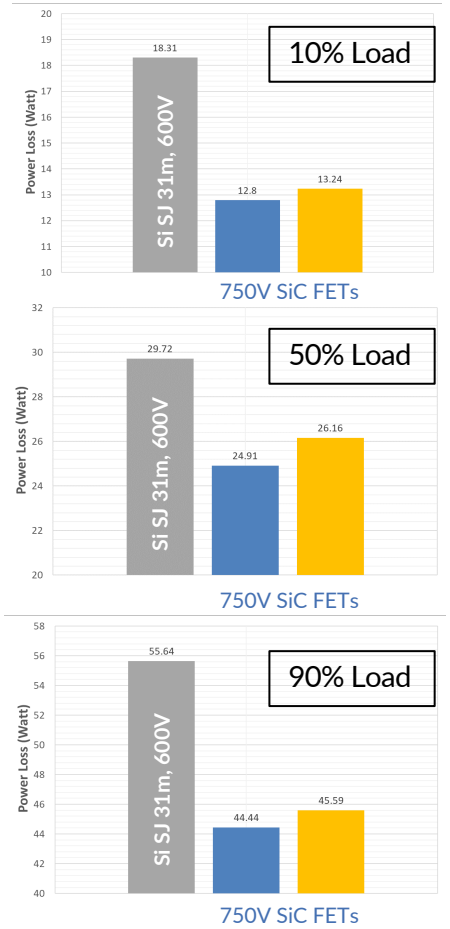
- Power Factor Correction
- DC/DC Converters



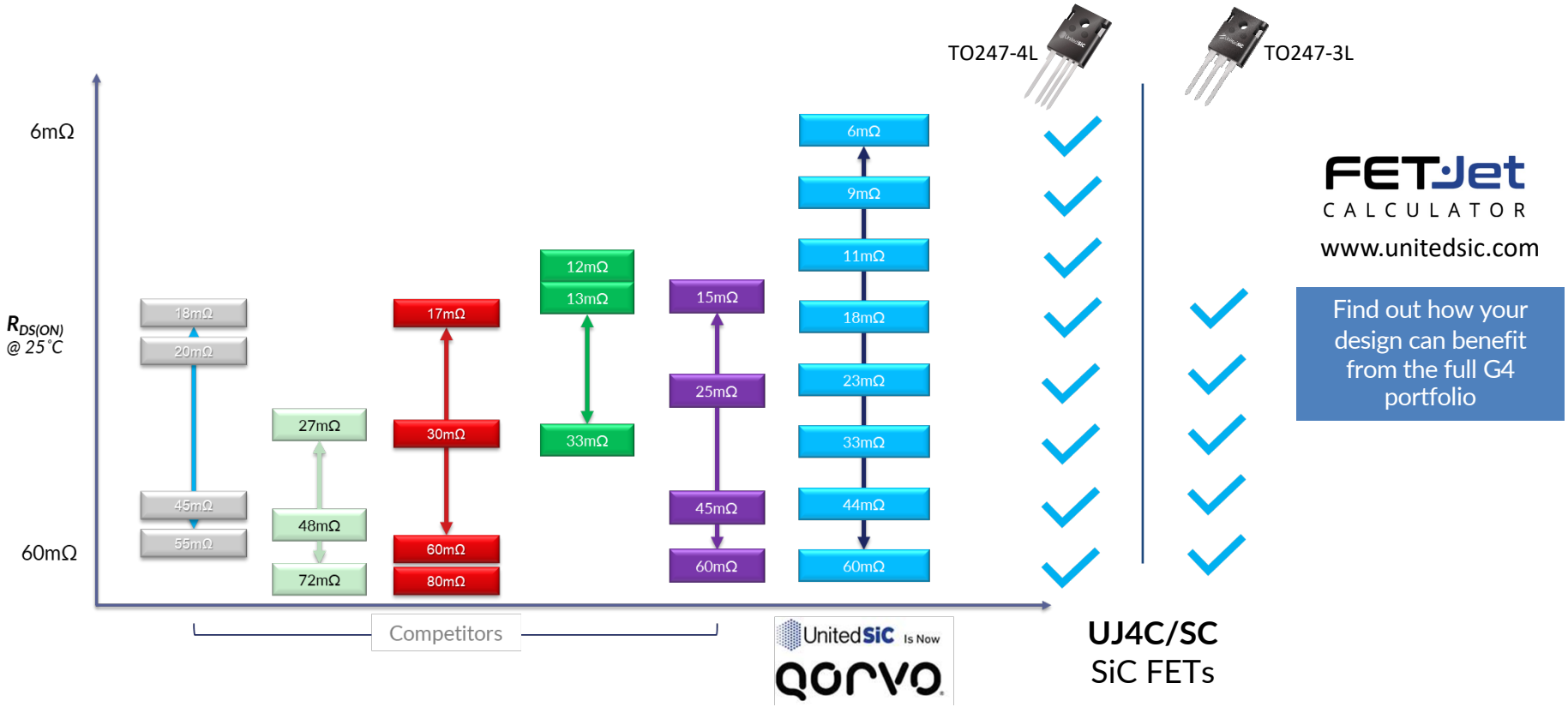
SiC FET vs. Si Superjunction



Drop-in replacement results



SiC FET options enable more design flexibility



Summary

- SiC Cascode FETs offer the lowest RDSON switches in 650V+ class
- Gen 4 750V SiC FETs are excellent options for hard, soft-switched applications
- Broad portfolio from 6mohm – 60mohm allow designers to select best system cost-performance in front end rectifier and dc-dc converters