



# Performance Parameters of SiC MOSFETs for Automotive Inverters

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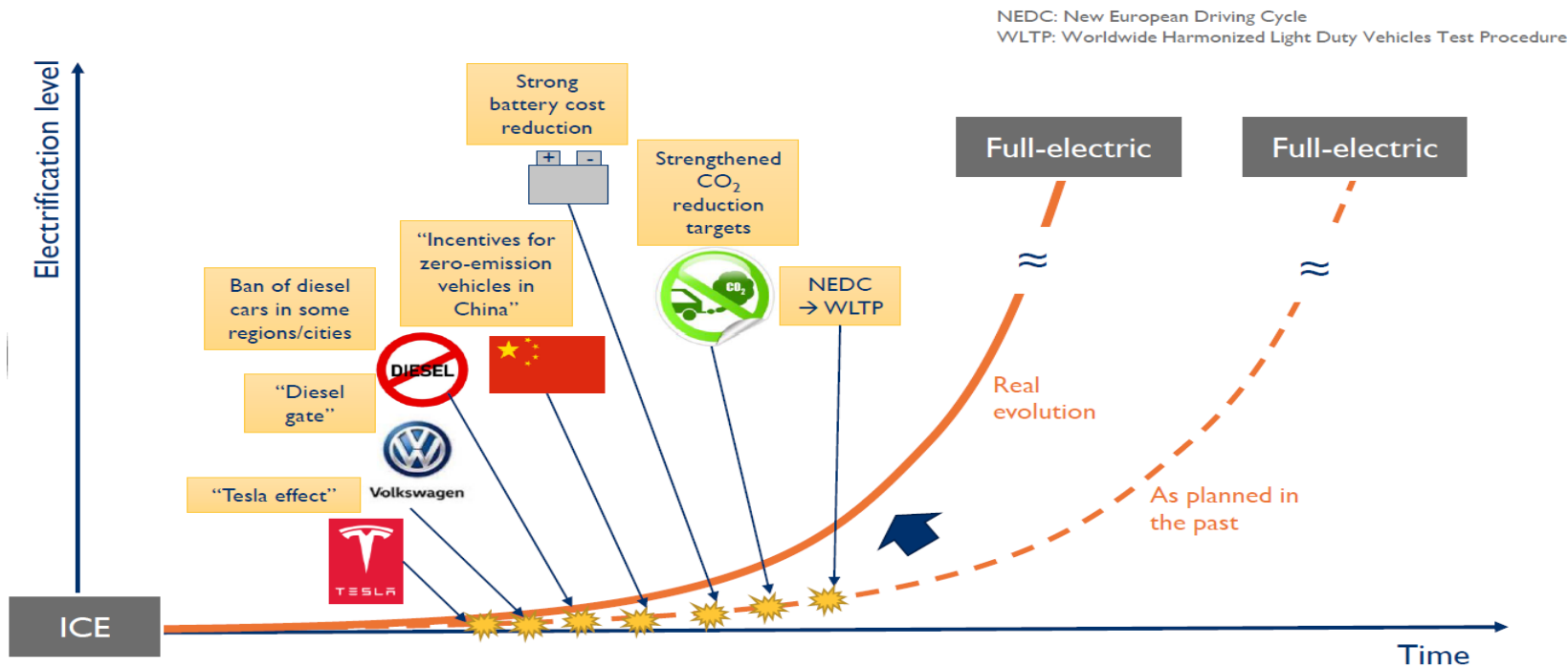
GeneSiC Semiconductor, Inc.

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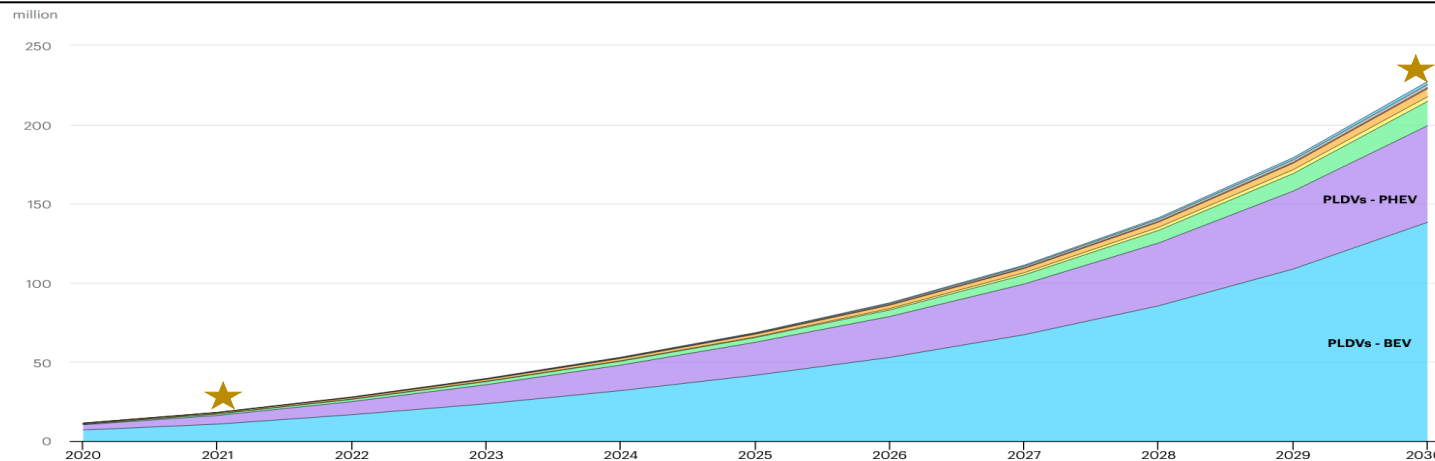
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# Vehicle Electrification Trends



- ❑ About 200 million electric vehicles expected on road by 2030
- ❑ Market share of EVs expected to exceed 30% by 2030
- ❑ ~9 % of global new car sales in 2021 were electric vehicles



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# Silicon Carbide (SiC) – Key Applications in Electric Vehicles



**Traction Inverters**

**On-Board Charger (OBC)**

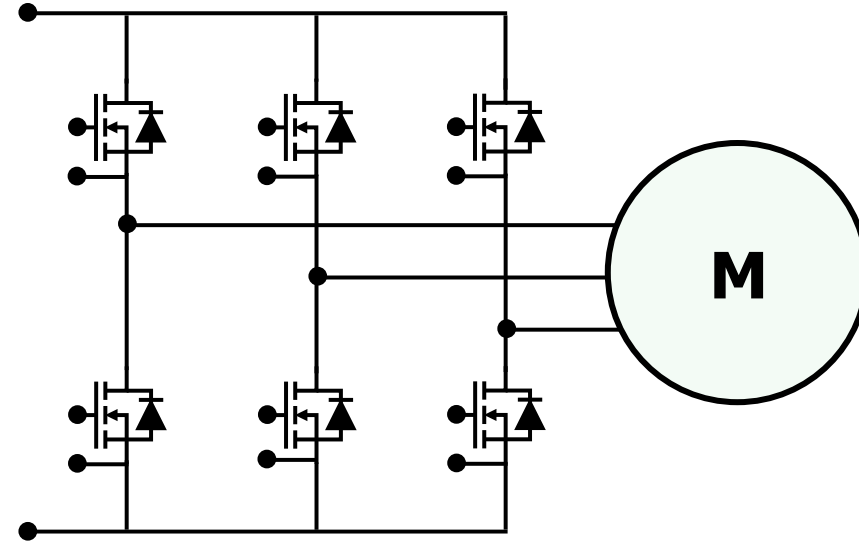
**DC-DC (HV→48V ; HV → 12V)**

**Extreme Fast Charger (XFC)**

- ✓ SiC technology is revolutionizing vehicle electrification  
Higher Voltage → Greater Power → Better Efficiency → Smaller Size → Lighter Weight
- ✓ SiC is proven significantly better than conventional silicon power device based solutions
- ✓ No longer a question of Si IGBT v/s SiC MOSFET in traction inverters !  
All leading OEMs adopting SiC



# SiC MOSFET in EV/HEV Traction Inverters



**3-Phase Inverter Based on SiC MOSFETs**

- ✓ Nominal power ranging from 10 kW (ICE assistance) to 200 kW (pure EV)  
 $V_{BUS}$  : 400 V – 450 V → **750V SiC MOSFET**  
 $V_{BUS}$  : 700 V – 800 V → **1200V SiC MOSFET**
- ✓ Bi-directional operation (feeding electric motor + regenerative braking)
- ✓ 80% or more reduction in total inverter losses when compared with silicon-based (IGBT) solutions (same voltage, same switching frequency, same cooling)



# SiC MOSFET Technologies – As it Exists Today

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- ❑ **Do all SiC MOSFET technologies existing in the market offer similar performance, robustness and quality ?**

SHORT ANSWER = **NO**

There are significant differences at the power device technology level and power electronics designers must perform thorough evaluation/assessment of each SiC MOSFET technology to maximize their system performance and robustness.

- ❑ **Which SiC MOSFET Parameters Differ by Each Vendor / Technology and how do they affect the performance ?**

NEXT SLIDE .....



# 750V SiC MOSFET Technology Comparison

## Superior power density and cooler operation

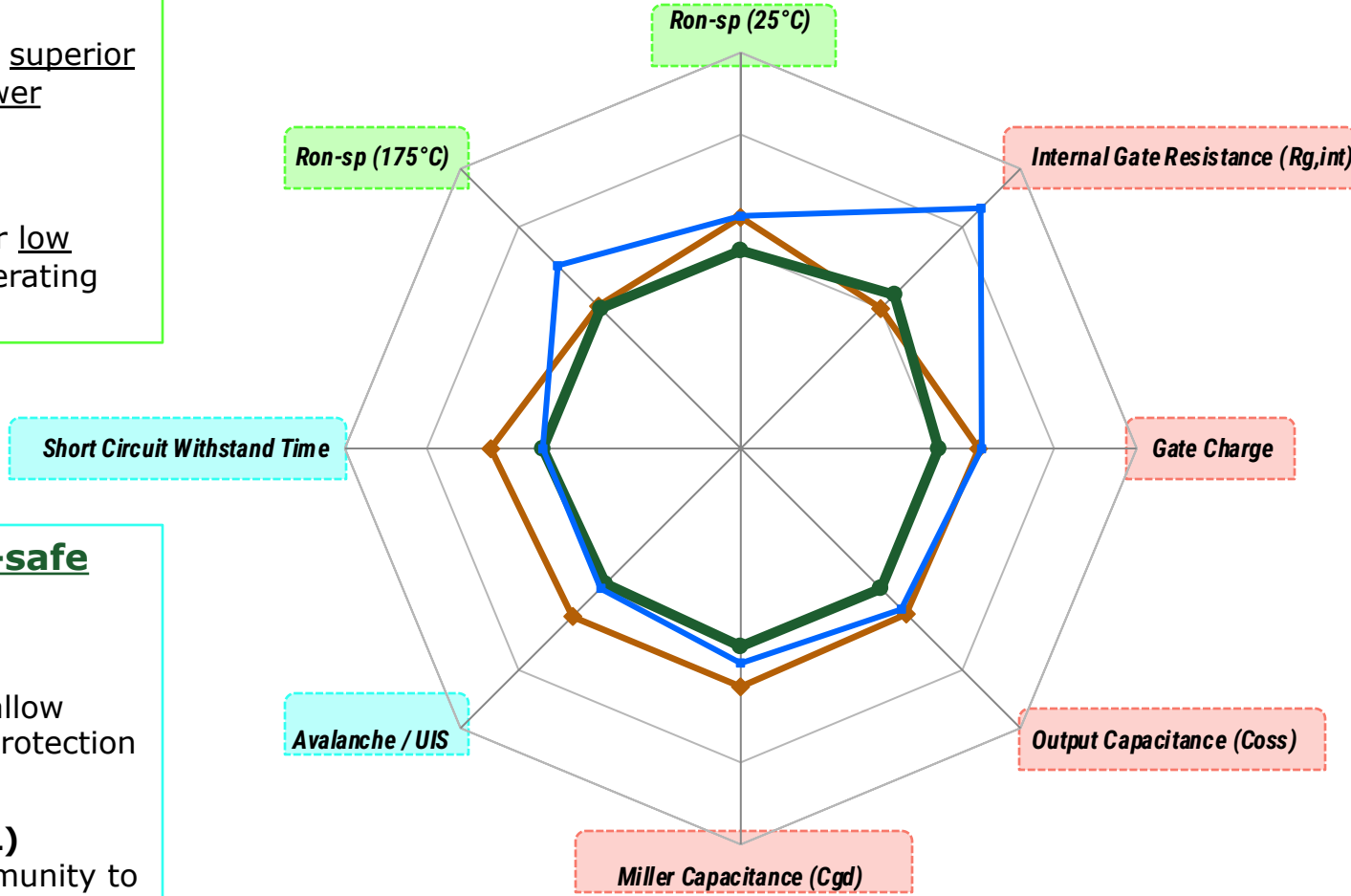
**Industry-leading CPI** for superior performance and more power density

**Softest temperature dependence of  $R_{DS(on)}$**  for low conduction losses at all operating temperature

## More robust and fail-safe designs

**Improved short circuit withstand capability** to allow designers develop robust protection circuits

**Superior avalanche (UIL) ruggedness** for better immunity to over-voltage transients. All production parts are **100% UIL tested**



## Faster and cleaner switching (lower switching losses)

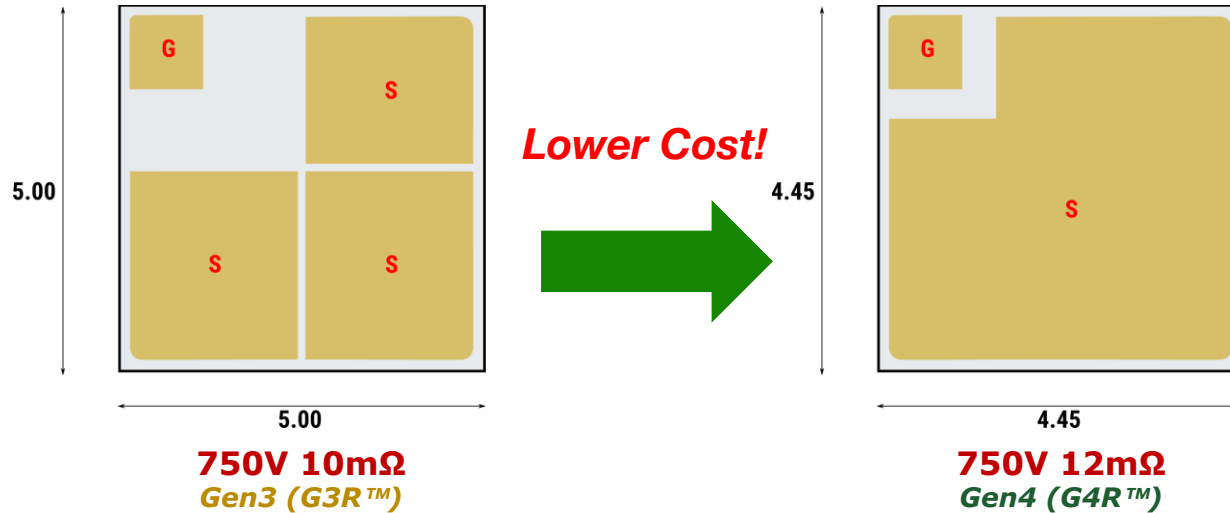
**Low  $R_{g,int}$  and low gate charge ( $Q_g$ )** to enable faster switching (lower losses)

**Low device capacitances ( $C_{oss}$  and  $C_{rss}$ )** to reduce ringing (lesser spikes) and lower switching losses



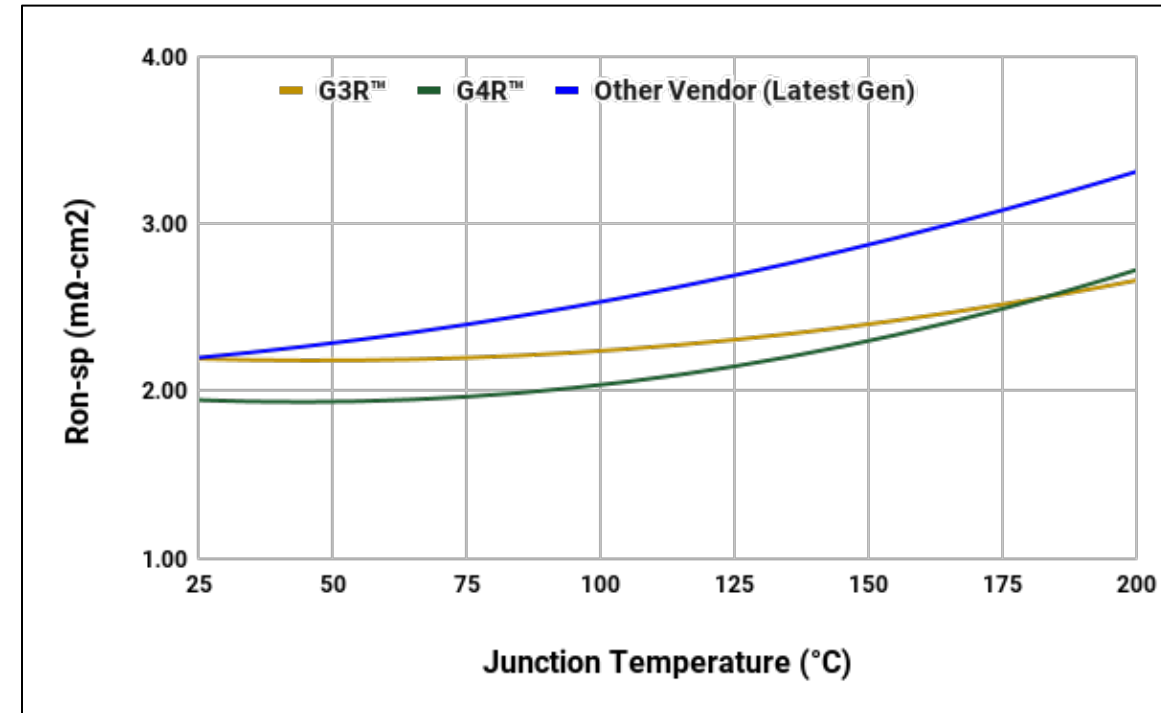


# Specific On-State Resistance ( $R_{ON-SP}$ ) v/s Temperature



	G3R™	G4R™	Other Vendor
$V_{DSS}$	750 V	750 V	750 V
Chip Size	5.00 mm x 5.00 mm	4.45 mm x 4.45 mm	5.00 mm x 5.00 mm
$V_{GS(op)}$	+15 V / -5 V	+15 V / -5 V	+15 V / -4 V
$R_{DS(ON)} @ 25^{\circ}C$	10 mΩ	12 mΩ	10.5 mΩ
$R_{DS(ON)} @ 175^{\circ}C$	11.5 mΩ	15 mΩ	14.8 mΩ

## Specific On-State Resistance, $R_{ON-SP}$ ( $m\Omega\text{-cm}^2$ )



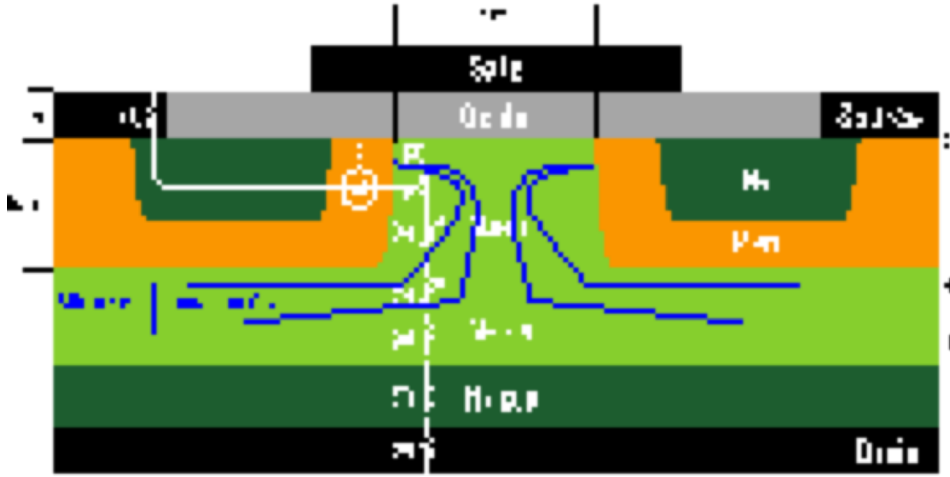
## Requirements for Better Efficiency in all Drive Cycles (all Load Conditions) :

- ✓ Low  $R_{on-sp}$  ( $m\Omega\text{-cm}^2$ ) at all temperatures ( $T_J$ )
- ✓ Cleaner switching performance and lower switching losses

i.e. Low Gate Charge ( $Q_G$ ), Low Internal Gate Resistance, Low  $C_{RSS}$ , Low  $Q_{OSS}$ , Low  $Q_{RR}$



# Physics-Based SPICE Model for Reliable Circuit Simulations

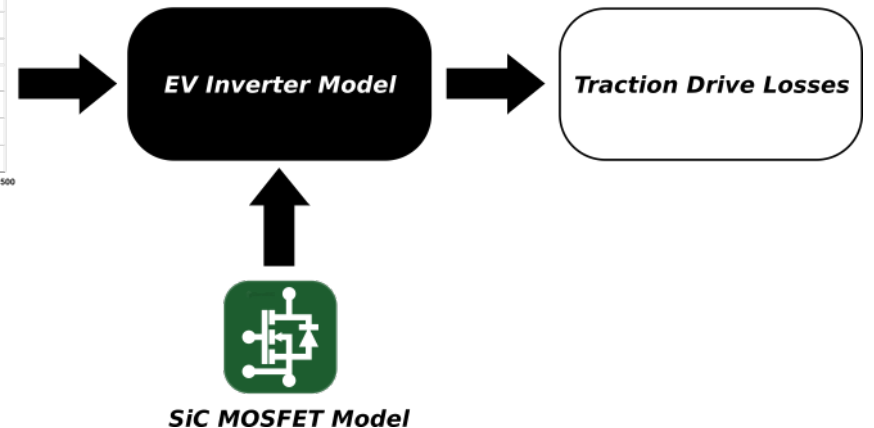
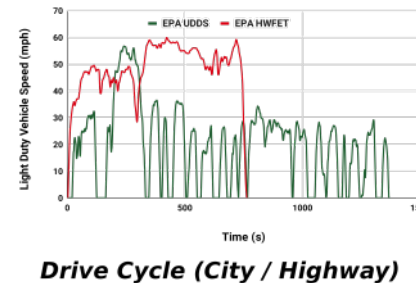


- ✓ Sophisticated and accurate physical model
- ✓ Scalable – device design and process parameters included
- ✓ Straight forward model parameter definition process
- ✓ Easy measurement-based calibration
- ✓ Covers the wide operating temperature range of SiC MOSFET
- ✓ Accurate modeling of gate-bias and drain-bias dependencies
- ✓ Compatible with commercially available SPICE software suites
- ✓ Low computational effort and high efficiency

## On-Resistance Components

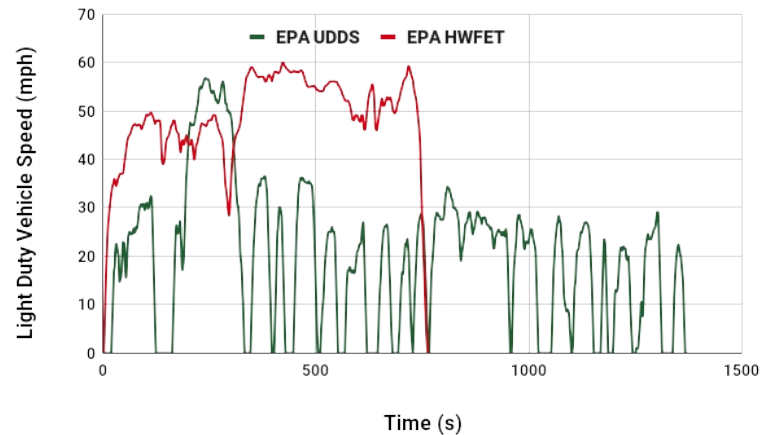
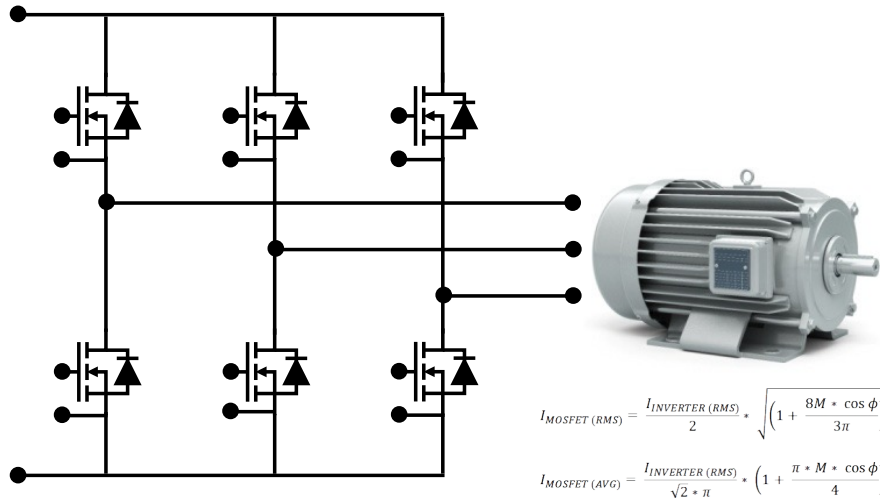
(1)	$R_{\text{source}}$	Source metal resistance
(2)	$R_{\text{ch}}$	Channel resistance
(3)	$R_{\text{acc}}$	Accumulation region resistance
(4)	$R_{\text{JFET}}$	JFET region resistance
(5)	$R_{\text{drift-var}}$	Bias-dependent drift layer resistance
(6)	$R_{\text{drift-con}}$	Drift layer resistance
(7)	$R_{\text{sub}}$	Substrate resistance
(8)	$R_{\text{drain}}$	Drain metal resistance

**Splitting of  $R_{\text{DS(ON)}}$  components is necessary to realize accurate temperature, gate-bias and/or drain-bias dependencies**





# Reducing Power Device Losses in Traction Inverters

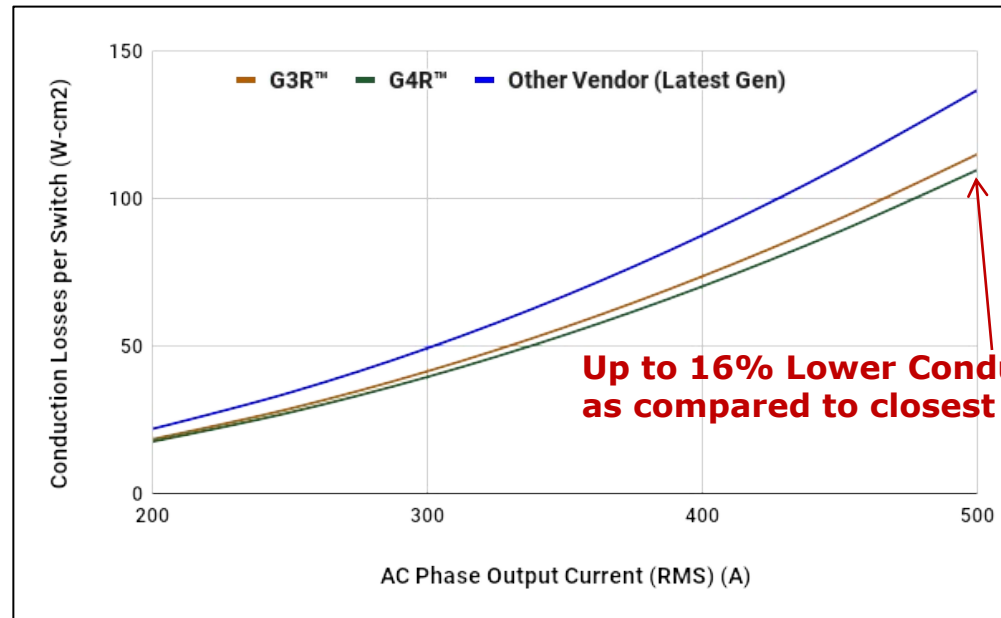


3-Phase Traction Inverter (Synchronous Rectification)  
SVPWM ( $m = 0.8$  ;  $\cos \phi = 0.8$ )

DC-Link Voltage = Up to 475V DC

Switching Frequency = 10 kHz

**Conduction Losses per Switch (W-cm<sup>2</sup>)**  
(Normalized to chip area in cm<sup>2</sup>) ( $T_j = 145^\circ\text{C}$ )

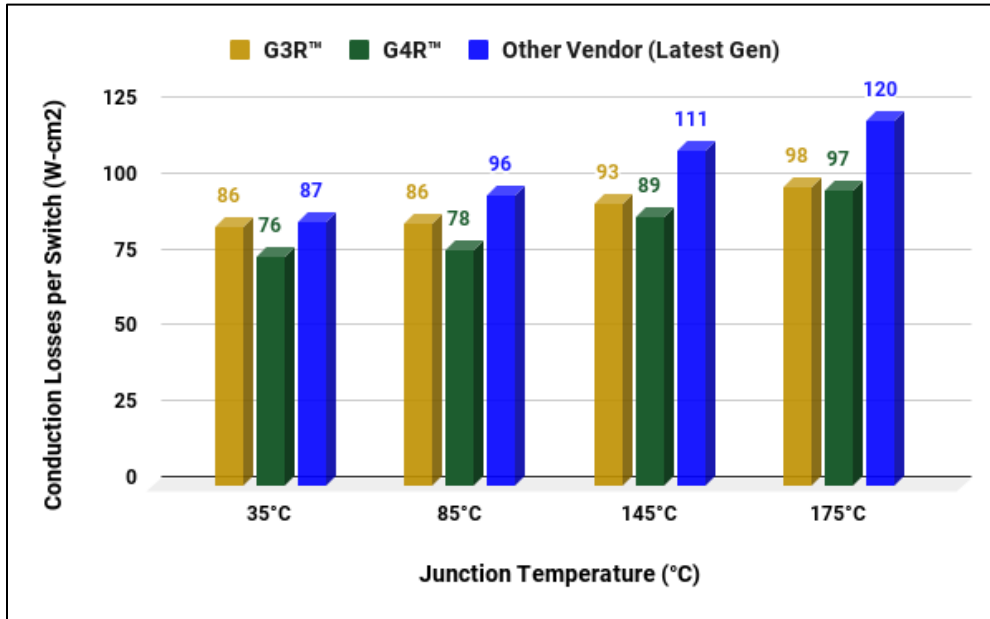


- ✓ Lowest possible conduction losses can be achieved by SiC MOSFETs with lowest  $R_{on-sp}$  (mΩ-cm<sup>2</sup>) and **softer temperature dependence of  $R_{DS(on)}$  (Better Temperature Coefficient)** for all drive cycles – *Urban Dynamometer Driving Schedule (UDDS)* ; *Highway Fuel Economy Test (HWFET)*



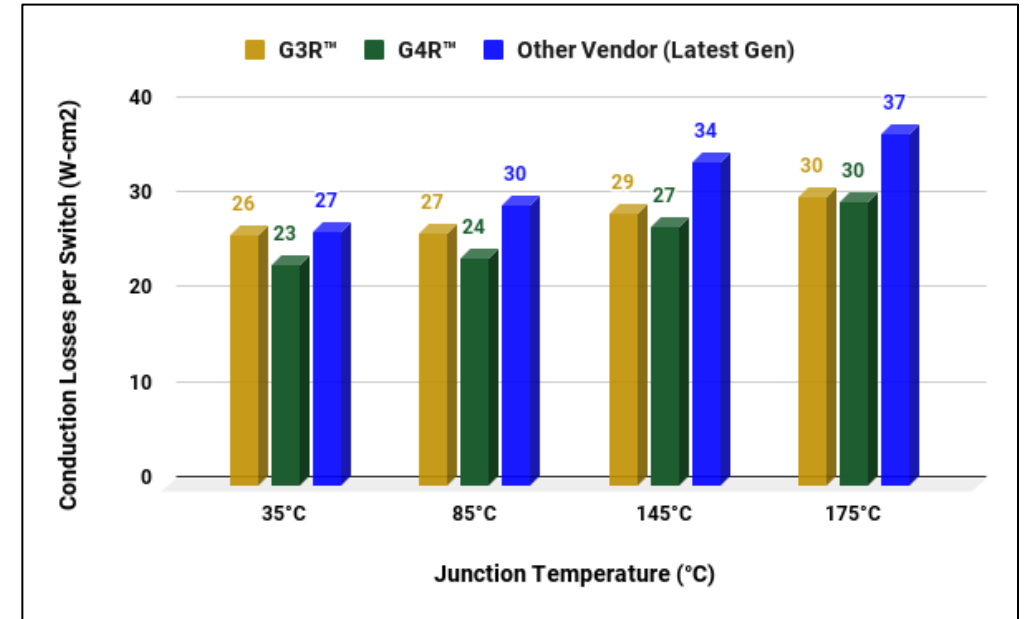
# Superior Drive Cycle Efficiency with Better SiC MOSFET Technology

## Conduction Losses per Switch (W-cm<sup>2</sup>)



**$I_{RMS} = 450 \text{ A}$**

*(AC Phase Output Current; 3-Ph Inverter)*



**$I_{RMS} = 250 \text{ A}$**

*(AC Phase Output Current; 3-Ph Inverter)*

### ✓ Light-Load Condition ( $I_{RMS} = 250\text{A}$ )

- ~18% reduction in conduction losses possible when temperature ( $T_J$ ) is in the 85°C – 145°C range.
- ~20% reduction when operating temperature is in the 145°C – 175°C range

### ✓ Heavy-Load Condition ( $I_{RMS} = 450\text{A}$ )

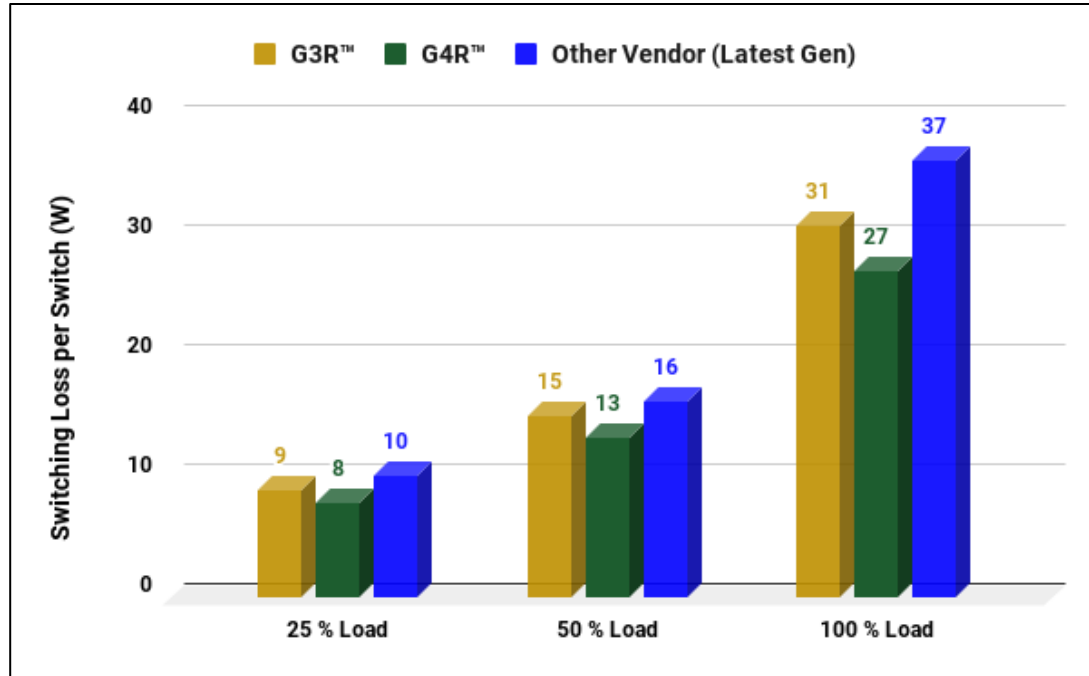
- ~20% reduction in conduction losses possible when temperature ( $T_J$ ) is in the 85°C – 175°C range.

**G4R™ (750V 12mΩ ; 19.8 mm<sup>2</sup>) v/s G3R™ (750V 10mΩ ; 25 mm<sup>2</sup>) v/s Other Vendor - Latest Gen (750V 10.5mΩ ; 25 mm<sup>2</sup>)**



# Superior Drive Cycle Efficiency with Better SiC MOSFET Technology

Working Load v/s Switching Losses per Switch (W) ;  $f = 10 \text{ kHz}$



## FULL LOAD – 100 %

**$I_{\text{RMS}} = 450 \text{ A}$**  (AC Phase Output Current; 3-Ph Inverter)

**$I_{\text{RMS-SW}} = 280 \text{ A}$**  (Per Switch Position)

(4 Paralleled Dies per Switch Position; 70A RMS per Die)

## NOMINAL LOAD – 50%

**$I_{\text{RMS}} = 250 \text{ A}$**  (AC Phase Output Current; 3-Ph Inverter)

**$I_{\text{RMS-SW}} = 155 \text{ A}$**  (Per Switch Position)

(4 Paralleled Dies per Switch Position; 38A RMS per Die)

### ✓ Full Load Condition

➤ ~25% reduction in switching losses possible (comparing G4R™ v/s closest SiC competitor)

### ✓ Nominal Load Condition

➤ ~18% reduction in switching losses possible (comparing G4R™ v/s closest SiC competitor)



# Criteria to Judge SiC MOSFETs

## METRICS

## WHAT IS REQUIRED ?

## HOW TO ASSESS ?

### Performance

- Superior Figure-of-Merit (FoM)
- Efficient and Cooler Operation under all Conditions

- ✓ **Low  $R_{ON(SP)}$**
- ✓ **Better Temperature Coefficient of  $R_{DS(ON)}$**
- ✓ **Better Switching Performance**

### Robustness

- Avalanche Robustness
- Short-Circuit Robustness

- ✓ **Sufficient  $E_{AS}$  Rating**
- ✓ **Sufficient Short Circuit Withstand Time**

### Reliability

- No  $V_{TH}$  Drift (Reliable Gate Oxide)
- Stable Performance under Body Diode Operation

- ✓  **$V_{TH}$  Stability Under NBTS and PBTS**
- ✓ **DIBL Effect ( $V_{TH}$  v/s  $V_{DS}$ )**
- ✓ **Body Diode Reliability**

### Quality

- Robust manufacturing process
- Automotive-qualified production line

- ✓ **Tight  $V_{TH}$  and  $R_{DS(ON)}$  Distribution**


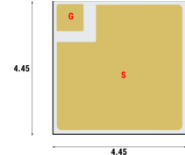
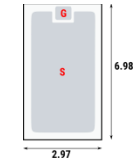
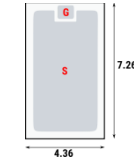
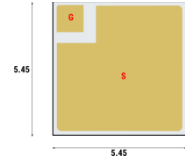
### Price

- Competitive price and Fast turn-Around
- Supply Chain Stability and Superiority

- ✓ **Low  $R_{ON(SP)}$  for Lower Cost**
- ✓ **Robust Supply Chain**
- ✓ **Capacity and Turn-Around Times**

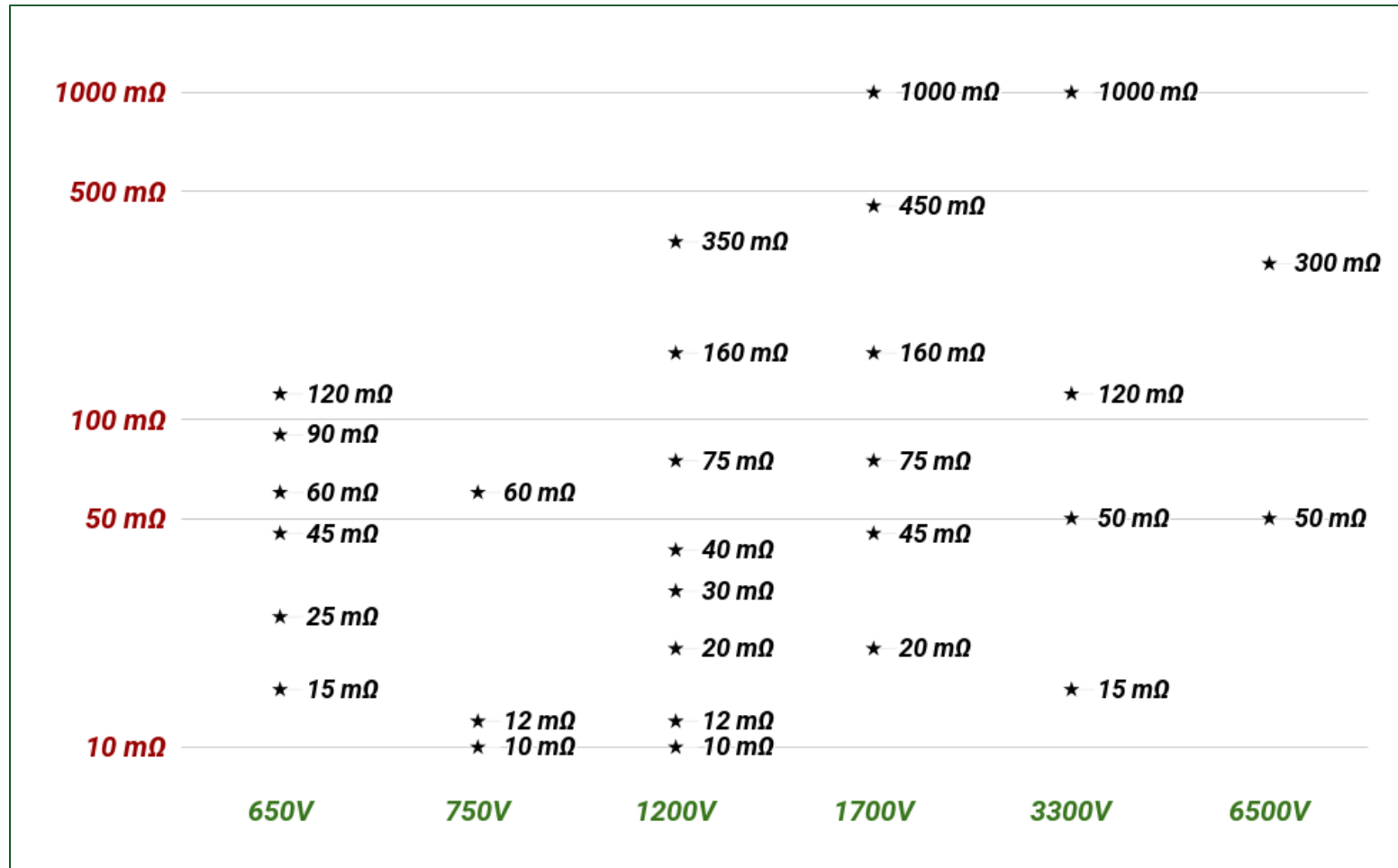


# SiC MOSFET Bare Chips for EV/HEV Traction Inverters

		P/N	Technology	Metallization	Image
750V	10 mΩ	G3R10MT07-CAU	G3R™	Top-Side : Ni+Pd+Au Back-Side : Ni+Pd+Au	 A square chip with a 5.00 mm width and 5.00 mm height. It features a central square region with a red 'S' and four smaller square regions at the corners with red 'G's.
	12 mΩ	G4R12MT07-CAU	G4R™	Top-Side : Ni+Pd+Au Back-Side : Ni+Pd+Au	 A square chip with a 4.45 mm width and 4.45 mm height. It features a central square region with a red 'S' and a small square region at the top-left corner with a red 'G'.
1200V	20 mΩ	G3R20MT12-CAL	G3R™	Top-Side : Al Back-Side : Ni+Ag	 A rectangular chip with a 2.97 mm width and 6.98 mm height. It features a central rectangular region with a red 'S' and a small square region at the top-left corner with a red 'G'.
	12 mΩ	G3R12MT12-CAL	G3R™	Top-Side : Al Back-Side : Ni+Ag	 A rectangular chip with a 4.36 mm width and 7.26 mm height. It features a central rectangular region with a red 'S' and a small square region at the top-left corner with a red 'G'.
	10 mΩ	G4R10MT12-CAU	G4R™	Top-Side : Ni+Pd+Au Back-Side : Ni+Pd+Au	 A square chip with a 5.45 mm width and 5.45 mm height. It features a central square region with a red 'S' and a small square region at the top-left corner with a red 'G'.



# Most Comprehensive SiC MOSFET Portfolio – 650V to 6500V



## 50+ SiC MOSFET Products

- ✓ **650V/750V** → 10 mΩ to 120 mΩ
- ✓ **1200V** → 10 mΩ to 350 mΩ
- ✓ **1700V** → 20 mΩ to 1000 mΩ
- ✓ **3300V** → 15 mΩ to 1000 mΩ
- ✓ **6500V** → 50 mΩ to 300 mΩ





# Questions

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