Feature Integration in GaN towards a Compact and Intelligent System Design

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Presented at APEC, March 23th, 2022, Paper IS07.6

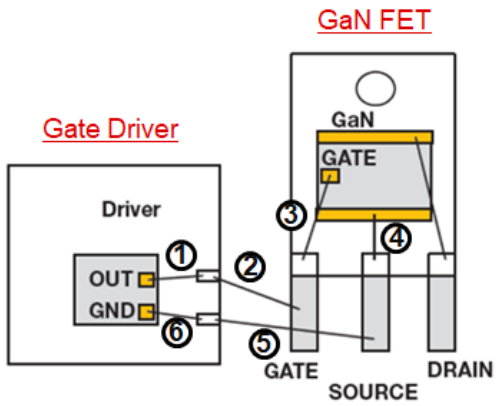
Presenters Bio:

Dr. Fei Yang received the M.S. degree from The University of Tennessee, Knoxville, in 2017, and the Ph. D. degree from the University of Texas at Dallas, in 2020, all in electrical engineering. Since 2020, he has been a system and application engineer at GaN product line in Texas Instruments.

Outline

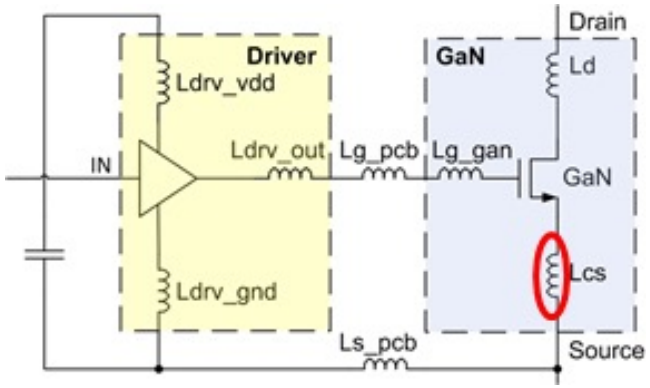
- **TI GaN Gate Driver Integration Benefits**
- **TI Gen-II GaN Feature Integration Overview**
  - Integrated gate driver for high *dv/dt* and adjustable slew rate
  - Current sensing for over-current and short-circuit protection
  - Integrated power supply
  - Junction temperature sensing
  - Ideal diode mode operation
  - Over temperature shut down protection
- **Summary**

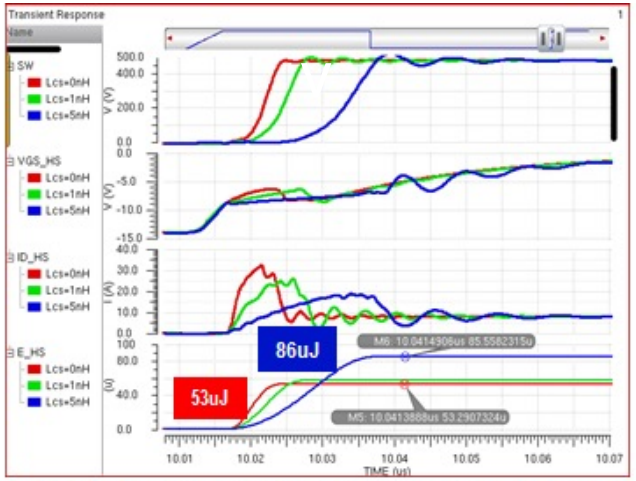
High-Frequency Design Challenges



- **Common Source Inductance (CSI)**
  - Slows V_{DS} transitions.
  - Higher overlap losses (Hard-Switching).
  - Longer dead-times (Soft-Switching).
- **Gate Loop Inductance**
  - Limit peak gate current: slow down gate drive and induce high overlap losses in hard switching.
  - Gate overstress reliability risk.
  - Miller shoot-through risk.
- **White Paper:** Optimizing GaN performance with an integrated driver

Common Source Inductance Effect

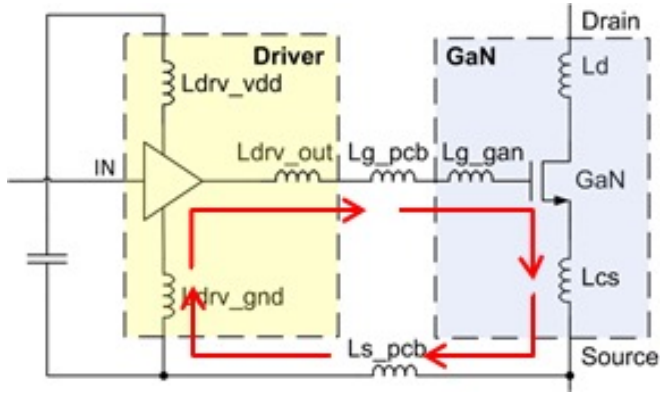


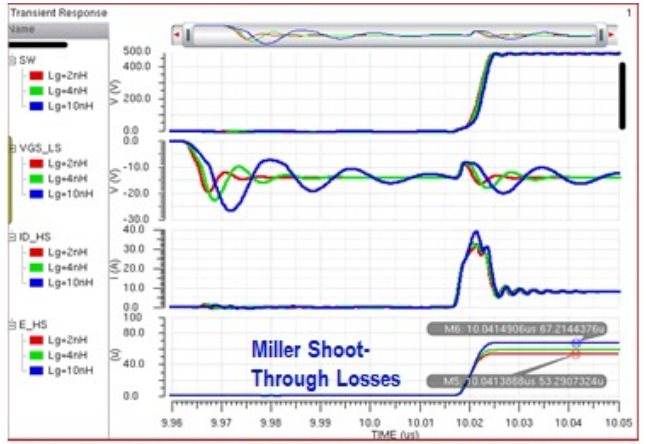


High-side turn on versus common-source inductance:
red = 0 nH, green = 1 nH, blue = 5 nH

Limits peak I_{DS}, De-biases V_{GS}

Gate Loop Inductance Effect





Low-side hold-off versus gate-loop inductance
red = 2 nH, green = 4 nH, blue = 10 nH

Limits peak I_{GATE} & slows down dV_{DS}/dt
Causes V_{GS} ringing & Miller shoot-through

LMG342x/352x: TI Gen-II GaN Feature Overview

>150 V/ns Drain-Source Slew rate capability; **adjustable from 30 V/ns to 150 V/ns**

Integrated **2.2-MHz** gate driver with industry's most comprehensive control and protections

LMG342x: 600-V GaN
LMG352x: 650-V GaN

Ideal diode mode **reduces reverse conduction losses**

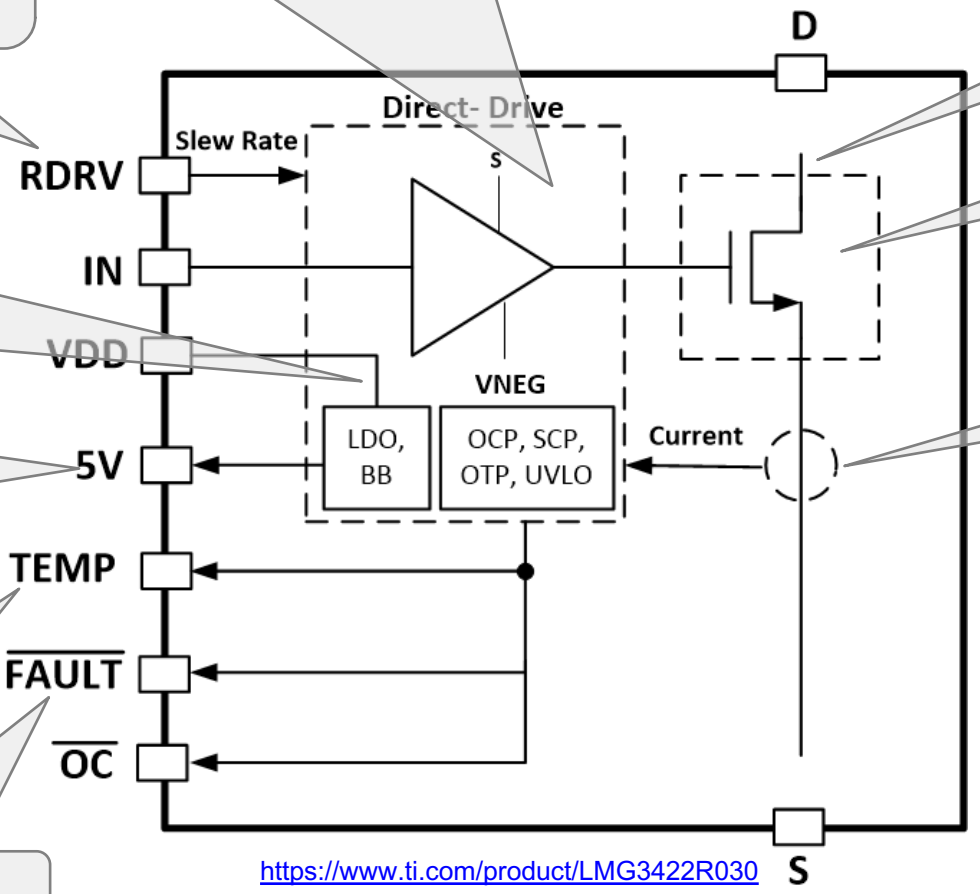
Integrated gate driver bias generated from 7.5-18 V unregulated supply supporting **2.2-MHz switching**

Overcurrent protection **Cycle-by-Cycle**
Short circuit protection **Latched**

5-V regulated output **for powering digital isolator**

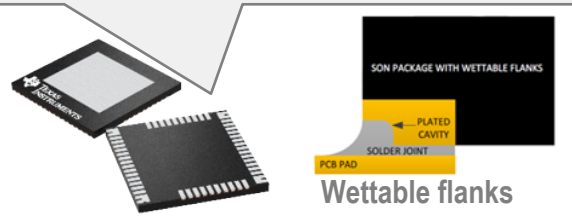
GaN FET temperature digital PWM reporting for **active power management**

V/I/T **fault reporting**



https://www.ti.com/product/LMG3422R030
https://www.ti.com/product/LMG3522R030-Q1

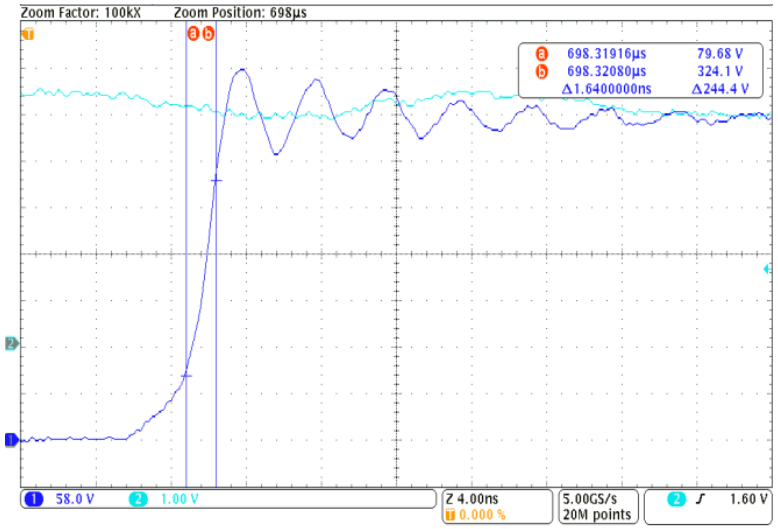
12mm-by-12 mm QFN
LMG342x: bottom-cooled
LMG352x: top-cooled QFN with wettable flanks



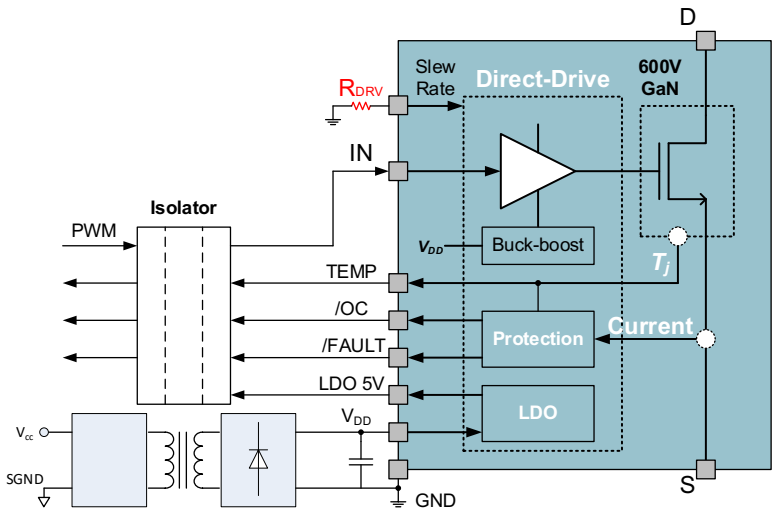
Wettable flanks

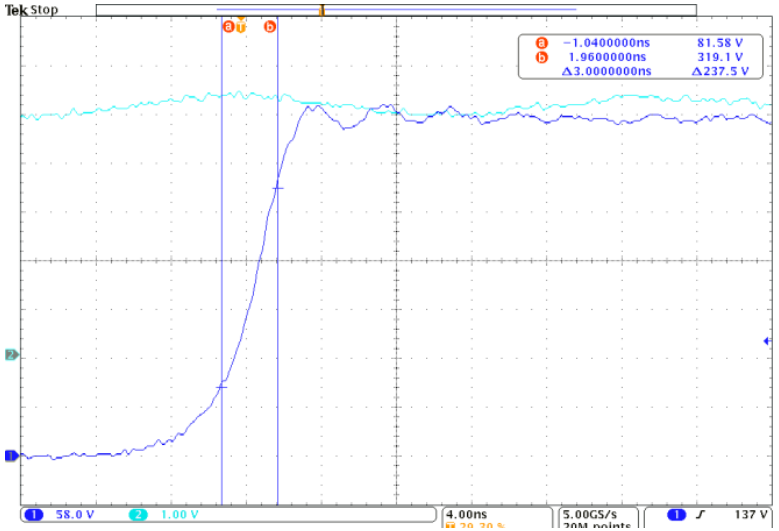
Integrated Drive for High *dv/dt* with Good Noise Immunity

- **High *dv/dt* Capability of TI GaN**
  - Tested in Buck converter at 400V, and the turn-on *dv/dt* reach **150V/ns** (defined from 20% to 80% of bus voltage) without any noise issues.
- **Adjustable Slew Rate Control**
  - The turn-on *dv/dt* slew rate can be adjusted according to different R_{drv} resistances.
  - The adjustable slew rate (**30V/ns to 150V/ns**) facilitates the system design for trade-offs between switching loss and EMI / voltage ringing spikes.



149 V/ns



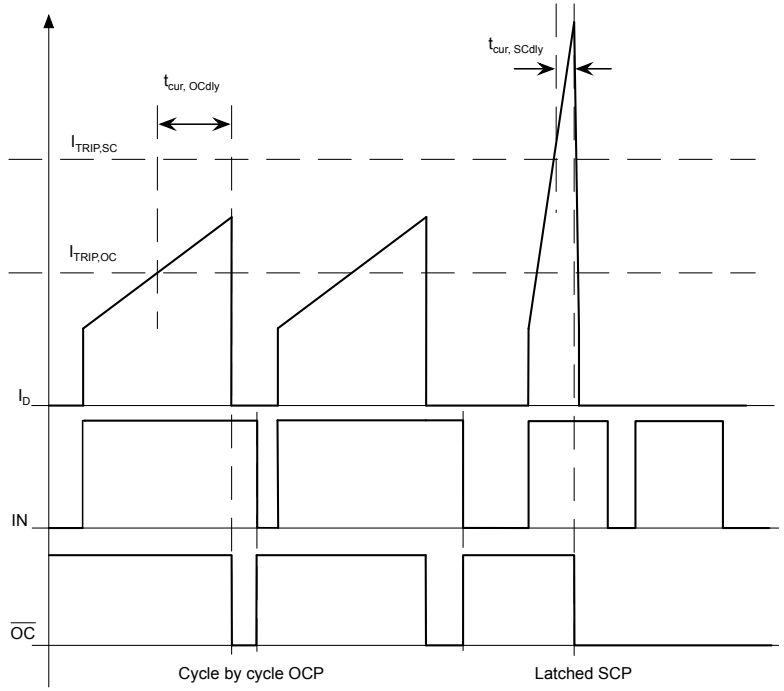


80 V/ns

Protection Features

- **Over Current and Short Circuit Protection**
  - <100ns over-current protection with zero external components to protect the system.
  - Cycle by cycle feature allows system to ride through transients.
  - <100ns response time for short-circuit condition to protect catastrophic event. The short-circuit fault is latched off for system intervention.

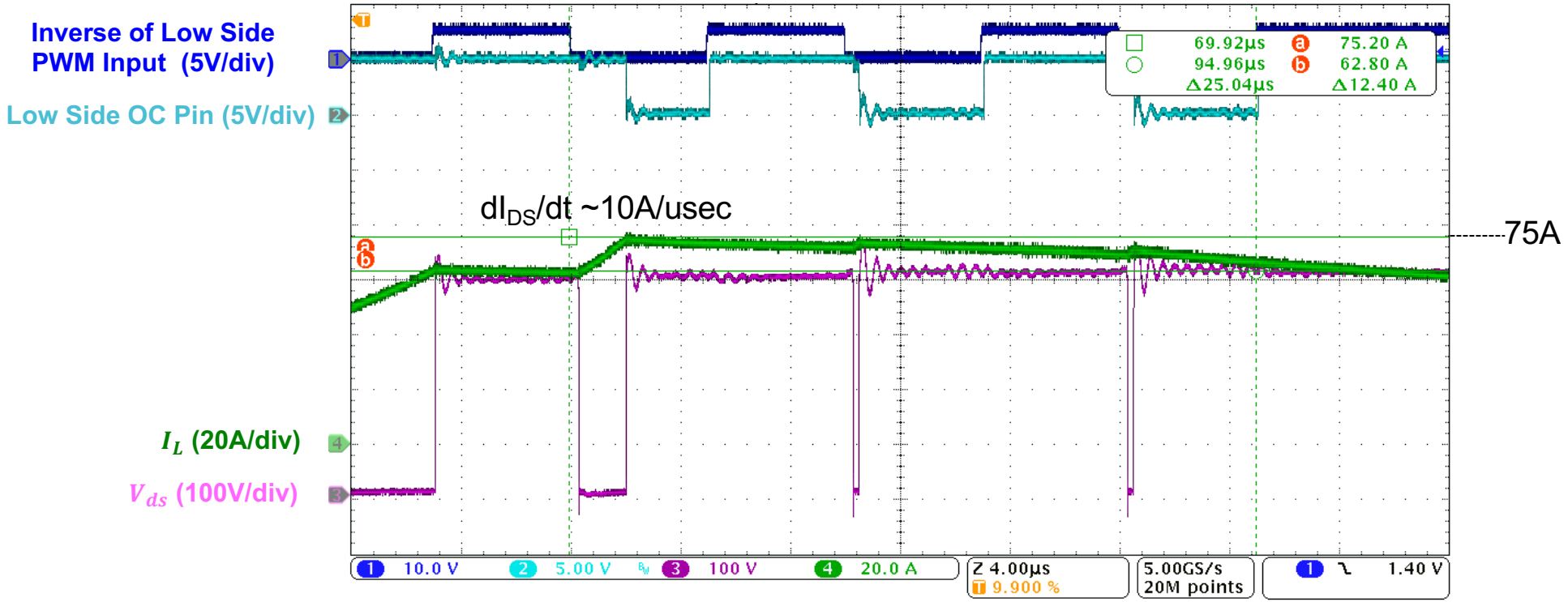
	Action
Over-Current Protection	Cycle-by-Cycle
Short-Circuit Protection	Latched-off



Over-current Detection vs. Short-circuit Detection

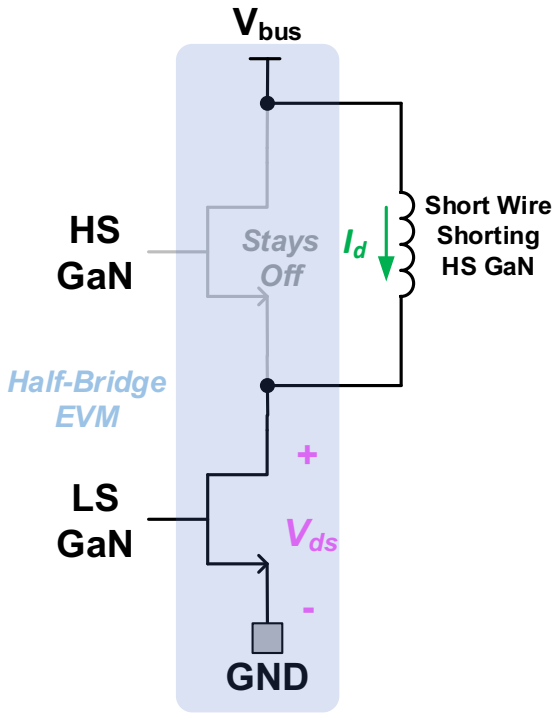
Cycle-by-Cycle Over Current Protection (OCP)

- **Condition and Results**
  - Boost converter configuration, and the current builds up when the low-side device is on.
  - When current builds up to ~75A, a cycle-by-cycle OCP is triggered. And the over-current fault is sent to system for feedback.
  - The cycle-by-cycle OCP allows the system to continue delivering power during the transient with certain current limit.

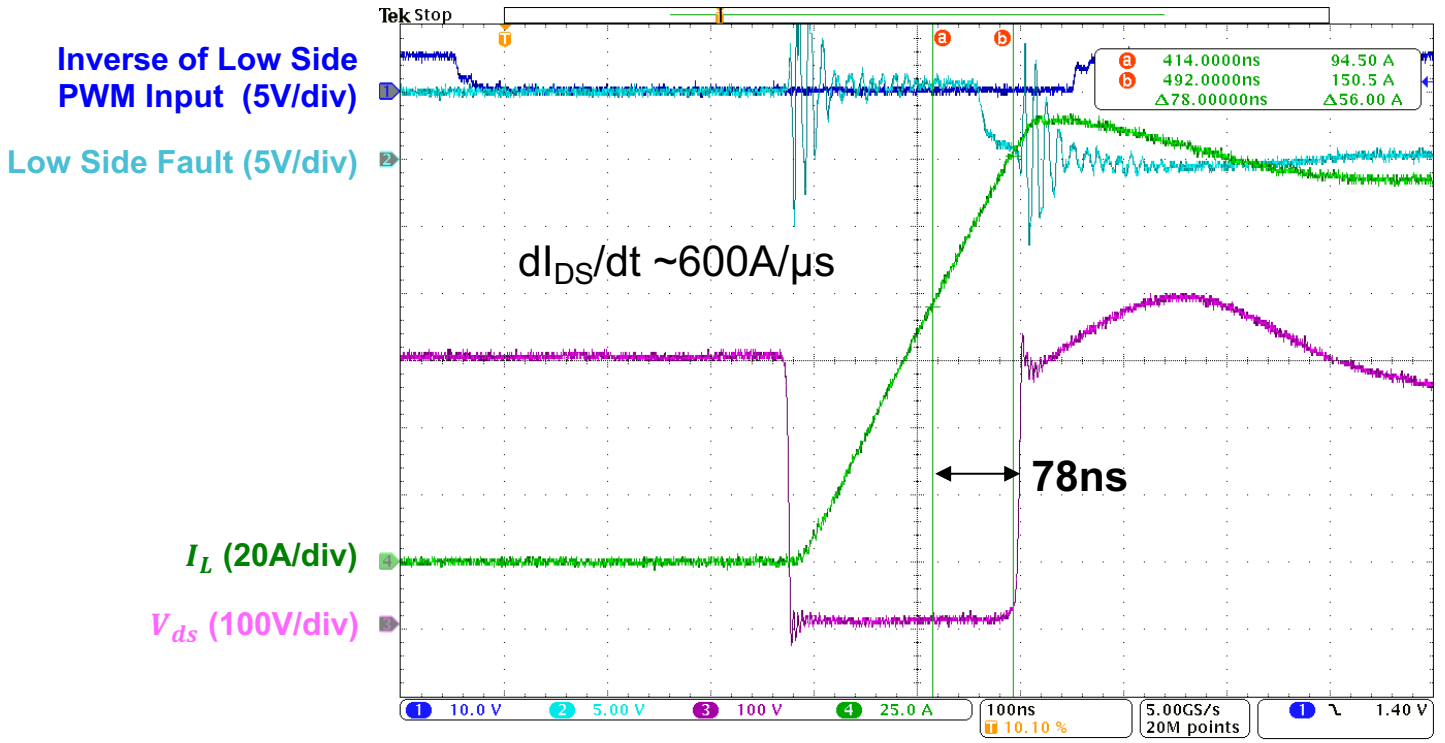


Latched Short Circuit Protection (SCP)

- **Condition and Results**
  - The high-side is in OFF state, and is bypassed by a short wire with low parasitic inductance.
  - The low-side device is stressed by the bus voltage initially, and a short circuit is induced when the low-side device is turned on.
  - The short circuit is detected at “cursor A”, and Soft turn-off action is taken within 78 ns (“cursor B”)



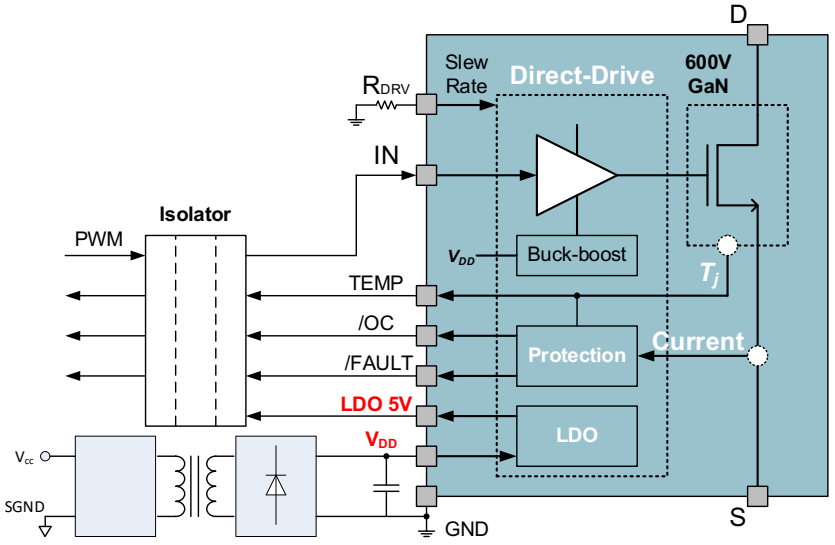
Short Circuit Test Diagram



Short Circuit Test at 400V

Integrated Power Supply

- **Wide Power Supply Input Range**
  - An internal buck-boost converter is used to convert the power supply input V_{DD} to a proper gate drive voltage. This allows an ***unregulated*** input voltage to have a wide range from **7.5V to 18V**.
  - Flexibility to choose different isolated bias power supply solutions with low coupling capacitance (exemplary designs) or bootstrap designs.
- **LDO 5V Output for Peripheral Circuits**
  - LDO 5V eliminates addition power supply to power digital isolator.



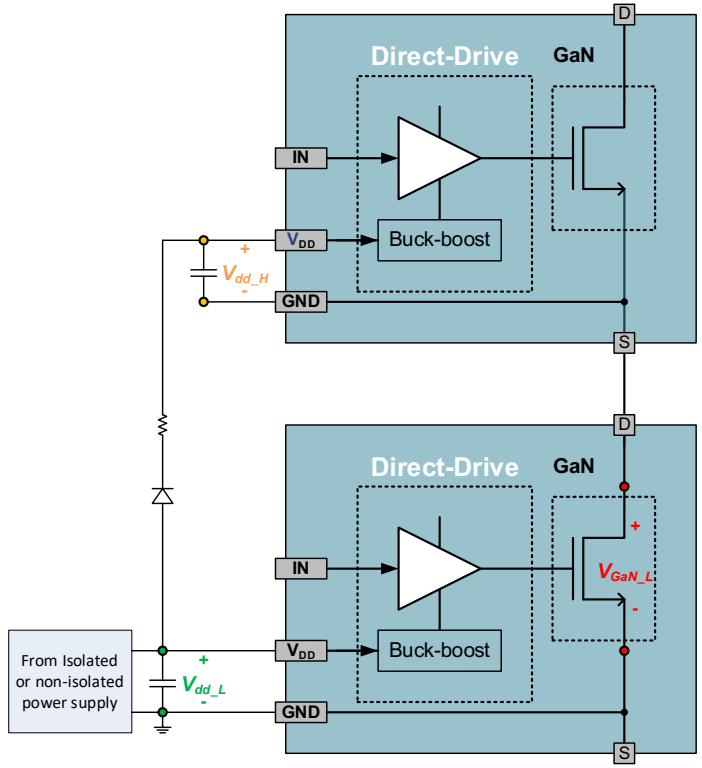
$$V_{dd\_H} \approx V_{dd_L} - V_{GaN\_L}$$

When low-side GaN is conducting **from D to S**:

$$V_{dd\_H} \approx V_{dd\_L} - I_{ds_L} \cdot R_{ds,on\_L} > 7.5V$$

When low-side GaN is conducting **from S to D**:

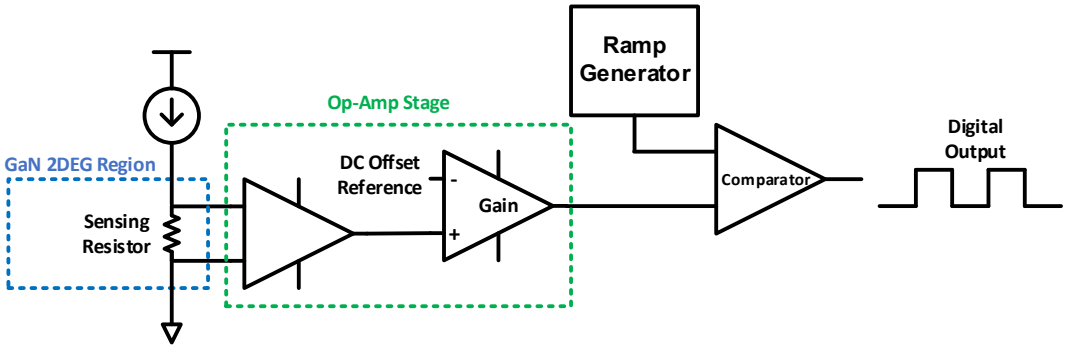
$$V_{dd\_H} \approx V_{dd\_L} + V_{SD\_L} < 18V$$

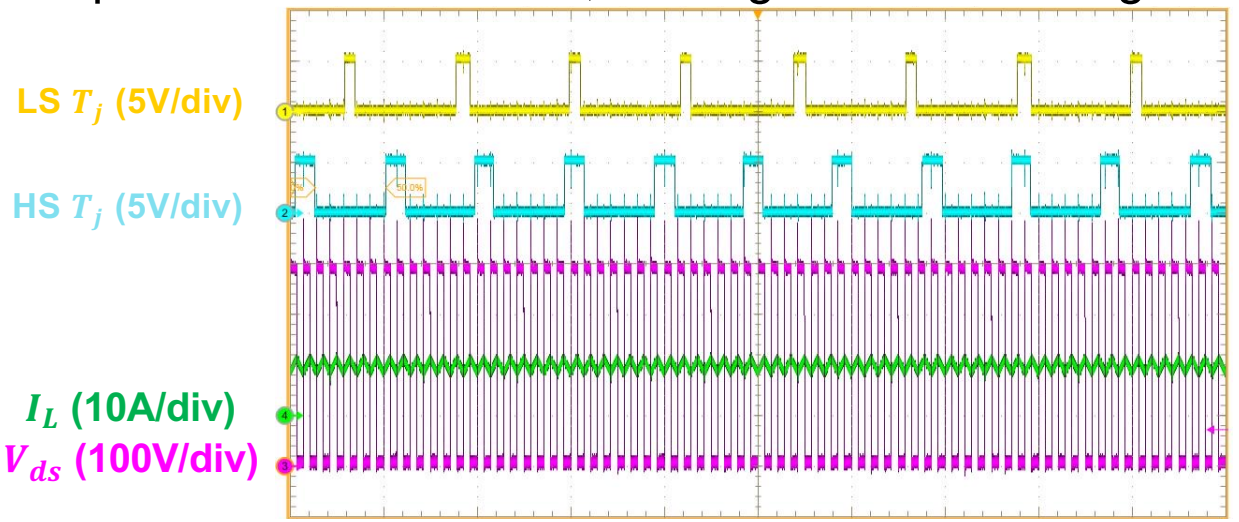


Wide V_{DD} for Bootstrap Design

Temperature Sensing Output

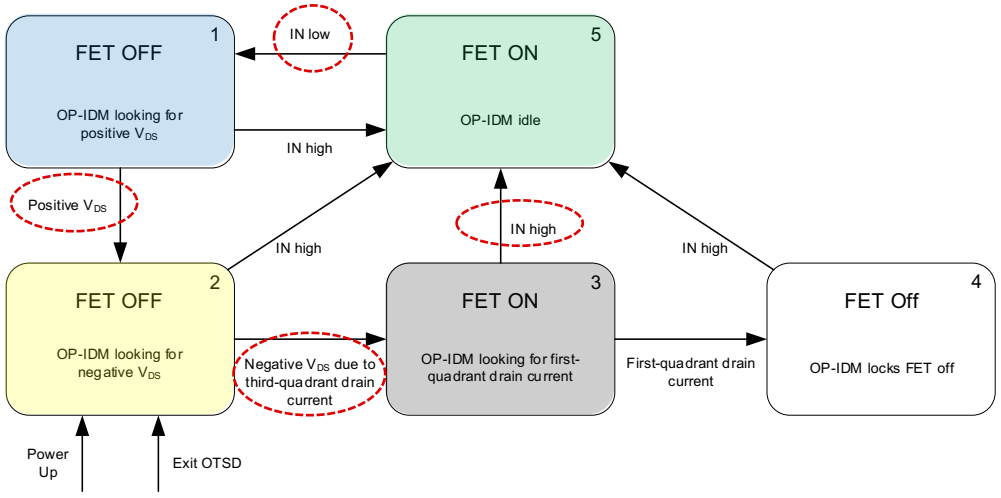
- **Real-Time Junction Temperature Output Through Digital Outputs**
  - The sensing resistor in the 2DEG region is used to measure the junction temperature T_j in real-time. The op-amp, ramp generator circuit, and comparator converted the T_j to a digital output: the duty cycle represents different junction temperature.
  - T_j feedback enables active thermal control (reducing power in compromised thermal conditions) and facilitates the prototype testing process.
- **Exemplary Waveforms in Hard-switching Conditions**
  - Buck converter operation at 400V bus, f_s = 70 kHz, I_L = 10 A, and R_{drv} = 0 Ω at 150 V/ns.
  - Both high-side and low-side GaN's TEMP outputs can be measured, and high-side shows higher T_j.



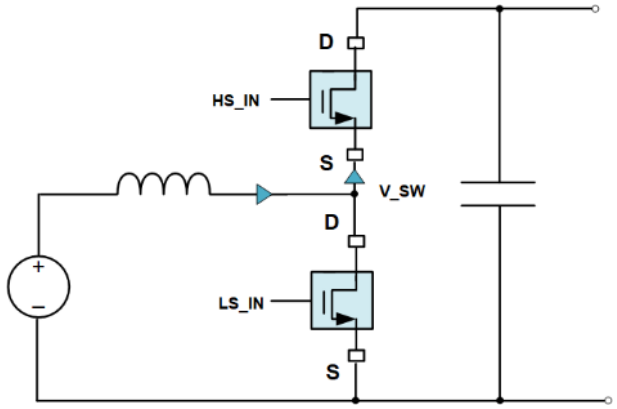


Ideal Diode Mode Operation

- **Operation Principle and Example**
  - At high-frequency operation, the **reverse conduction loss during deadtime** becomes significant.
  - The ideal diode mode (IDM) helps to **reduce** the 3rd quadrant conduction loss by **implementing synchronous FET** operation shortly (~50ns) after a reverse conduction is detected.
  - The reverse conduction detection helps to optimize deadtime loss across different load conditions.



Operational Ideal-Diode Mode (OP-IDM) State Machine of High-side GaN



CCM Boost Converter Example

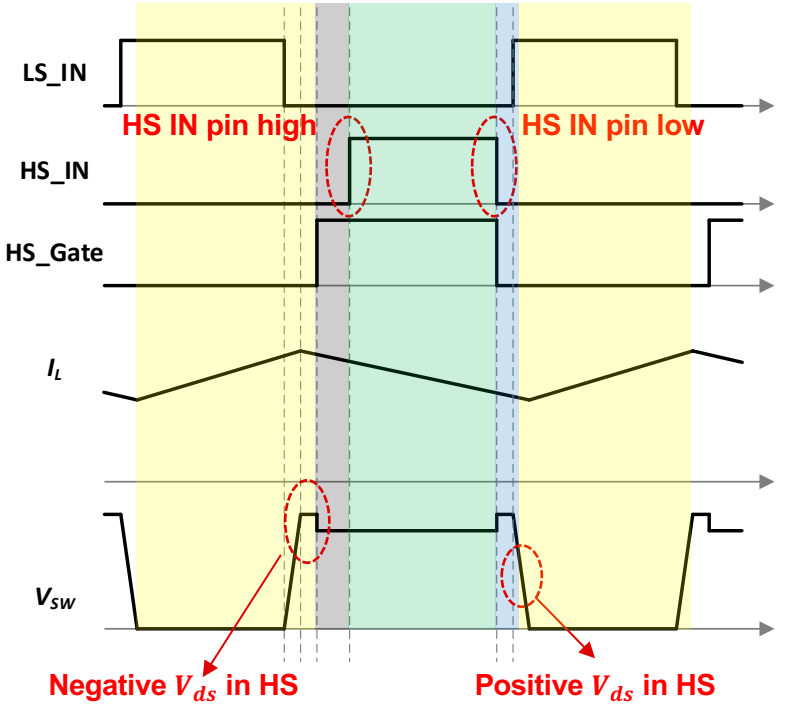
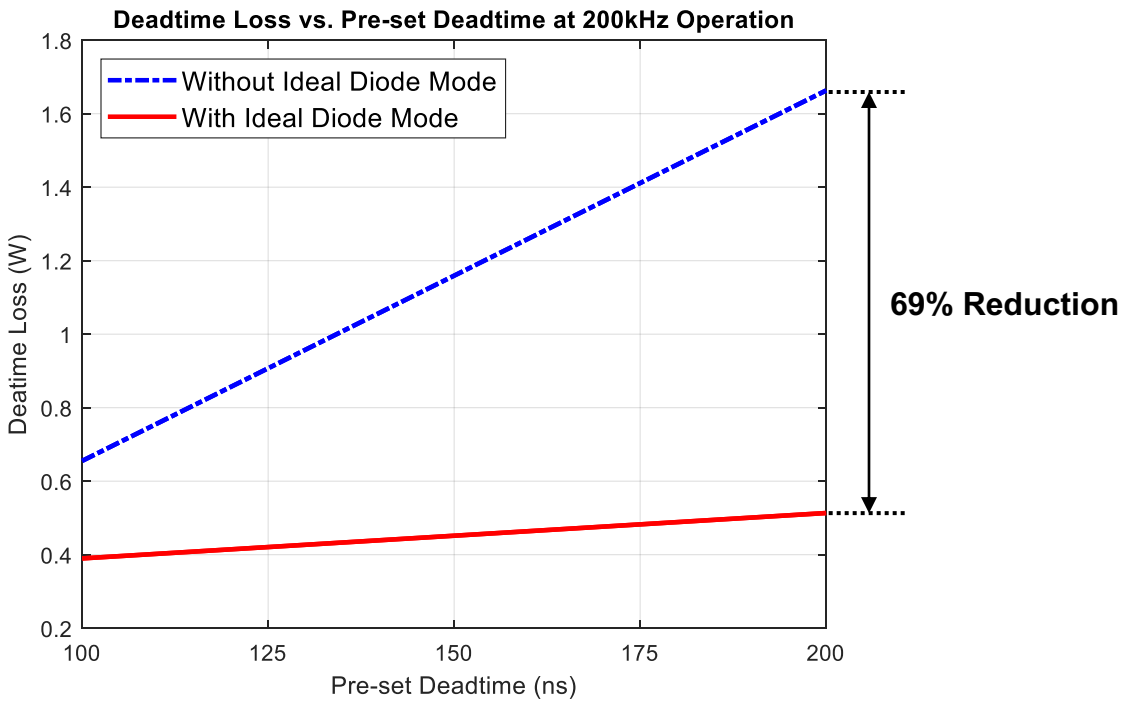
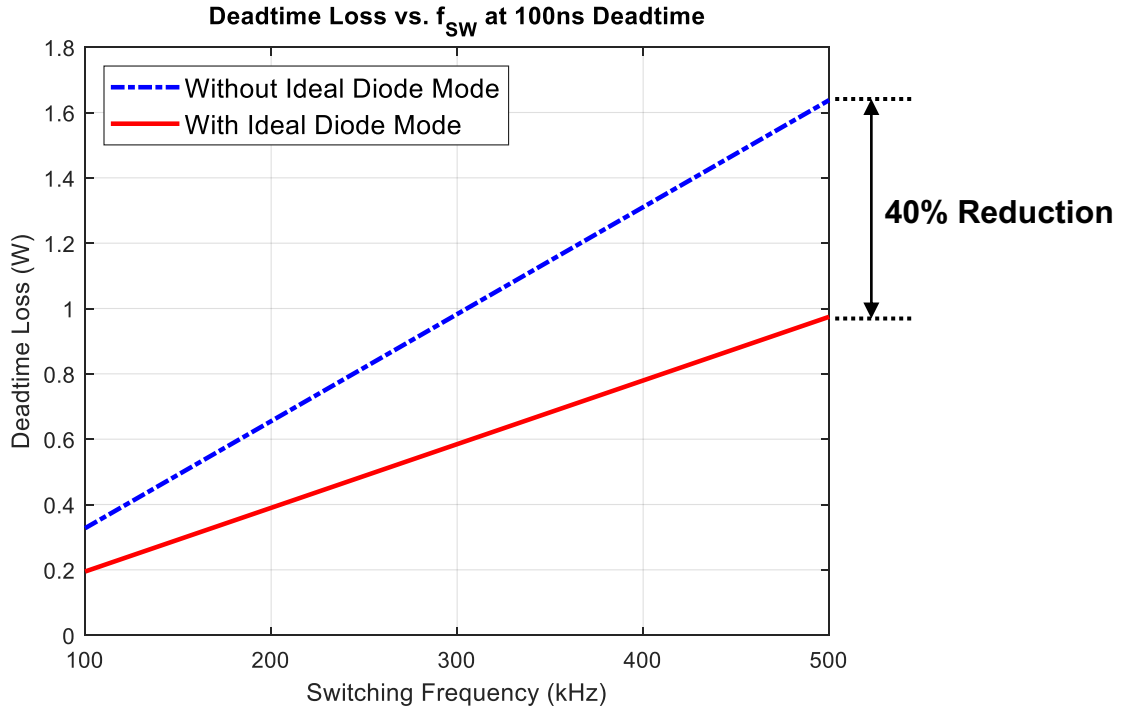


Illustration Waveforms

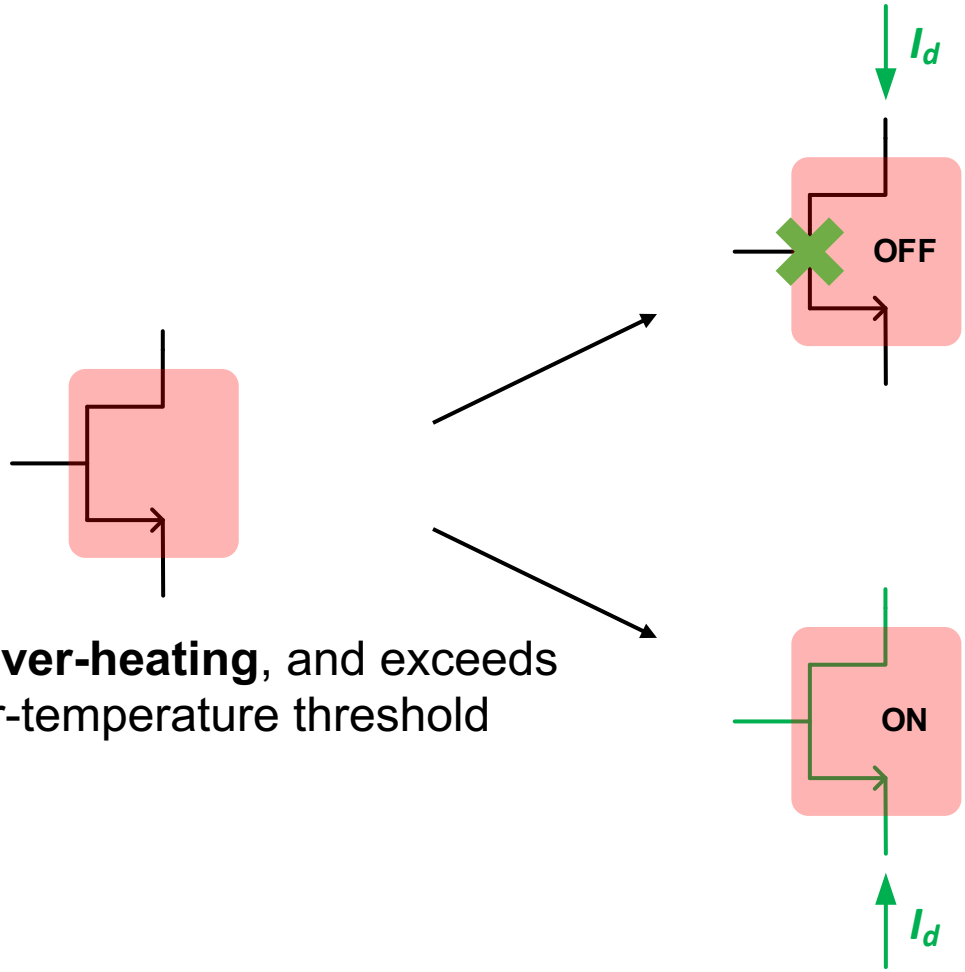
Ideal Diode Mode Operation Benefits

- **Condition and Result**
  - The soft-switching device's deadtime loss before turning-on is considered: I_{SD} = 10.5 A, V_{SD} at high T_j, and the soft-switching transition time is 35 ns.
  - The IDM helps to save reverse conduction loss during deadtime, especially at high frequency or large deadtime conditions.





Over Temperature Shut Down (OTSD)



Device is **over-heating**, and exceeds the over-temperature threshold

Over temperature shut down when current is in 1st quadrant conduction:

- The device will stop switching and remains OFF to avoid further over-heating through conduction or switching losses.

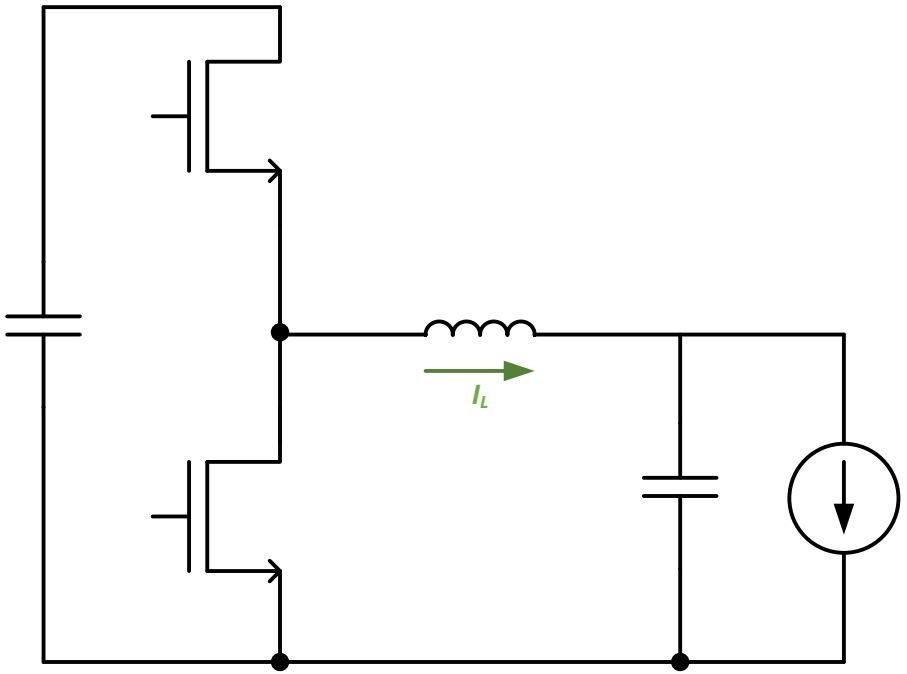
Over temperature shut down when current is in 3rd quadrant conduction:

- The GaN device is turn ON to avoid further over-heating through the reverse conduction losses.

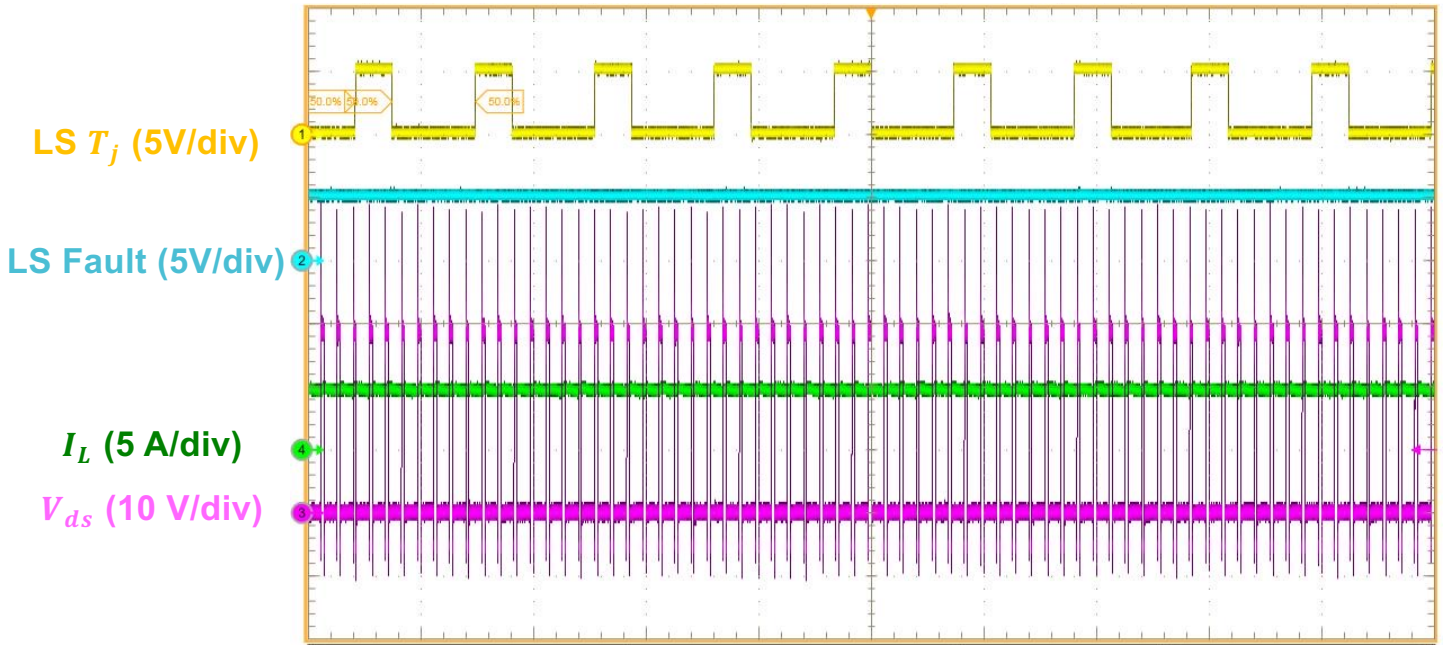
$$I_{SD}^2 \cdot R_{ds,on} \ll I_{SD} \cdot V_{SD}$$

Setup for Over Temperature Shut Down (OTSD)

- **Low Duty Cycle Buck Operation**
  - On the EVM, the heatsink is removed for over-temperature protection test.
  - V_{bus} = 30V, 5A, and low duty cycle (20%, 70 kHz) is implemented such that the load current is heating up the low-side device to trigger over-temperature protection.



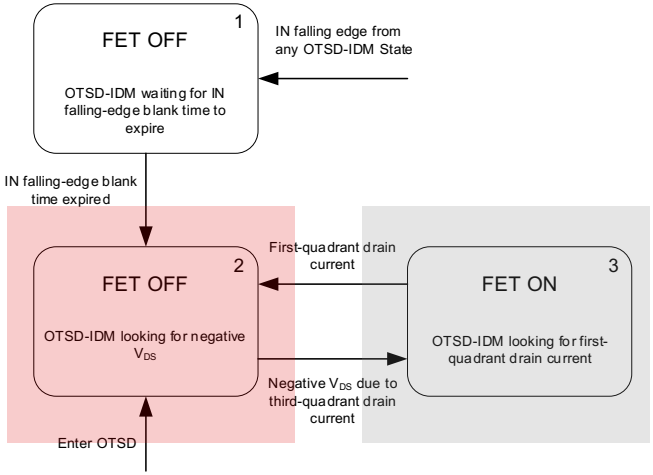
CCM Buck with Load



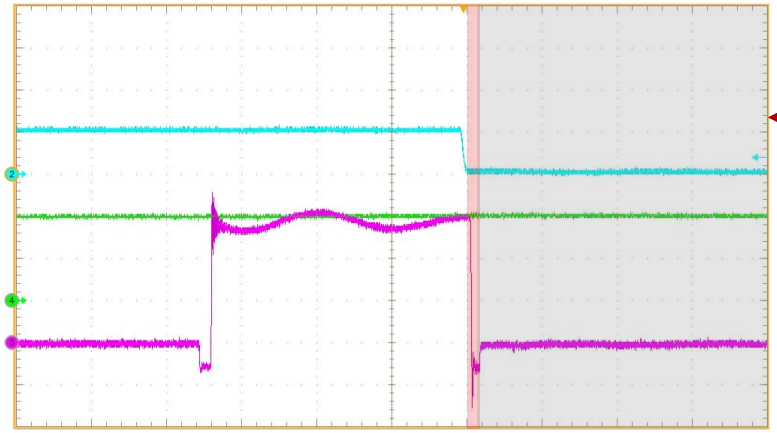
20% Duty Cycle at 30V

Benefits of Ideal Diode Mode of TI Gen-II Device in OTSD

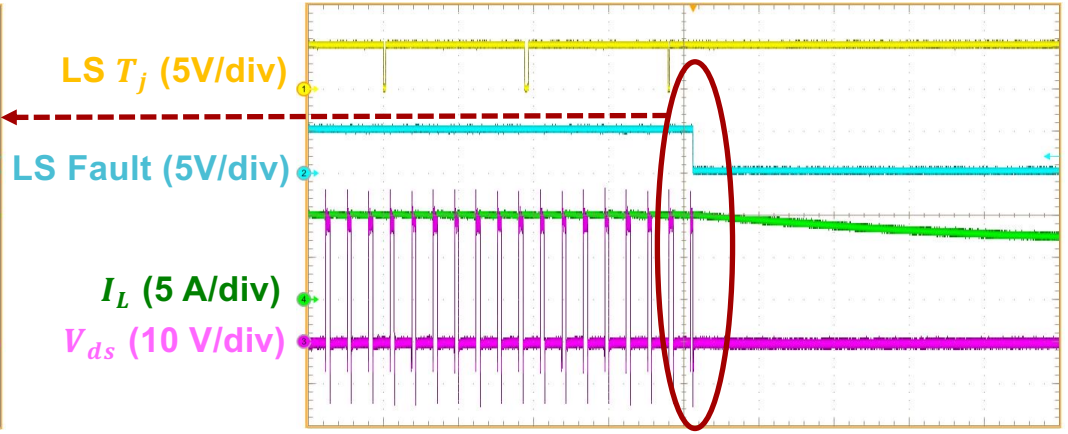
- **Testing Results**
  - Current is increased to **10A** to trigger over-temperature protection, and its T_j is indeed high from sensing signal.
  - The fault signal goes low to indicate the over-temperature fault, and reset **all the PWM signals to OFF state**.
  - When a reverse current is flowing under OTSD condition, instead of going through the high reverse conduction (with the device in OFF state), the device will be in **ON** state to reduce its power loss.
  - This helps to protect the device from further heating and damages.



OTSD-IDM Diagram

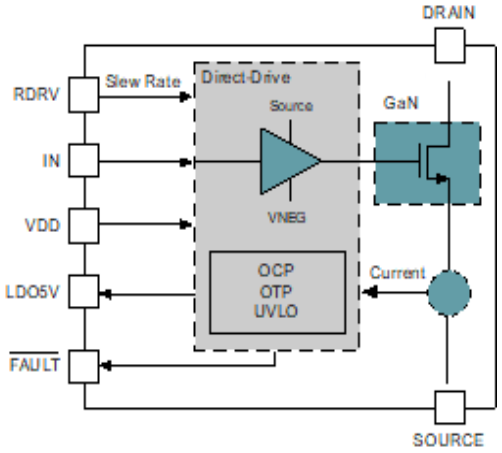


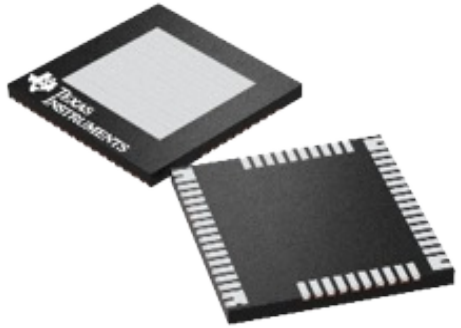
Zoom in of OTSD in TI GaN

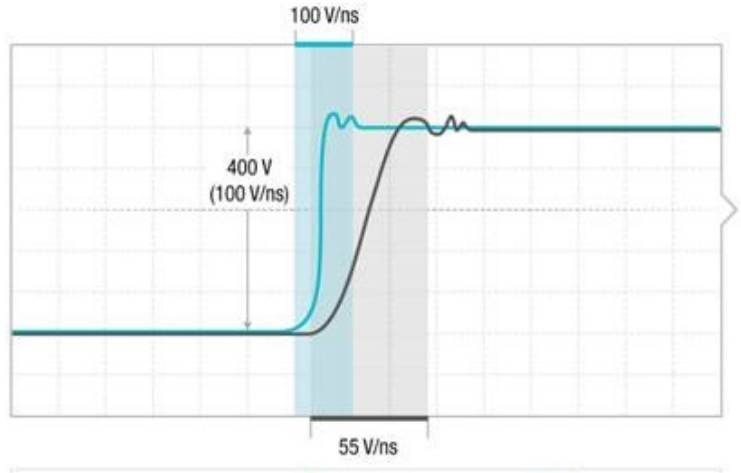


OTSD in TI GaN

Summary: TI GaN Integrated for High Frequency and Robust Operation







Integration and Features

- Integrated gate drive
- Integrated gate driver supply.
- OC/SC protection through current sensing.
- T_j sensing for advanced power management.
- Ideal diode mode operation
- Over-temperature shut down scheme.

+

Compact SMD package

- Low parasitic lead inductance
- Enhanced thermal with Gen-II 12x12 QFN vs. Gen-I 8x8 QFN for 2x power output.
- Flexible thermal management with top-side and bottom-side cooling.

=

Design simplicity & confidence

- Robust switching at high dv/dt.
- EMI consideration.
- Allows different power supply solutions.
- Compact PCB footprint.
- Robust system with on-chip protections.