GaN Integration Enables Next Generation USB-C Chargers with Ultra-High Power Density and Wide Output Voltage Range

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APEC Industry Session 7.3
23 March 2022

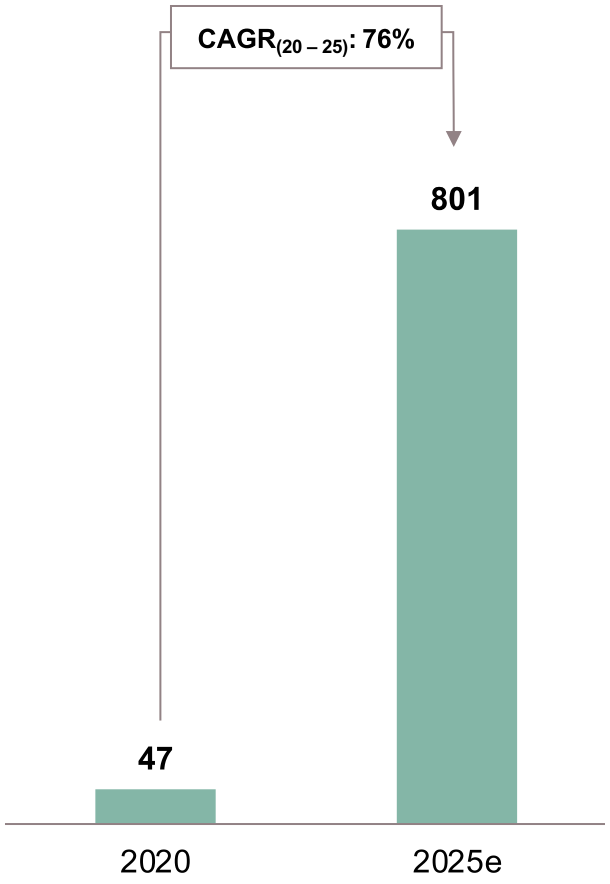
infineon

Outline

Introduction: CoolGaN™ technology – Infineon well positioned to address key markets

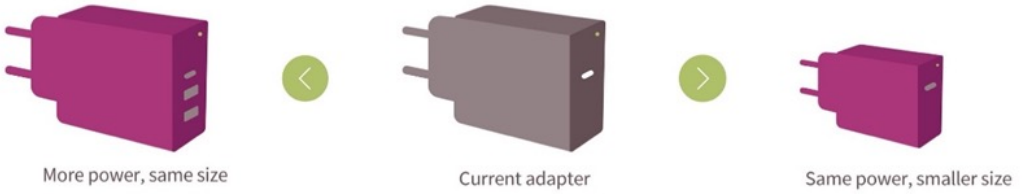
GaN market forecast[1]

[USD m]



Key values of GaN vs Si

Higher power density in adapters and chargers



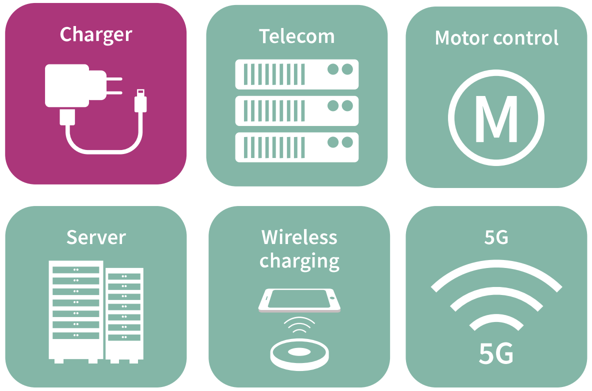
10x	> 2%	20%	25%	3x
switching frequency	more power efficiency	lower System Cost	higher power density	less weight

We combine leading-edge system and application understanding with additional strengths:

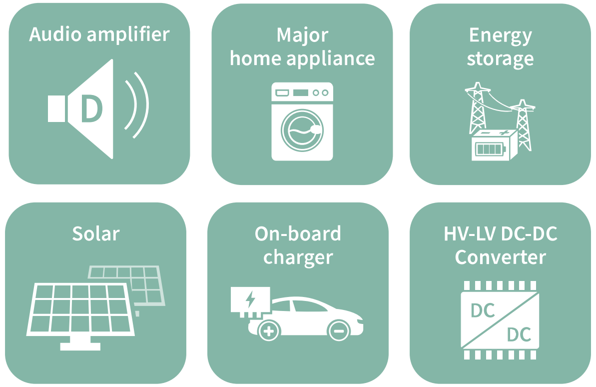
Broad GaN IP portfolio, large R&D force and best-in-class manufacturing landscape

Applications

Focus applications



Emerging applications



1 GaN power devices market forecast. Yole Développement (Yole): *Compound Semiconductor Quarterly Market Monitor: From technologies to markets; Quarterly Update Module 1.* Q3 2021

Specifications of the over-next 240W ultra-high density charger generation

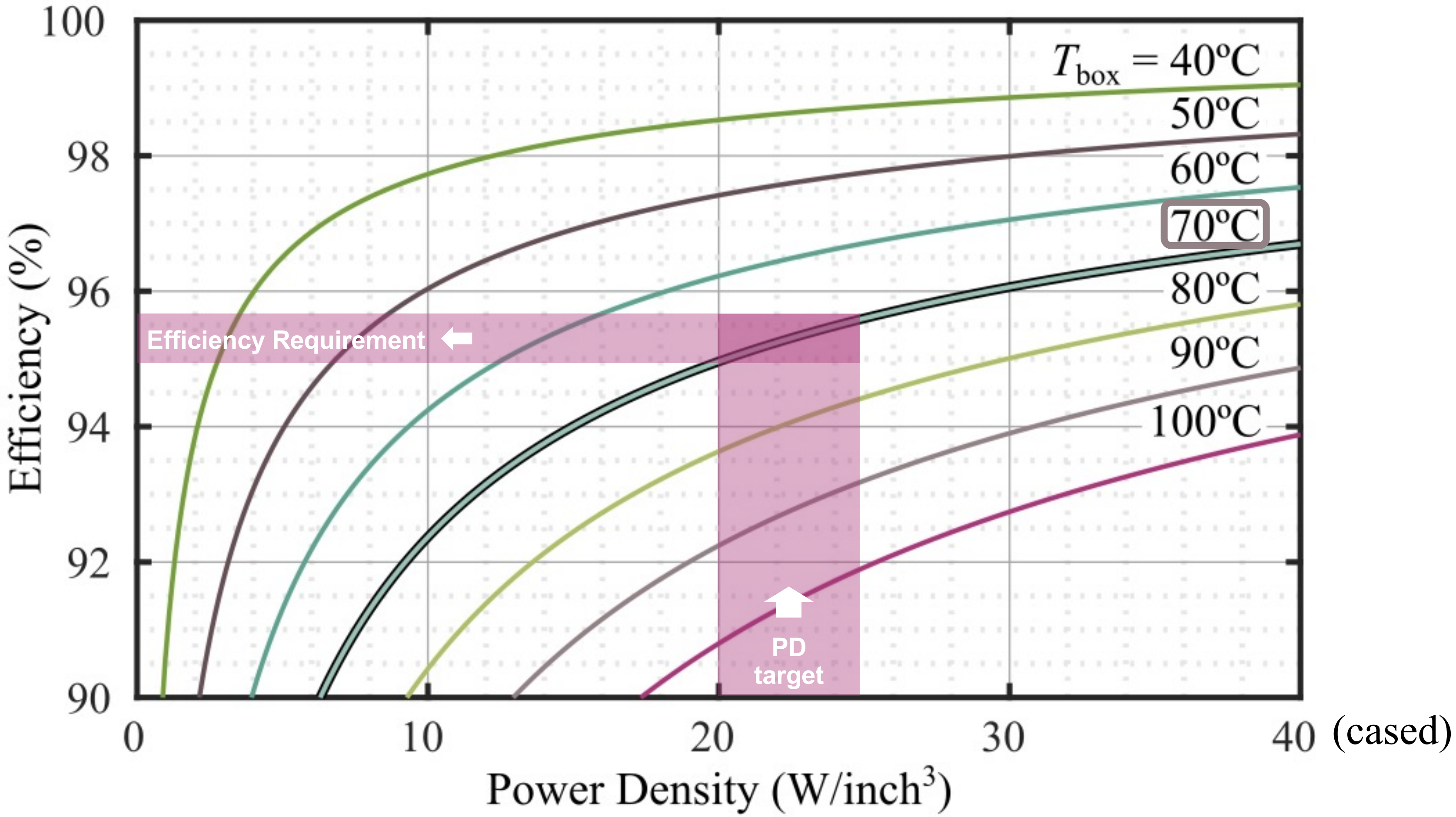
- State-of-the-art 65W chargers soon no longer enough to charge all consumer devices → **Increase to future-proof 240W**
- **Dual USB-C output ports** to support simulatenous charging of two mobile devices
- Increase of **output voltage to 48V** (USB PD Rev. 3.1)

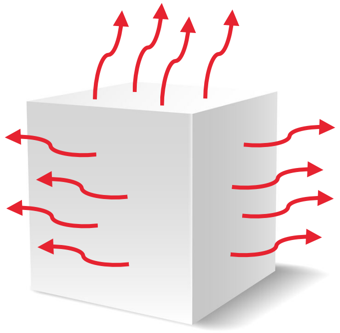
Challenges:
- Dual output
- 240W power → PFC requirement
- Wide input & output voltage ranges
- $90V_{rms}$ thermally most critical

→ **Charger specifications become more similiar to other applications with 48V and >200W like SmartTVs or All-in-One PCs!**

Efficiency & power density performance target for maximum case temperature

› Increasing **power density** requires **higher efficiency** to keep **case temperature within limits**!





Cooling capability is proportional to surface area
→ Lower adapter volume requires lower losses!

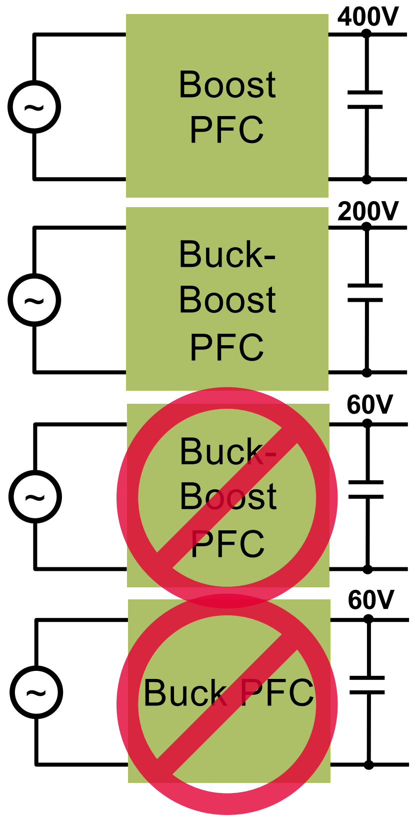
Possible topologies and system partitioning

- Final solution needs to have a **PFC**, **galvanic isolation**, and **two regulated output ports**.
- Based on circuit simulations and rough size/loss estimations several solutions can be ruled out for this project.

PFC Options

„Conventional “

„Novel PFC“



Simple and proven circuit topologies e.g. Totem Pole

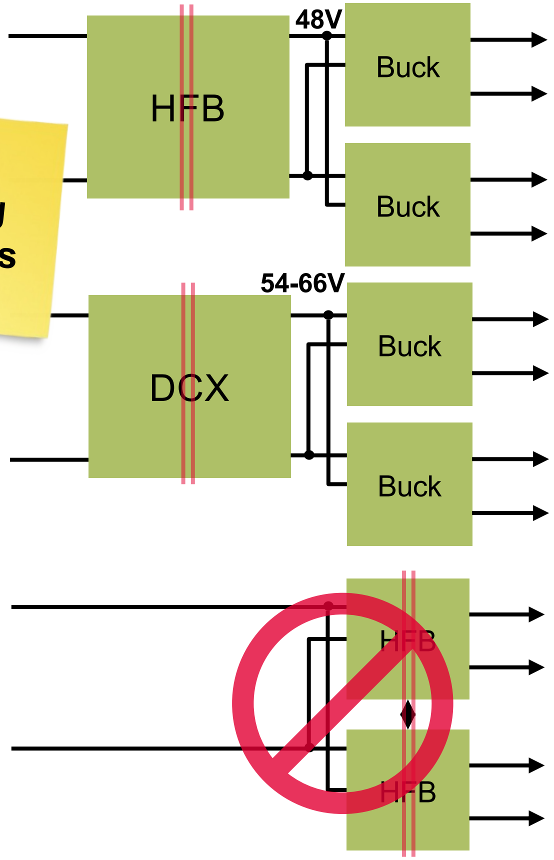
Requires less step-down conversion of DC-DC stages

Low energy density of 80V Caps and large step-down ratio at High Line operation

Leads to intermittent input current and exceeds harmonic emission levels

4 promising combinations

DC-DC Options



HFB can provide regulated output voltage of 48V and can allow to bypass one buck stage

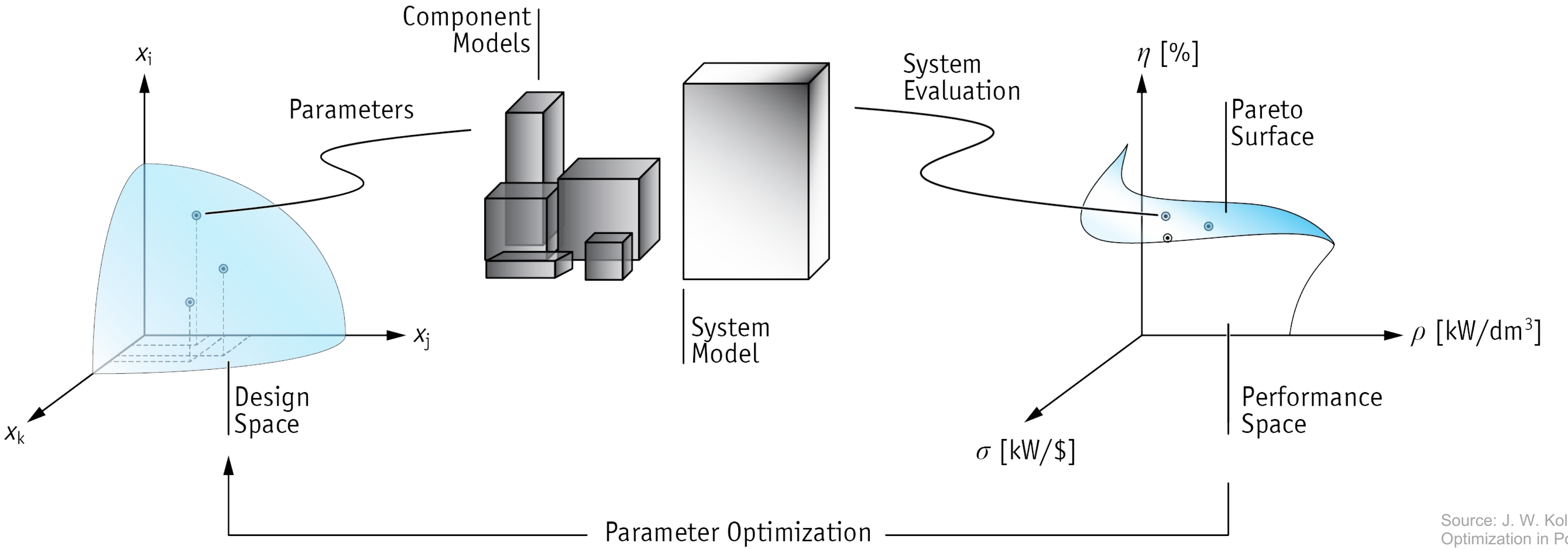
DCX is uncontrolled and doesn‘t store energy in transformer like flybacks

Requires two transformers (both rated for 240W)

HFB: Hybrid Flyback **DCX**: Unregulated series resonant converter

Multi-objective Pareto optimization

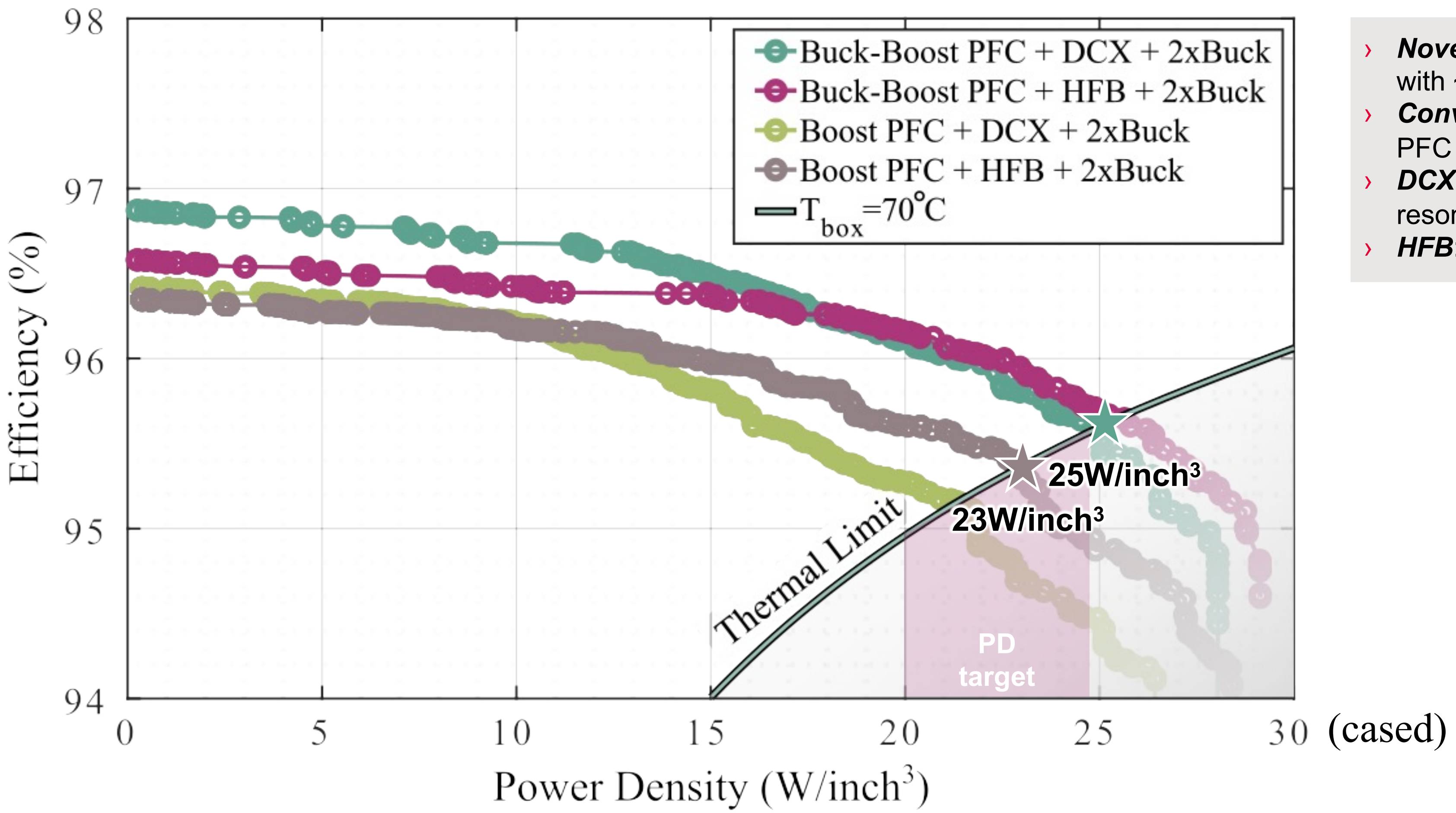
- **Systematic approach** to consider all degrees of freedom
  - E.g.: Semiconductor technologies, # of HF legs in totem-pole, # of matrix transformers, switching frequencies, current/voltage ripples, magnetic component realizations, paralleling of switches
- Comprehensive and **detailed modeling** of **components** and **systems behavior**
- Finding **trade-offs** („Pareto-Front“) between **Efficiency, Power Density, and Costs**



Source: J. W. Kolar, "Multi-Objective Optimization in Power Electronics", Plenary Presentation SPEC, 2016

Pareto optimization of 4 remaining converter options for the most challenging operating point

- Optimization results for **full load (240W)** and low line **(90V$_{rms}$)**



- ***Novel PFC***: Boost+Buck PFC with ~150V output
- ***Conventional PFC***: Totem-Pole PFC with ~400V output
- ***DCX***: unregulated series-resonant converter
- ***HFB***: Hybrid Flyback

Summary of optimization results

23 W/in³	25 W/in³
Conventional Solution (400V DC link): TP + HFB + 2x Buck	**Novel Solution (160V DC link): Boost+Buck PFC + DCX or HFB + 2x Buck**

23 W/in^3

Conventional Solution (400V DC link):
TP + HFB + 2x Buck

Why to use this solution:
- Straightforward solution
- Proven controllers
- Explore higher frequencies (within bounds of controllers)

Risks:
- Might miss target of $20W/in^3$
- Not going to extreme power densities
- Not learning about new topologies
- Missing chance to go to „new territory“

25 W/in^3

Novel Solution (160V DC link):
Boost+Buck PFC + DCX or HFB + 2x Buck

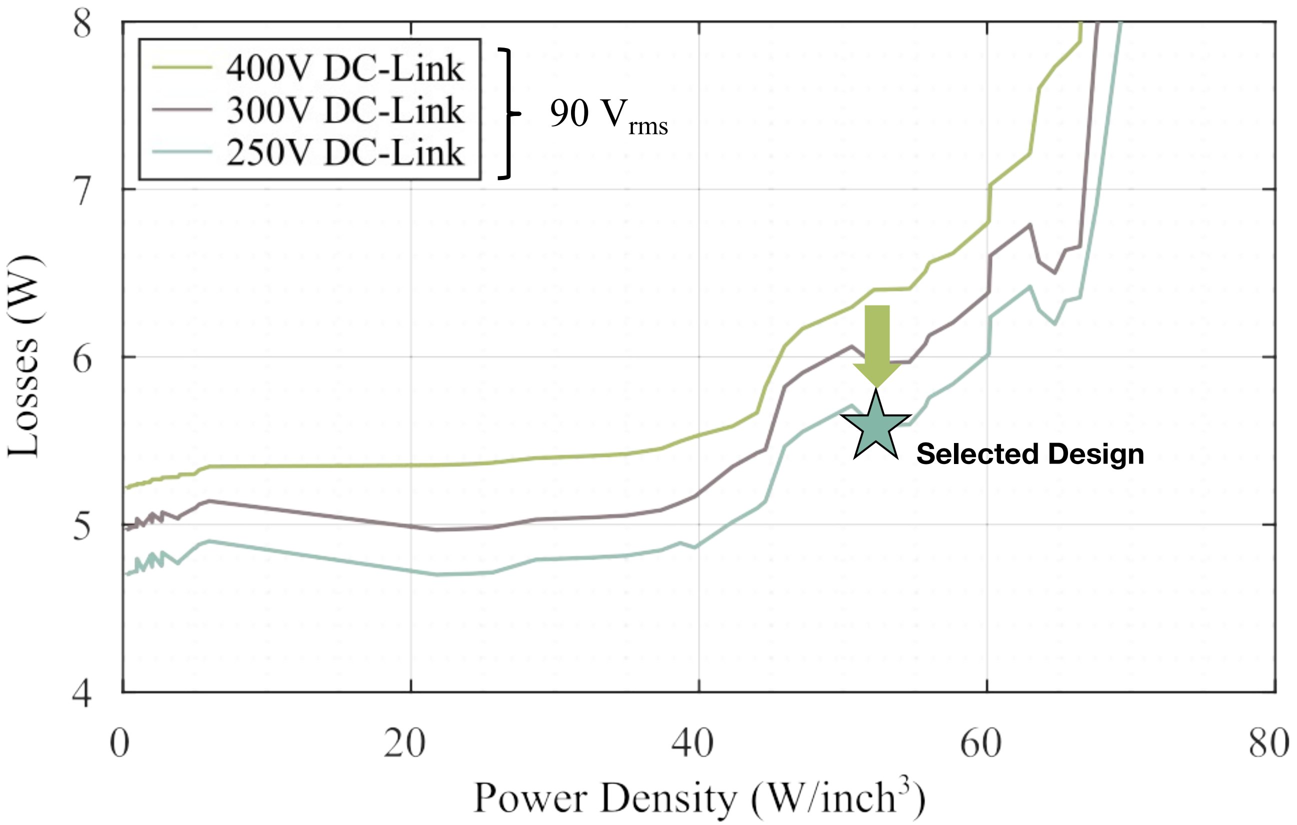
Why to use this solution:
- Highest power density
- Learning about new topology
- Explore highest frequencies with proprietary control

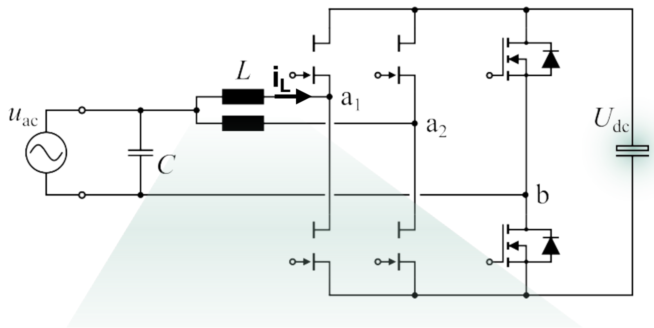
Risks:
- Not fulfilling requirements:
  - Standby power; Harmonics/EMI; Surge; ESD; Safety test (i.e. Short circuit)
- Cost
  - High number of devices; controller development

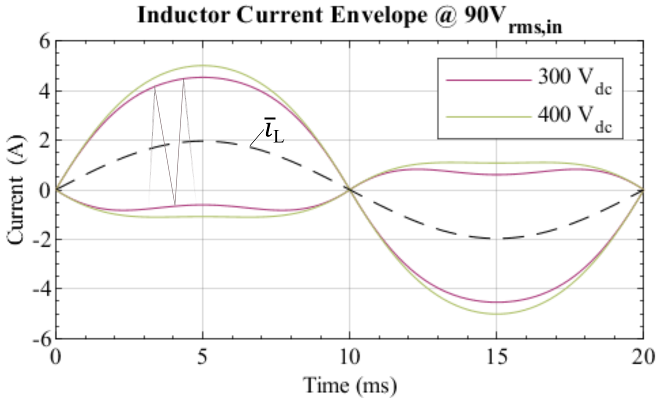
→ **Possibility to combine both solutions: „Boost Follower“ Totem-Pole which is a conventional Totem-Pole that is operated with lower DC-link voltage depending on line voltage**

Boost-Follower PFC operation to maximize efficiency at low-line operation

- Optimization of **Boost-Follower Totem-Pole PFC** stage at 240W and $90V_{rms}$ input





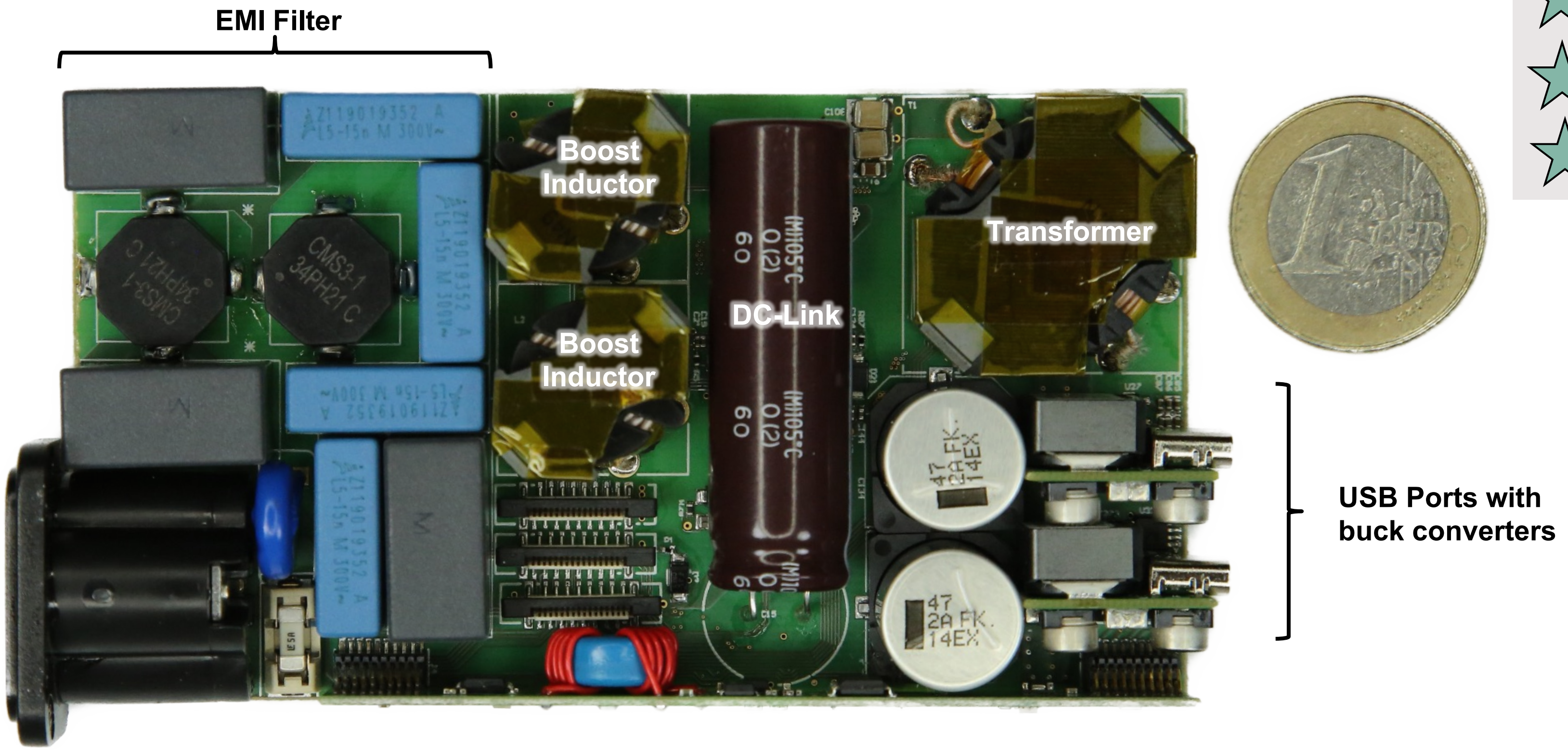


Novel Control Scheme: Variation of DC-link voltage for diff. line voltages to achieve ZVS at fixed f_{sw}

- Reduction of losses at most critical $90V_{rms}$ operating point → High f_{sw} → Low converter volume
- Simplified control without variation of switching frequency like in TCM control
- Easier EMI filter design with defined noise spectrum

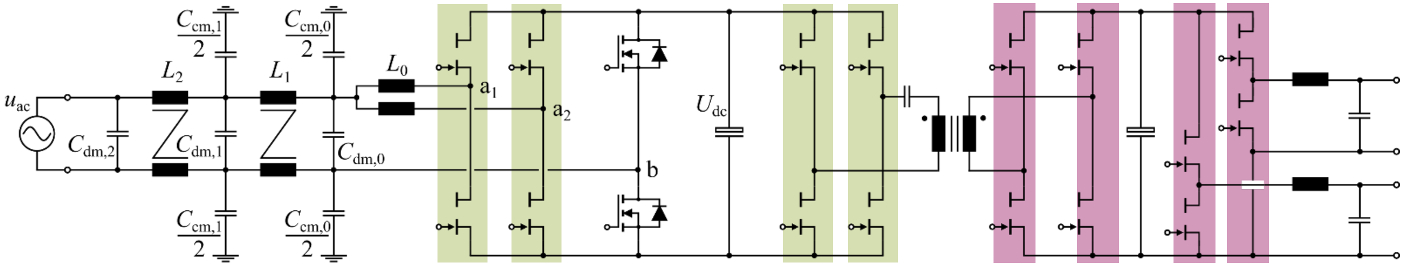
Hardware Demonstrator of Next-Gen 240W USB-C Charger

- Dimensions: W x L x H: **100mm x 55mm x 17mm** without case



- **42 W/inch³** (uncased, 24W/inch³ cased)
- **113 g** (uncased)
- **95.3 % Eff** (240W, 90Vrms)

Topology:
- **Interleaved Totem-Pole**
- **DCX**
- **ZVS Buck converter**



4x 600V 140mΩ$_{typ}$ Integrated GaN Half-bridges

4x 100V 2.5mΩ$_{typ}$ Discrete GaN Half-Bridges

PFC Stage – Details and Measurement Results

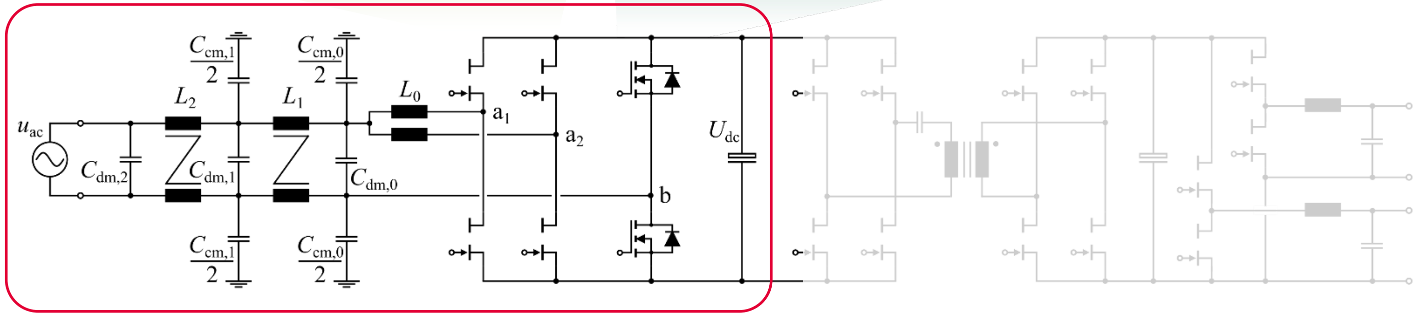
ZVS Totem-pole PFC with 2x interleaving

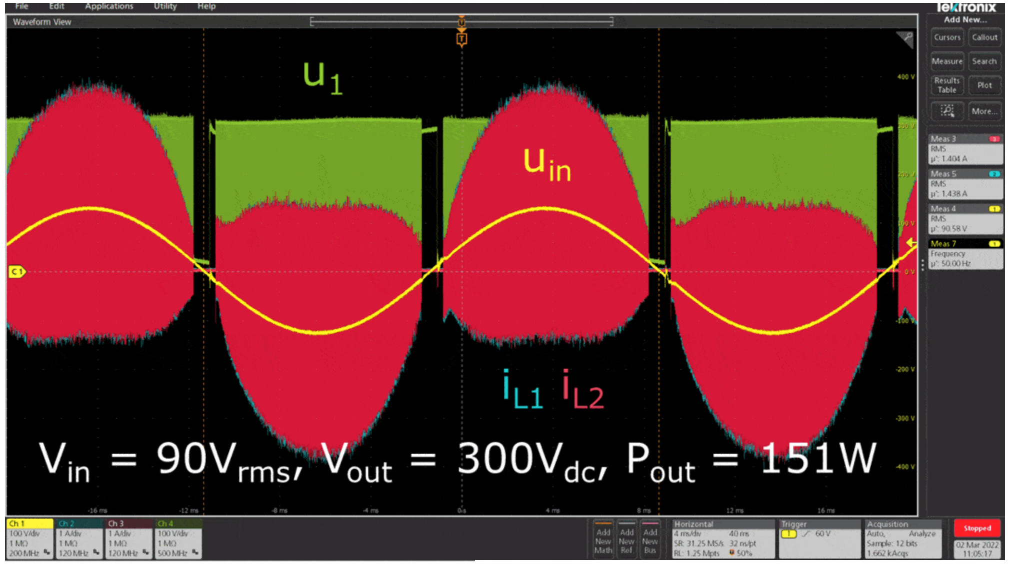
- **Fixed f_{sw} = 400kHz CCM PFC**
- **Effective 800kHz for EMI Filter**
- **Large Δi_L** (L = 35 µH, Litz Wire) for **natural ZVS** → For All Voltage Ranges
- **Operating-Point-Dependent U_{dc} variation** to always achieve ZVS
- Easy-to-Implement **Avg. Current Control**

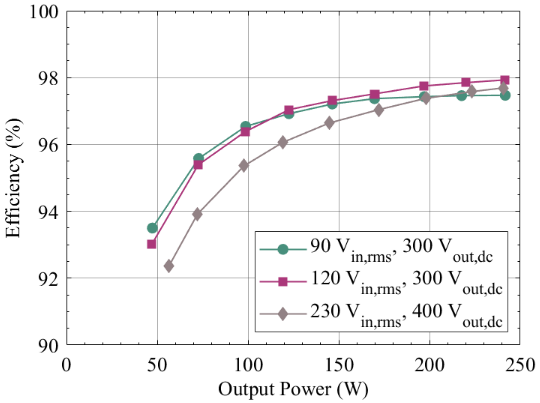
97.9% @ 240W, 120V$_{in}$, 300V$_{out}$

- CoolGaN™ GIT IPS
- 600V 140mΩ$_{typ}$

- CoolMOS™ Si-SJ
- 600V 48mΩ$_{typ}$





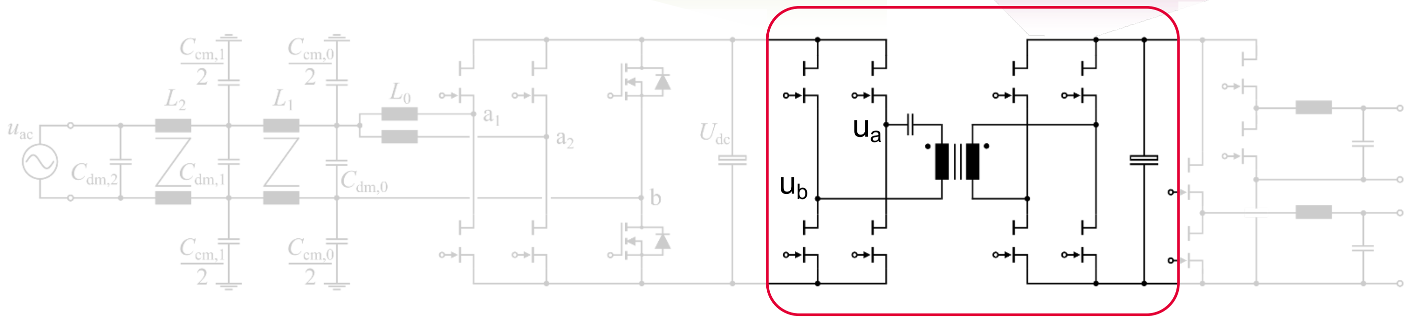


DCX stage details and measurement results

98.3% @ 240W, 300V_{in}, 52V_{out}

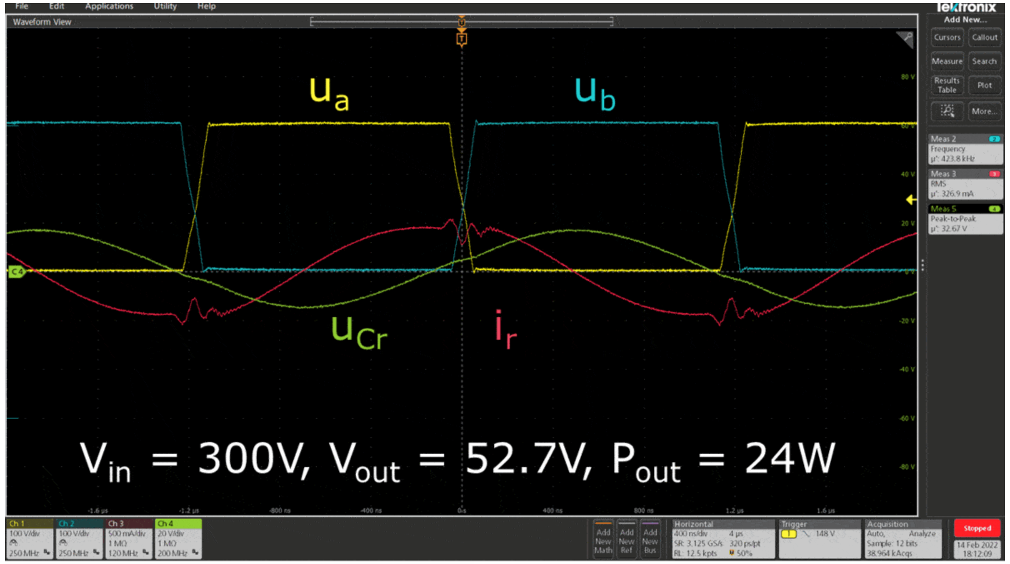
Unregulated DCX w/ Fixed Conversion Ratio (N_1:N_2 = 28:5 = 5.6)

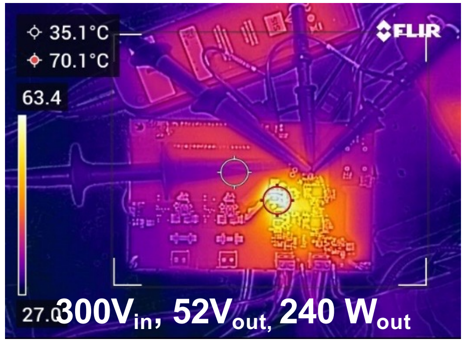
- **f_{sw} = 425kHz → Very High Dynamics**
- **Load independent ZVS** in **all operating points**
- **Small overall size** by **utilizing leakage inductance** (L_r = 12.6µH, Litz-Wire) of transformer **as resonance inductor**
- **Full-Bridge & Full-Bridge** configuration allows to start-up with discharged output with duty-cycle modulation

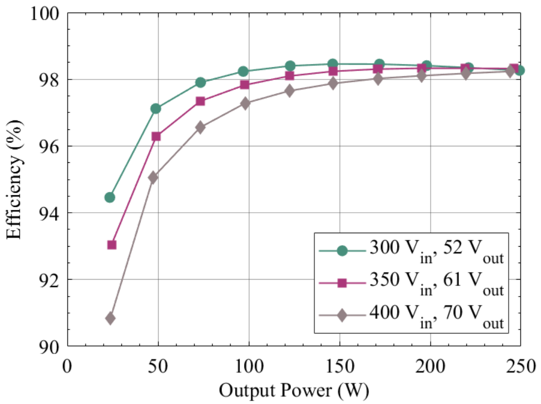


- **CoolGaN™ GIT IPS**
- **600V 140mΩ$_{typ}$**

- **CoolGaN™ SG**
- **100V 2.5mΩ$_{typ}$**







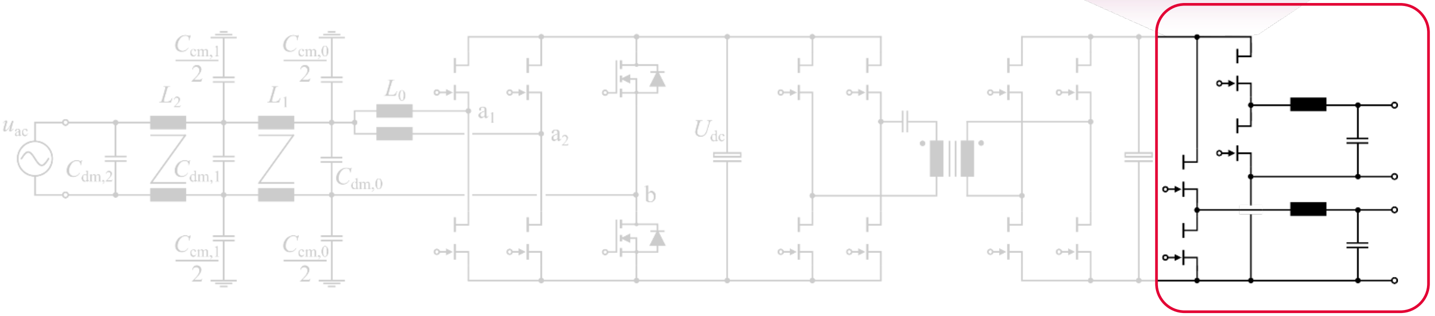
ZVS Buck Converter Stage

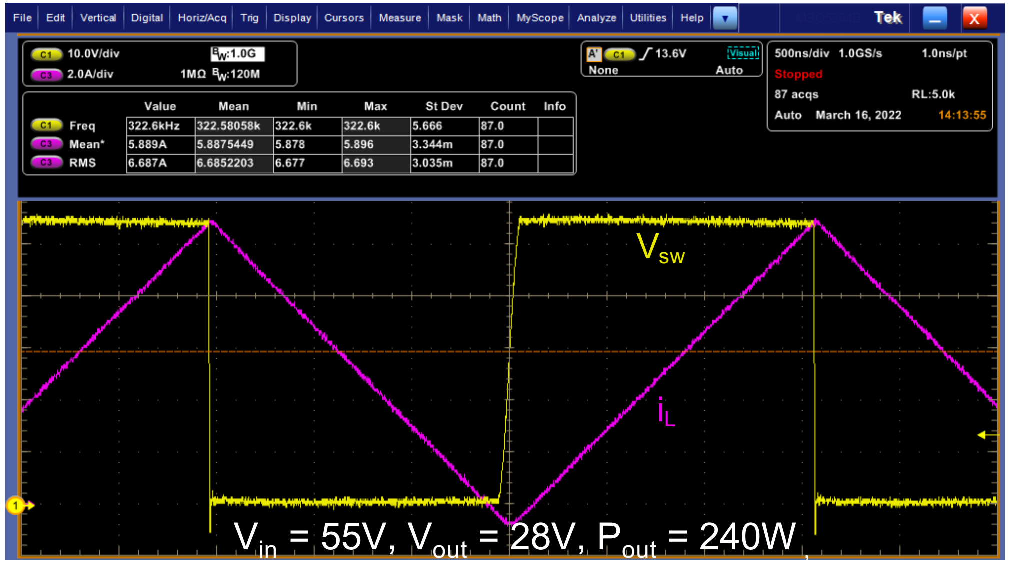
99.3% @ 240W, 55V_{in}, 48V_{out}

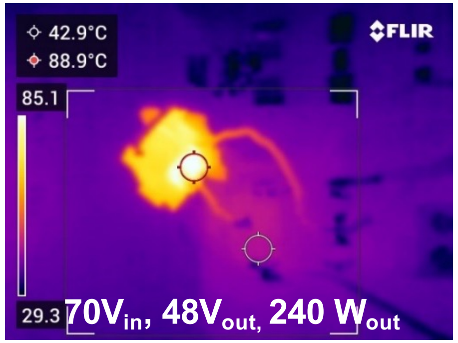
Full-ZVS Buck Stage

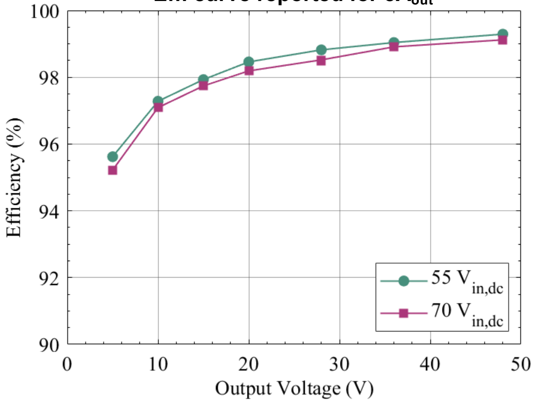
- **ZVS in All Operating Points**
- **Enabled by:**
  - **Variable frequency: f_{sw} = 120…420 kHz**
  - **Optimal Inductor Design** (L = 3.6 µH, Litz-Wire)

- **CoolGaN™ SG**
- **100V 2.5mΩ_{typ}**

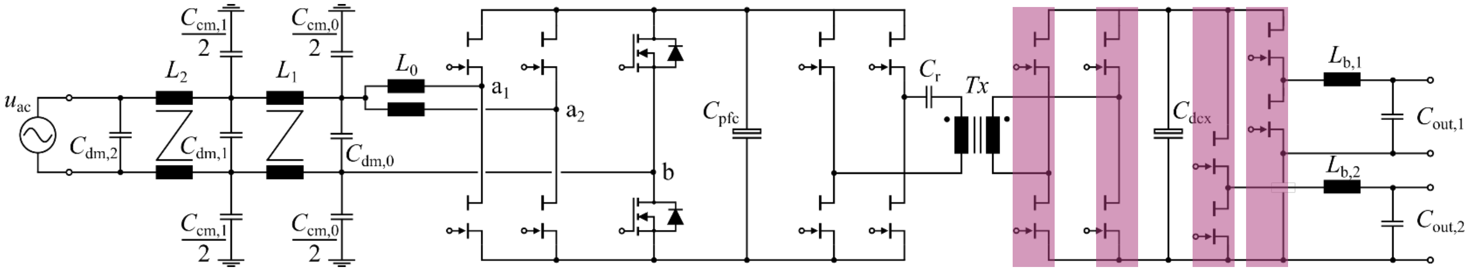






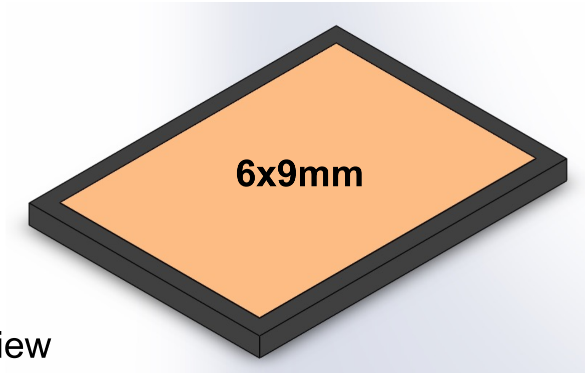


Outlook: 100V CoolGaN^{TM} SG Integrated Power Stage

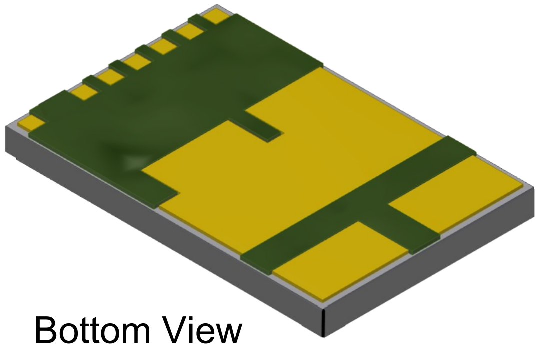


Size and BOM reduction with integrated 100V power stages

- **Half-bridge** multi-chip module (MCM) in **6x9 mm laminate package**:
  - **2x 100V 2.5mΩ_{typ} CoolGaN^{TM} SG HEMTs** in half-bridge configuration
  - **GaN-optimized half-bridge gate driver** with **regulated bootstrapping supply**
  - **ALL high-frequency capacitors included!** – PCB layout has no impact on switching performance or overshoot voltages, even on a single-layer PCB
- **Thermally optimized** package
  - Copious thermal microvias connecting to large PCB pads
  - Galvanically isolated top-side metal pad for easy heatsink attachment



Top View



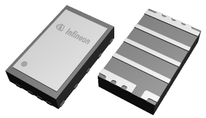
Bottom View

Conclusions

- **Unprecedented 240W USB-C charger power density (42 W/inch^3 & 113g uncased, 24W/inch^3 cased)**
- Thoroughly **optimized system performance** due to **Infineon's comprehensive technology portfolio and system expertise**:
  - **600V CoolGaN™ GIT Integrated Power Stage**
  - **100V CoolGaN™ Schottky Gate HEMTs**
  - **Matching gate drivers**
  - **Digital control with advanced modulation methods**
  - **Pareto multi-objective system optimization**

CoolGaN™ IPS 600/650 V

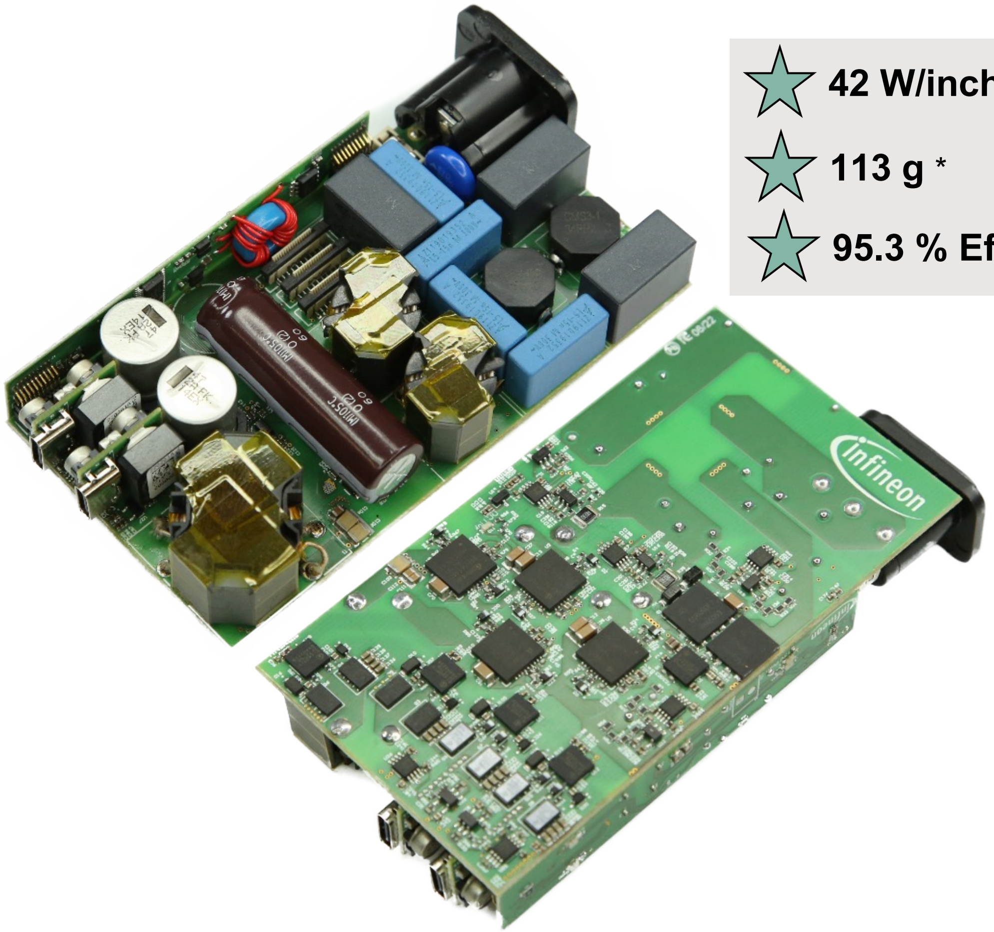
+



CoolGaN™ 100 V Schottky Gate HEMT

+

Matching Gate Drivers



★ **42 W/inch^3 ***

★ **113 g ***

★ **95.3 % Eff** (240W, 90Vrms)

* Uncased

Thank you for your interest!

Dr. Matthias J. Kasper, Dr. Jon Azurza & Dr. Gerald Deboy
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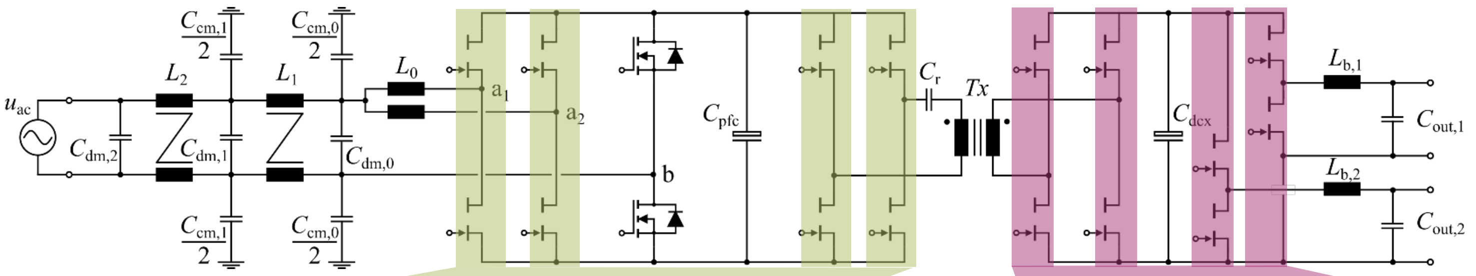
Part of your life. Part of tomorrow.

Infineon CoolGaN™ Solutions for 600V and 100V

Topology:
Interleaved Totem-pole & DCX & ZVS Buck converter

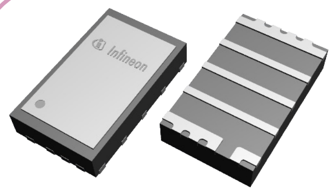


4x 600V 140mΩ$_{typ}$ Integrated GaN Half-Bridges

4x 100V 2.5mΩ$_{typ}$ Discrete GaN Half-Bridges

600V CoolGaN™ GIT Integrated Power Stage (IPS)

- Isolated digital input with digital-in, power-out building block
- Application configurable switching behavior
- Fast, highly accurate, and stable timing
- Thermally enhanced 8x8mm QFN-28 and 6x8mm QFN-26 packages



100V CoolGaN™ Schottky Gate (SG) HEMT

- Lower Q_{OSS} & more linear C_{OSS}
- Lower Q_G and no Q_{rr}
- 3x5 mm PQFN package with dual-sided cooling

+

TDI EiceDRIVER™ for SG GaN

- Optimized driving strength – no gate resistors
- Featuring TDI & active Miller clamp
- 1.8x1.8mm TSNP package