PwrSoC: Industry Adoption in High-Volume Applications

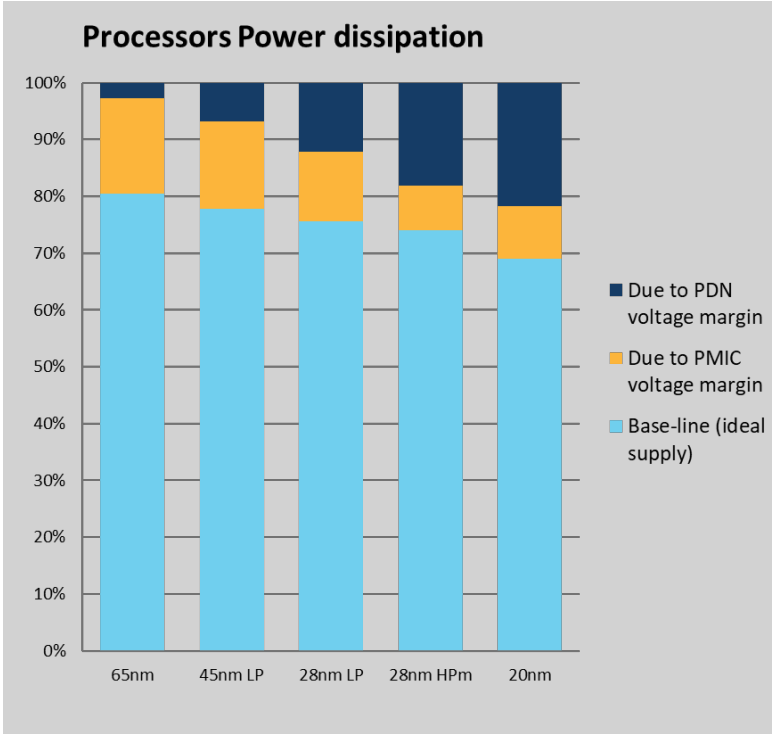
Francesco Carobolante, IoTissimo® LLC

Agenda

- Computing Requirements Driving Power Supply on Chip
- Drivers and Enablers
- Evolution of Products in the Market
- What Is Next?
- Conclusions

The Evolution of PwrSoC Requirements

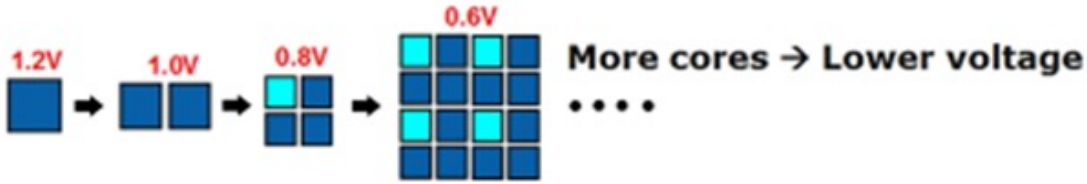
- Initial Motivation:
  - PDN-induced Voltage Margin

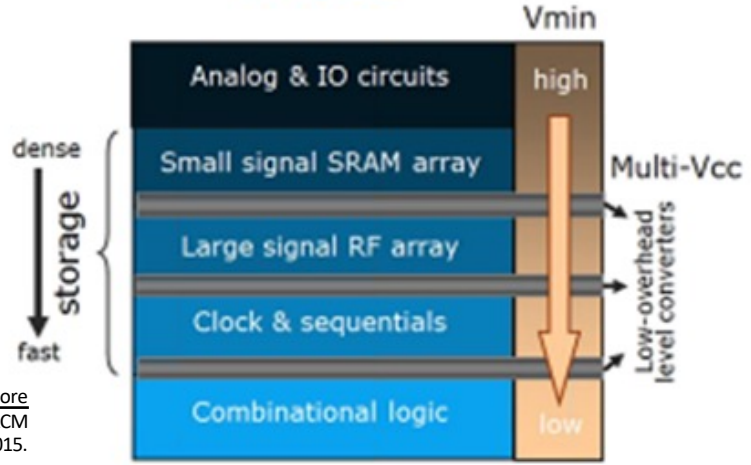


F. Carobolante, Power Supply on Chip: from R&D to commercial products, PwrSoC 2014

The Evolution of PwrSoC Requirements

- Initial Motivation:
  - PDN-induced V.
  - Granular Power Management

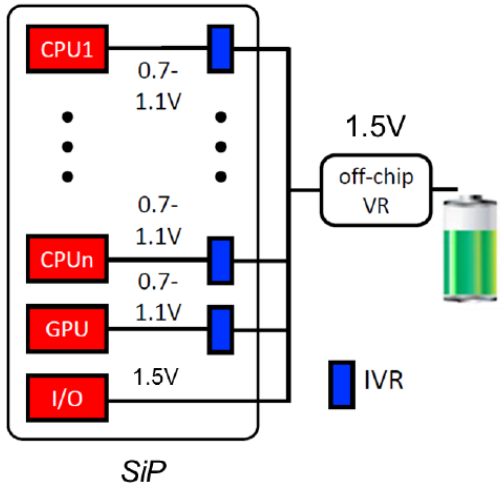


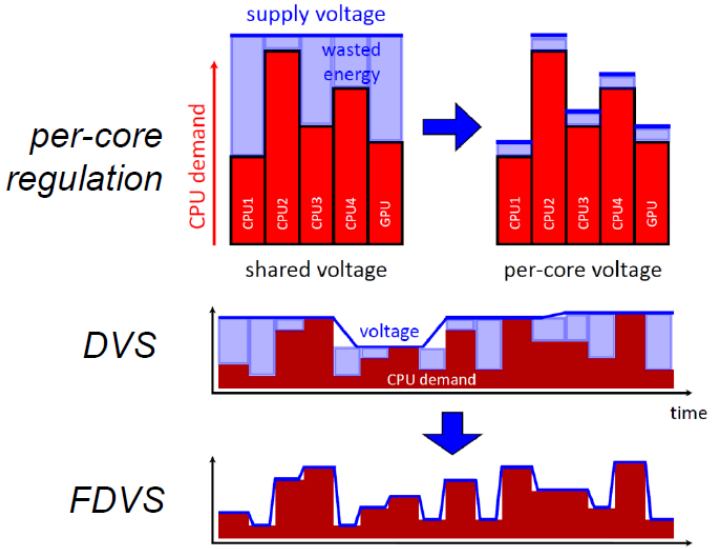


V. De et al, Fine-grain power management in manycore processor and System-on-Chip (SoC) designs, IEEE/ACM International Conference on Computer-Aided Design, 2015.

The Evolution of PwrSoC Requirements

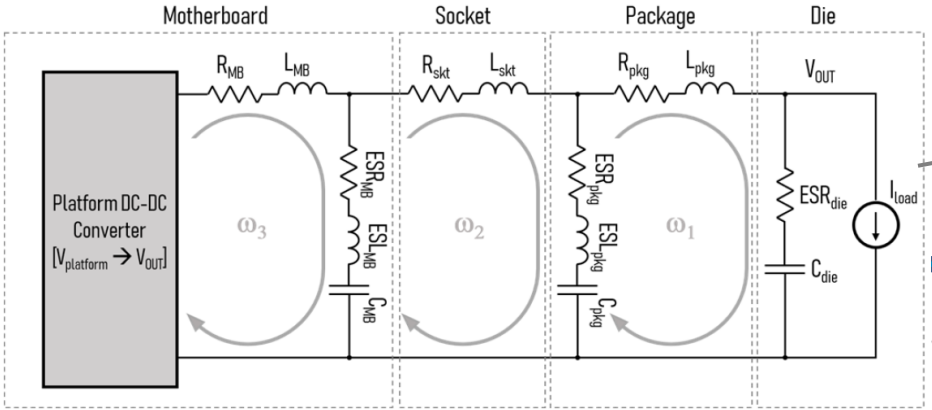
- Initial Motivation:
  - PDN-induced V_t Margin
  - Granular Power Delivery
  - Fast DVFS



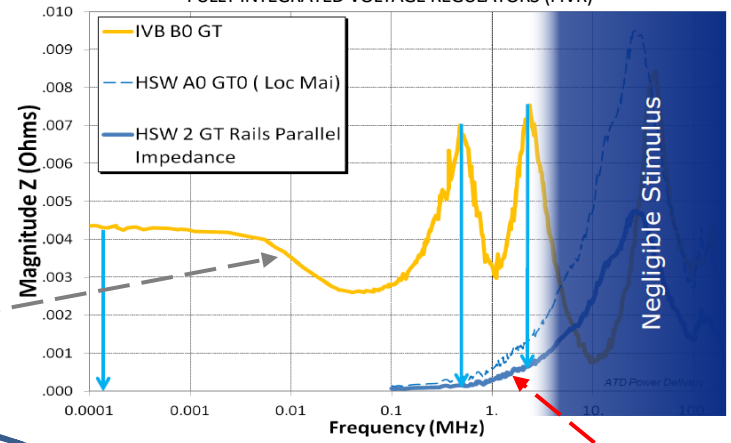


S. Kulkarni, Voltage Regulators with Integrated Inductors on Chip vs in Package, Applied Power Electronics Conference and Exposition, 2020.

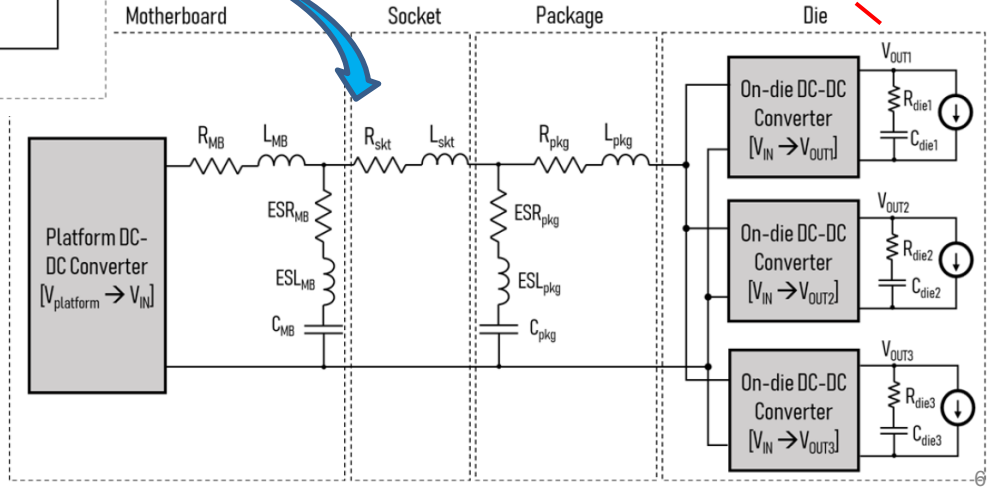
The Original Idea



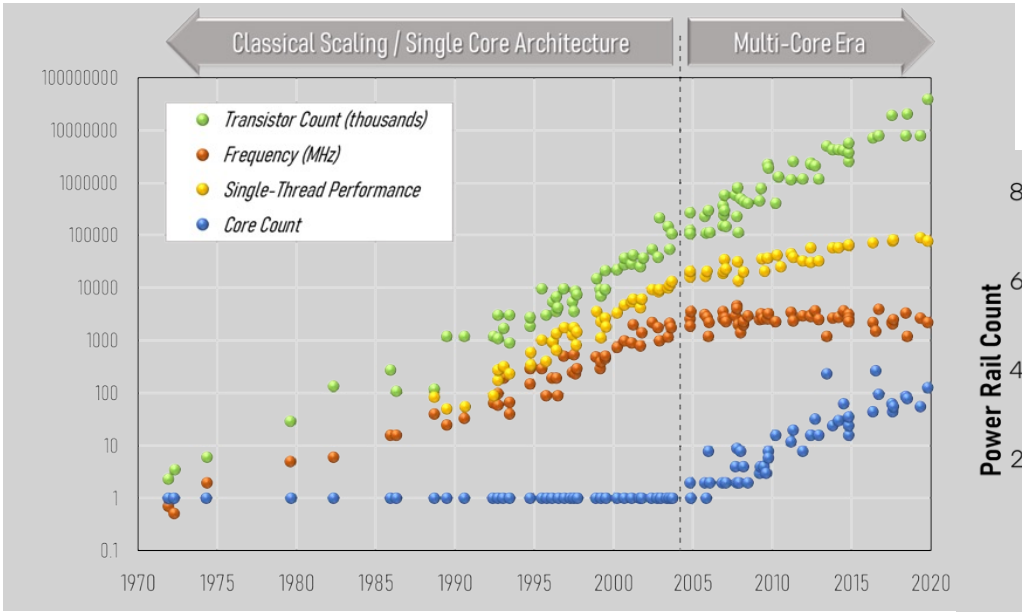
E. Burton, PACKAGE AND PLATFORM VIEW OF INTEL'S FULLY INTEGRATED VOLTAGE REGULATORS (FIVR)

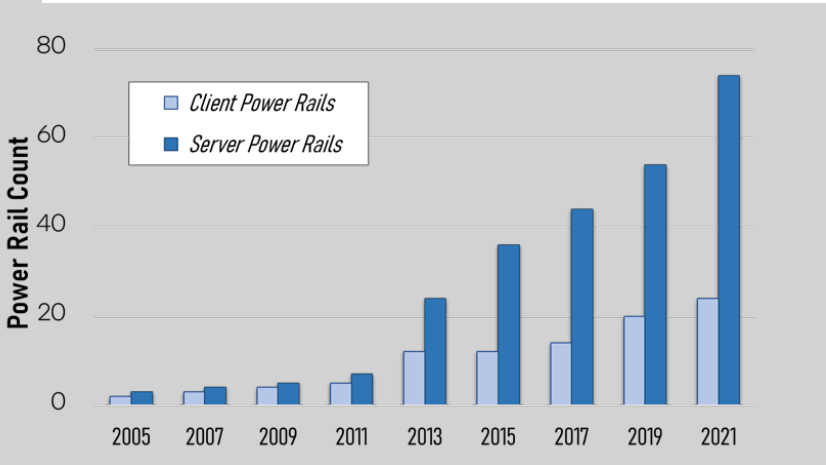


K. Radhakrishnan et al, Power Delivery for High Performance Microprocessors – Challenges, Solutions and Future Trends, IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume 11, Issue 4, April 2021.



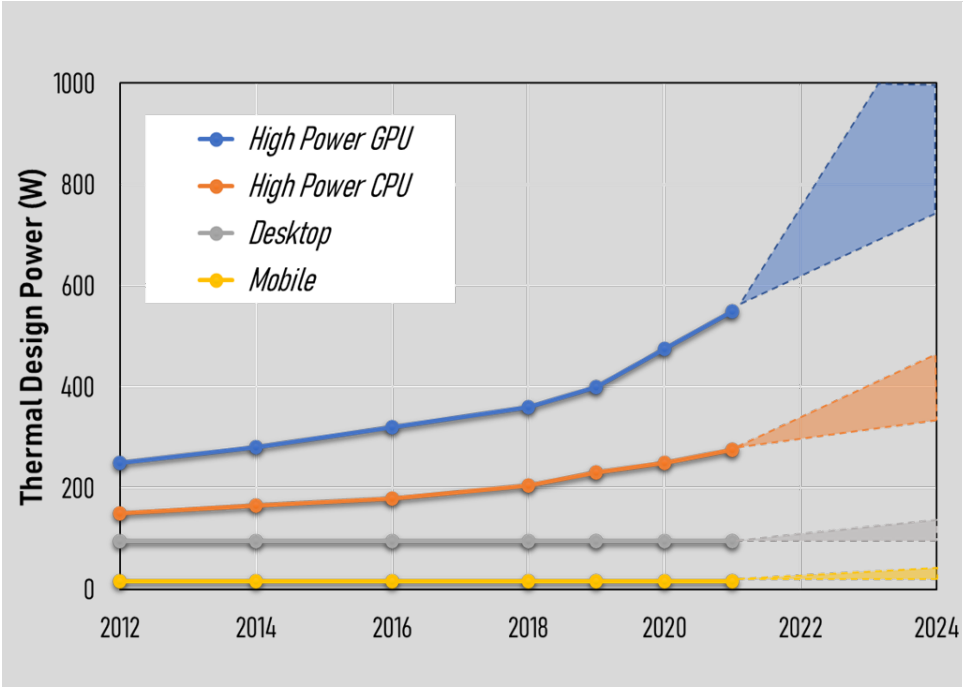
Meantime, on the Processor Side…



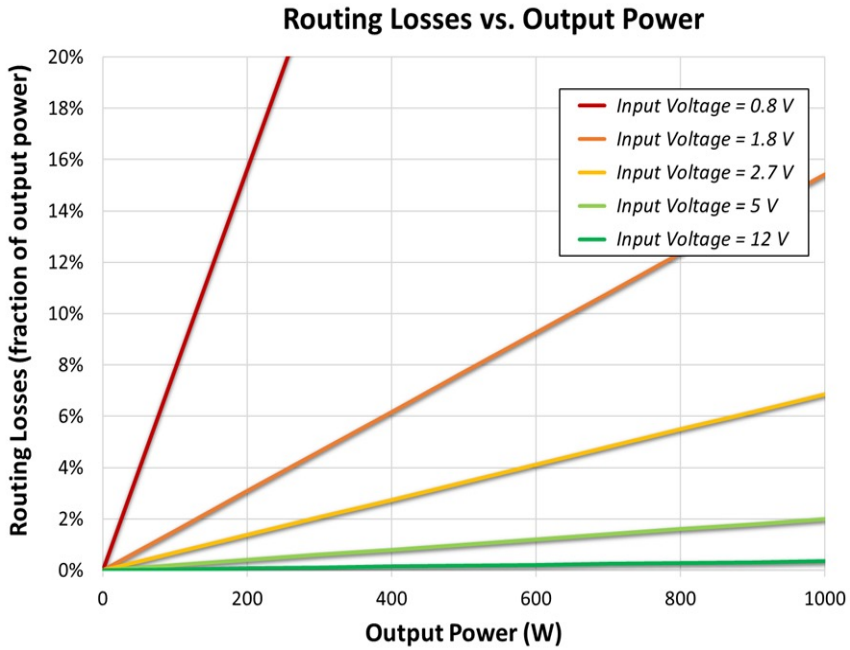


K. Radhakrishnan et al, Power Delivery for High Performance Microprocessors – Challenges, Solutions and Future Trends, IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume 11, Issue 4, April 2021.

The New “Power Wall”



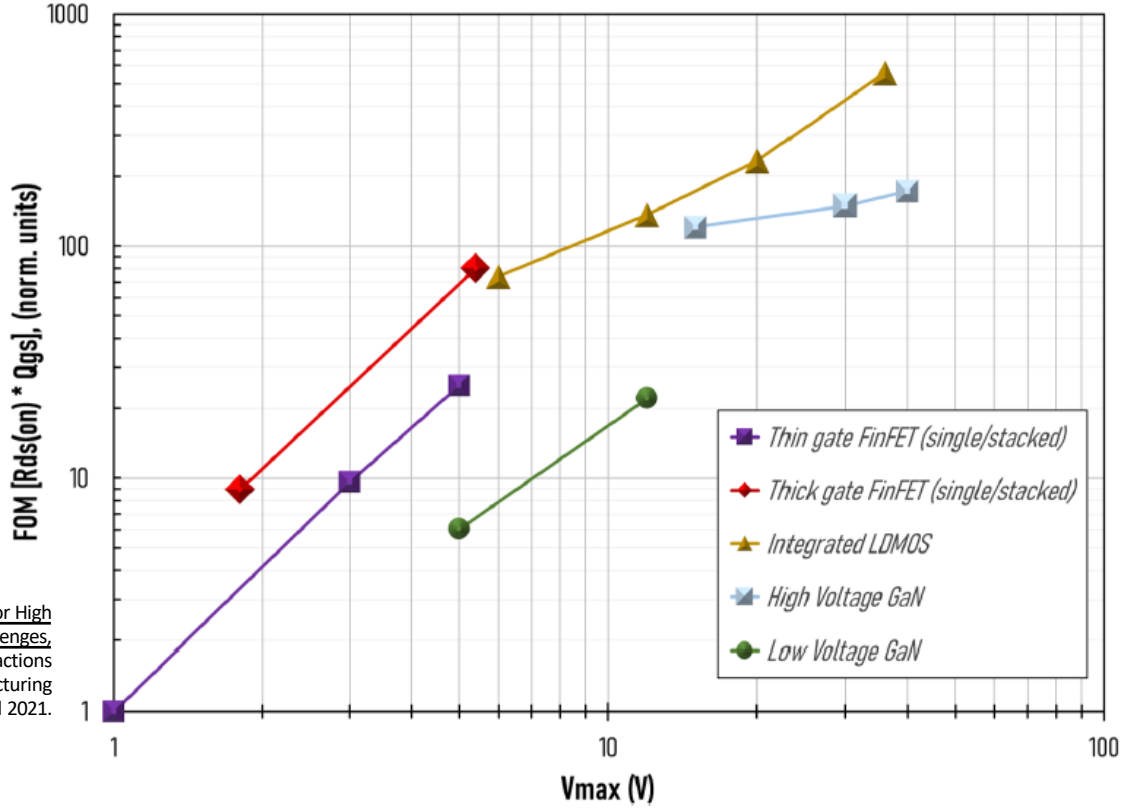
R. Mahajan, Advanced Packaging Architectures for Heterogeneous Integration, PwrSoC 2021



Assumes path resistance of 0.5 mΩ

K. Radhakrishnan et al, Power Delivery for High Performance Microprocessors – Challenges, Solutions and Future Trends, IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume 11, Issue 4, April 2021.

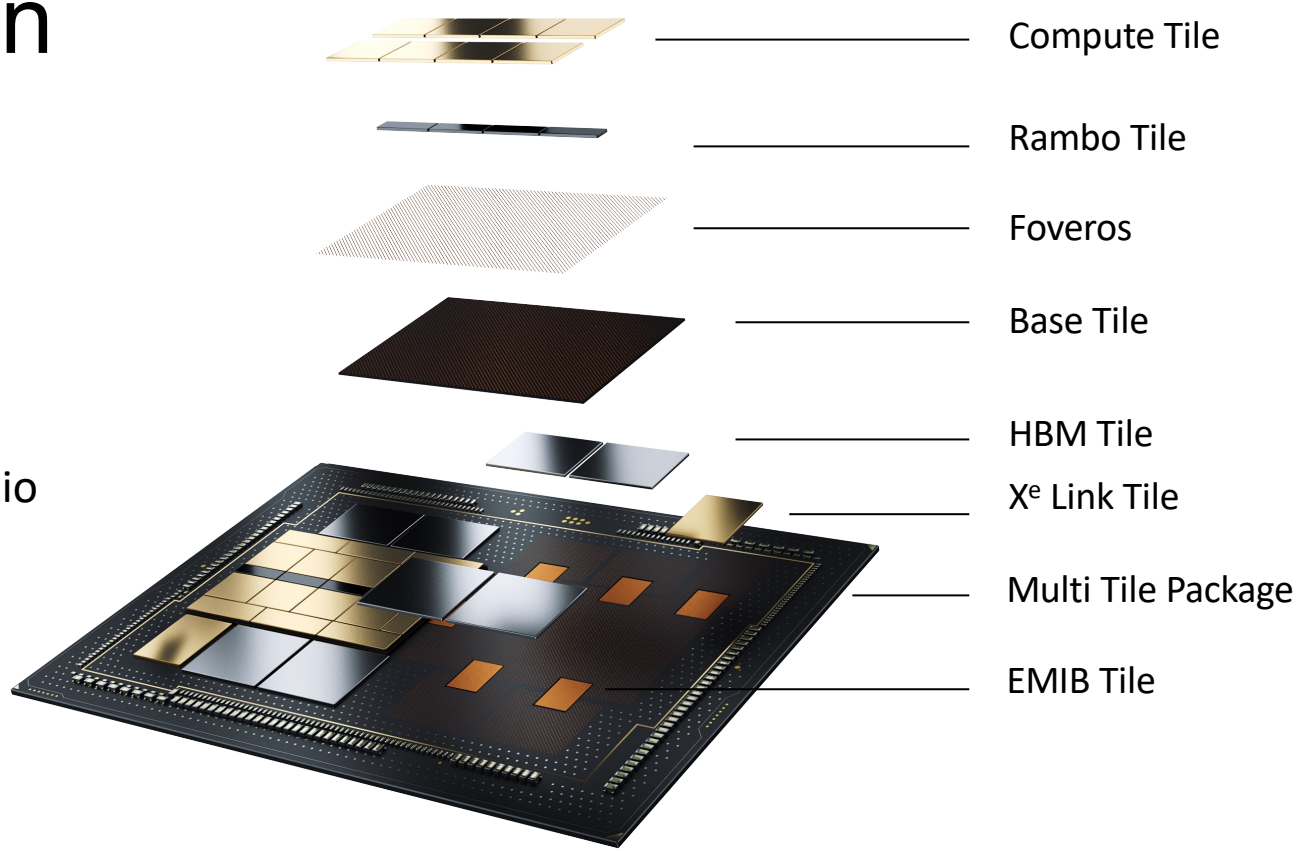
Two-stage Conversion Is Mandatory



K. Radhakrishnan et al, Power Delivery for High Performance Microprocessors – Challenges, Solutions and Future Trends, IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume 11, Issue 4, April 2021.

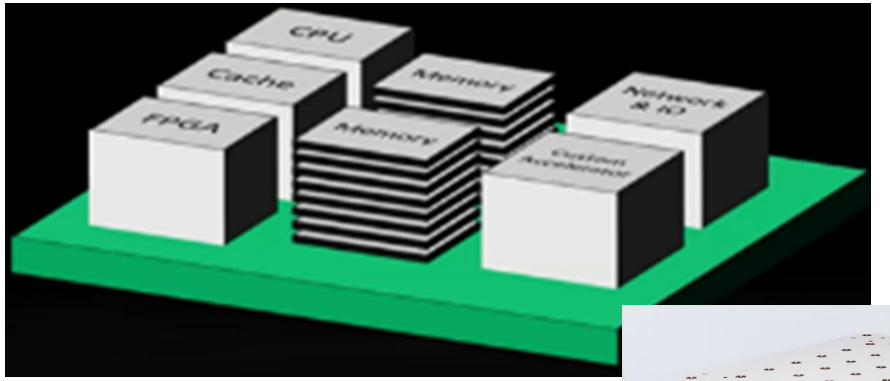
Now: Chiplets and Heterogeneous Integration

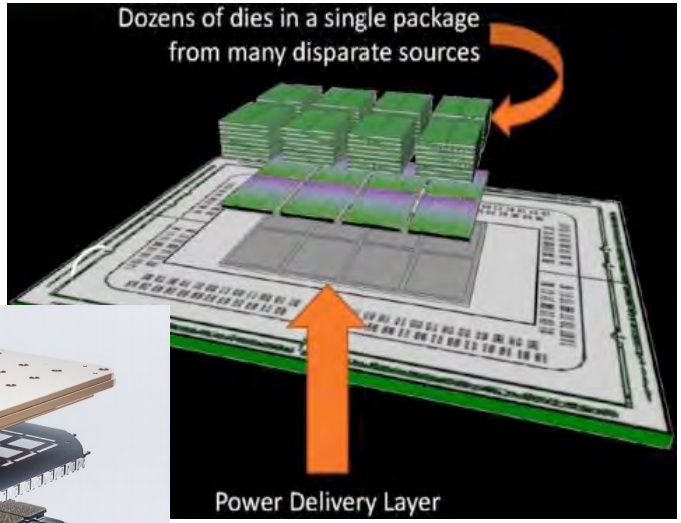
Intel Ponte Vecchio

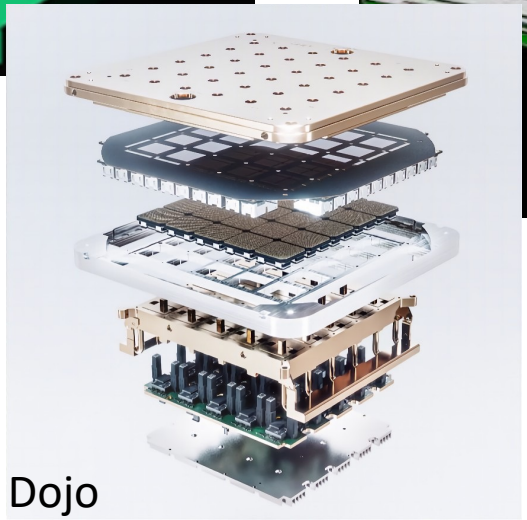


R. Mahajan, Advanced Packaging Architectures for Heterogeneous Integration, PwrSoC 2021

Shortest Path for Current Flow Is Vertical

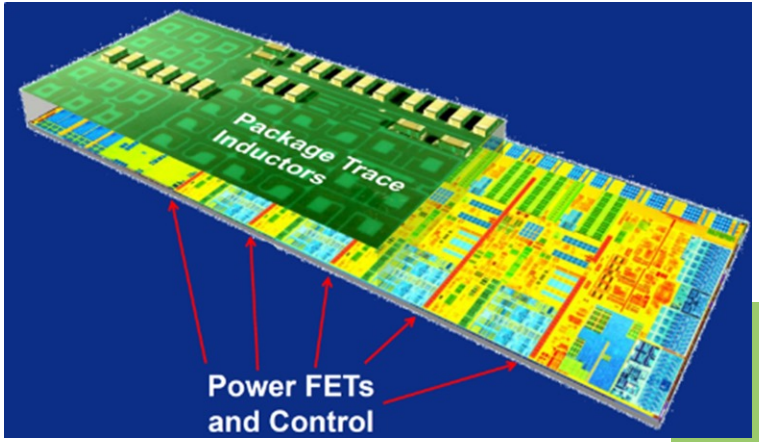






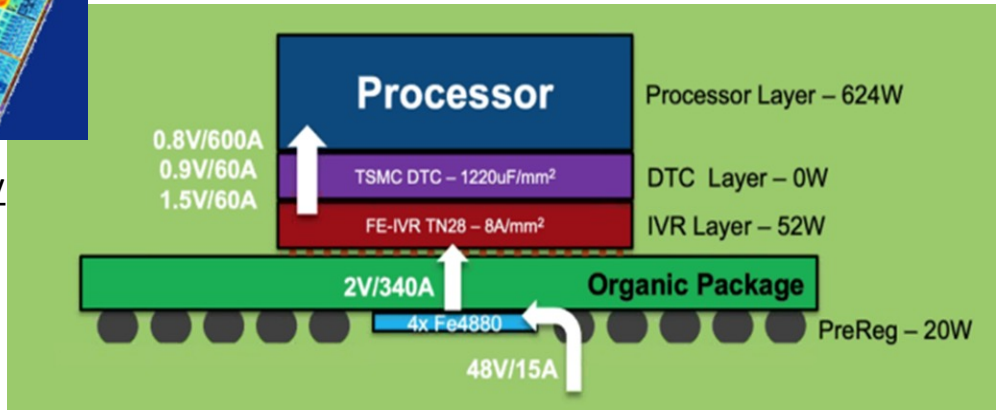
Tesla Dojo

How do we get there?

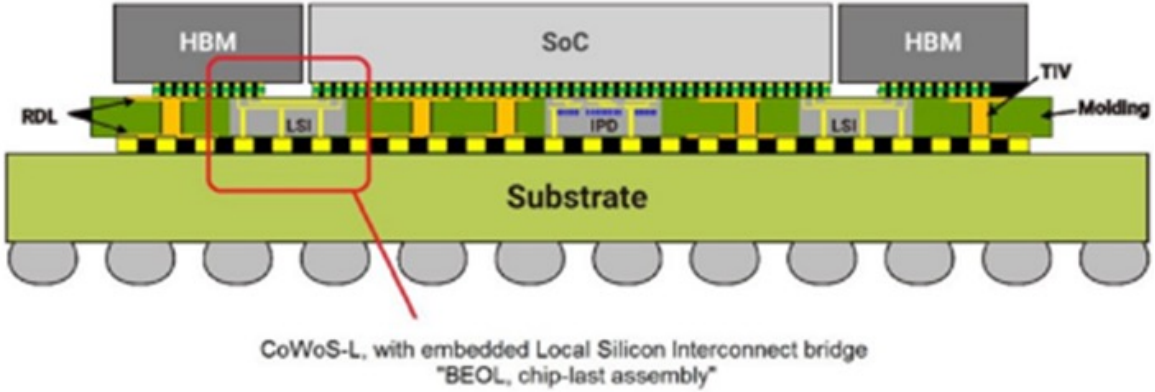


Package and Platform View of Intel's Fully Integrated Voltage Regulators (FIVR)

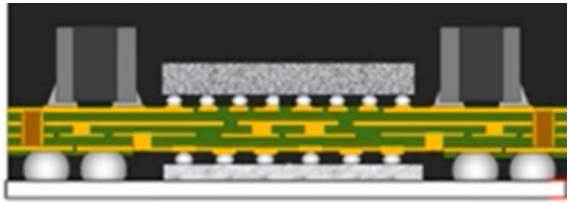
N. Sturcken, IEEE Power Electronics Society October 22, 2020, Integrated Power – A Virtual Panel Session



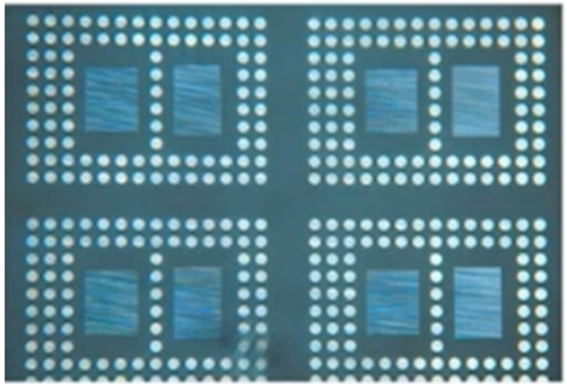
Many Options Are Proposed



Highlights of the TSMC Technology Symposium Part 2



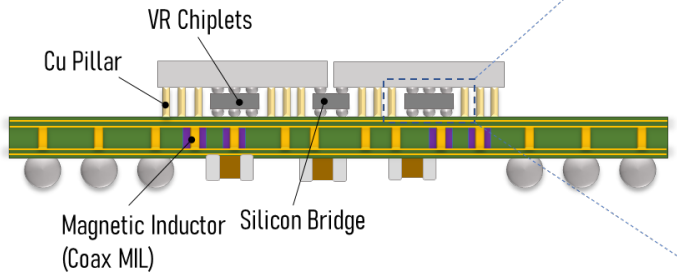
ASE's Double-Sided Mounting SiP

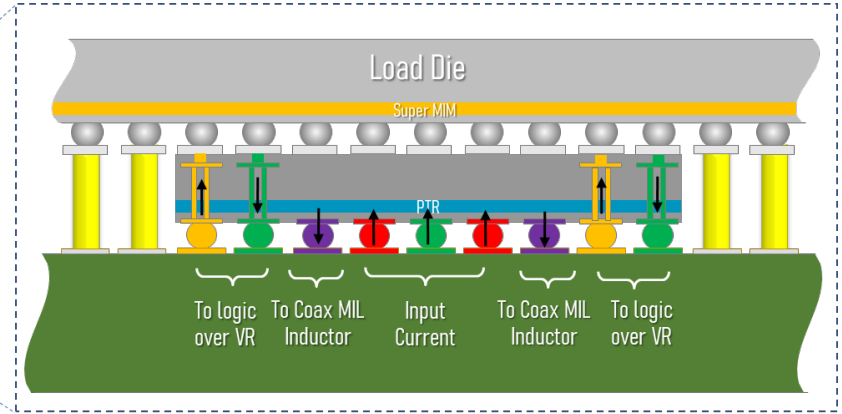


2020 11 18 IMAPS' webinar
Enabling a Path to System Level Solutions

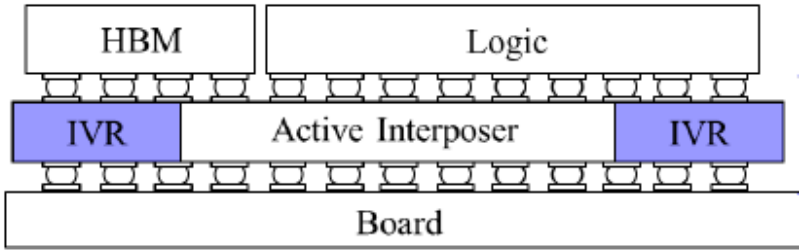
Many Options Are Proposed

K. Radhakrishnan, Power Delivery for Heterogeneous Systems, Connecting Heterogeneous Systems Summit, September 2021.





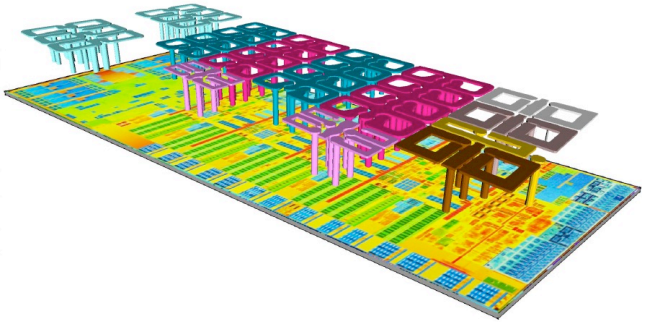
IVR on Active Interposer

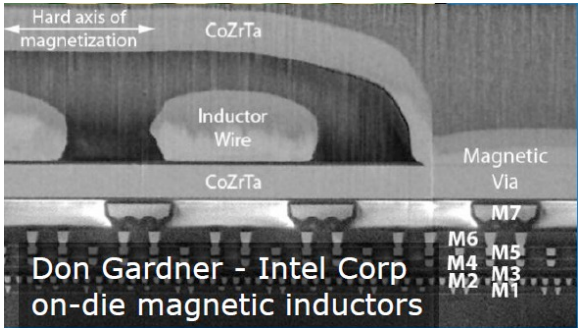


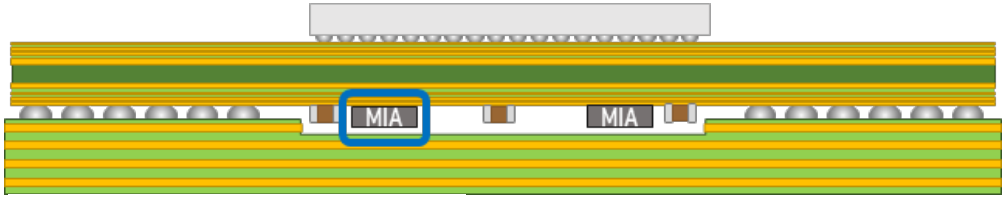
S. Kim et al., Power Integrity Comparison of Off-chip, On-interposer, On-chip Voltage Regulators in 2.5D/3D Ics

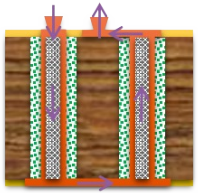
PWRSOC IS NOW INTO EVERYDAY PRODUCTS

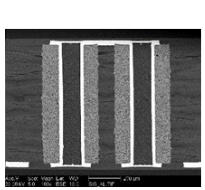
Product Generations: **Intel**

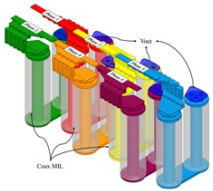






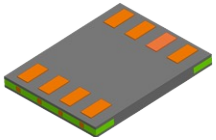


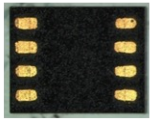




MIA Module

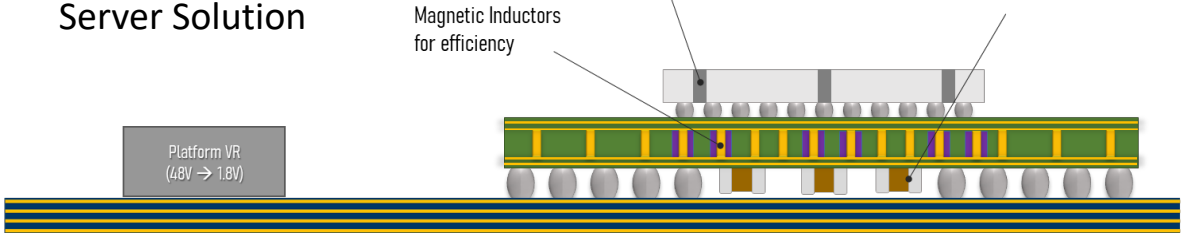
MIA – Top View





Client Solution

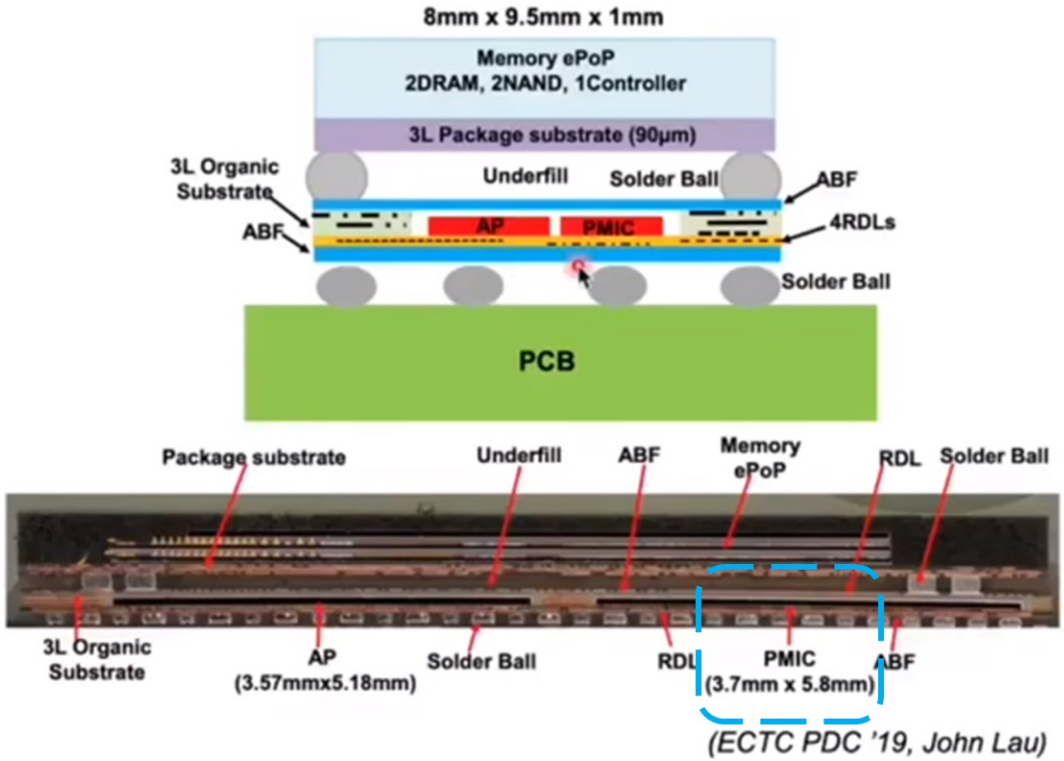
Server Solution



R. Mahajan, Advanced Packaging Architectures for Heterogeneous Integration, PwrSoC 2021

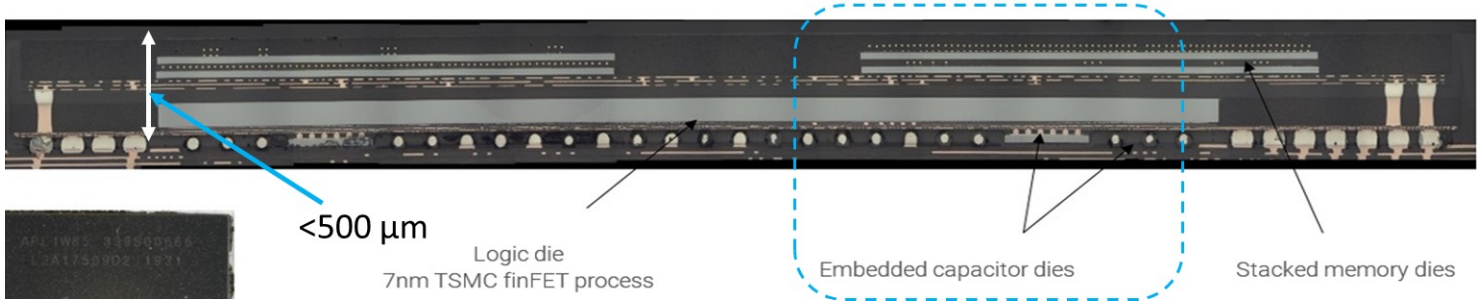
Product Generations: **Samsung**

- This 2018 Product shows initial integration of Power Management
- **Where is Samsung in 2022?**



Product Generations: **Apple**

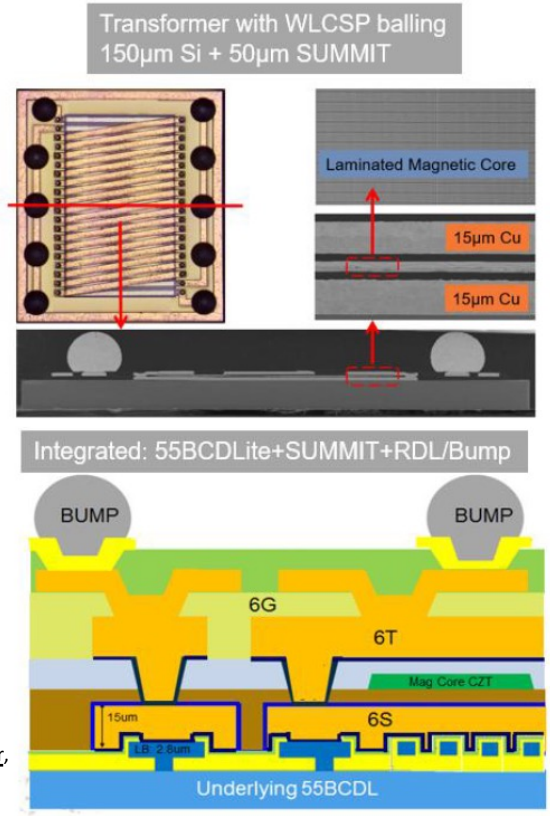
Apple A13 designed by Apple (2019)
(manufactured by TSMC, 7 nm finFET process and packaged by TSMC's InFO technolgy)



(2021) Apple M1 Pro (and M1 Max) utilize 3 (or more) **IVR**'s for power delivery

Global Foundries Joins the Path

- GF joins TSMC in providing integrated inductors in silicon
- Others are working on it



L. Peng et al., Silicon-based Ultimate Miniature Magnetic Inductors and Transformers (SUMMIT) for High-frequency Switching Regulator, PwrSoC 2021

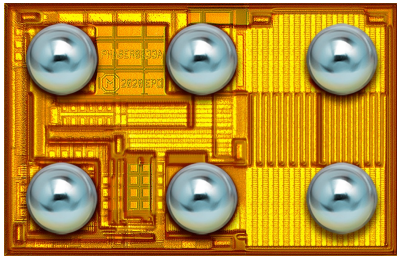
What Is “More Than Moore”?

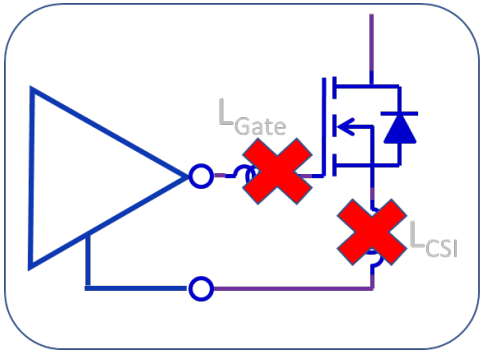
- Heterogeneous Integration enables:

1. Higher Performance and Efficiency
   - Integration of Passive Components
   - Integration of III-V Semiconductors
2. Co-optimization of Signal & Power Integrity
   - FO-packaging
   - TSV’s
   - WoW and CoW
   - Silicon Interposers and Silicon Bridges

GaN Is Making Great Progress

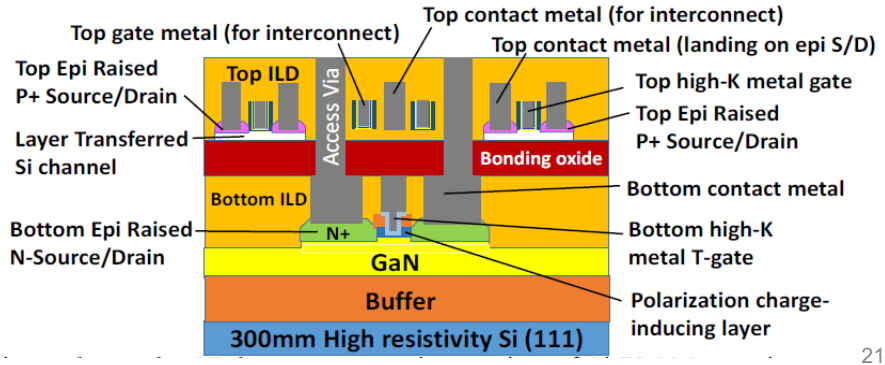
- Integration of Power and Drivers





A. Lidow, APEC 2021 Industrial Session presentation number 3017

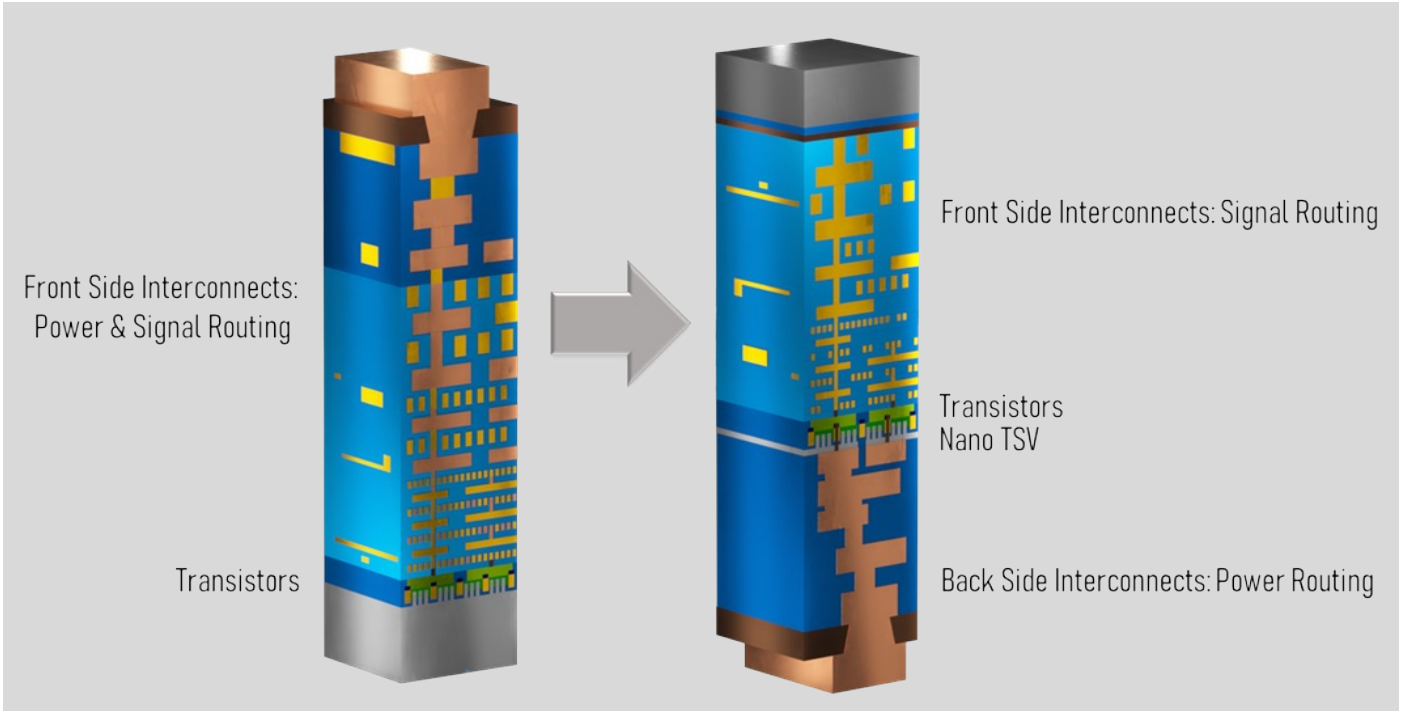
- Heterogeneous Integration of Low-Voltage Si+GaN Processes



H.W. Then et al., 3D heterogeneous integration of high performance high-K metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications, IEDM19-402

Process Is Driven by Power Routing

Signal on one side – Power from the other side



R. Mahajan, Advanced Packaging Architectures for Heterogeneous Integration, PwrSoC 2021

Conclusions

- Incorporating Power Management in High Performance SoC is mandatory! Heterogeneous Integration is the solution.
- Each application has different requirements and constraints: there is no single solution!
- High Performance Computing requires Two-stage architecture for any supply ≥5 V. GaN is a good option for the first stage.
- Back-end processing has evolved dramatically: FO packages, TSV, WoW and CoW bonding are now in volume production.
- Computing Industry has hit the “Power Wall”: Performance and Efficiency improvements require bringing Power Management into the System Architecture – from the start of the project!

Many Thanks to the IEEE HIR Members!

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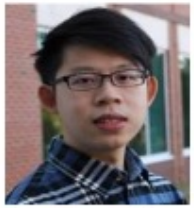

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Slide 1

Thank You for Listening!

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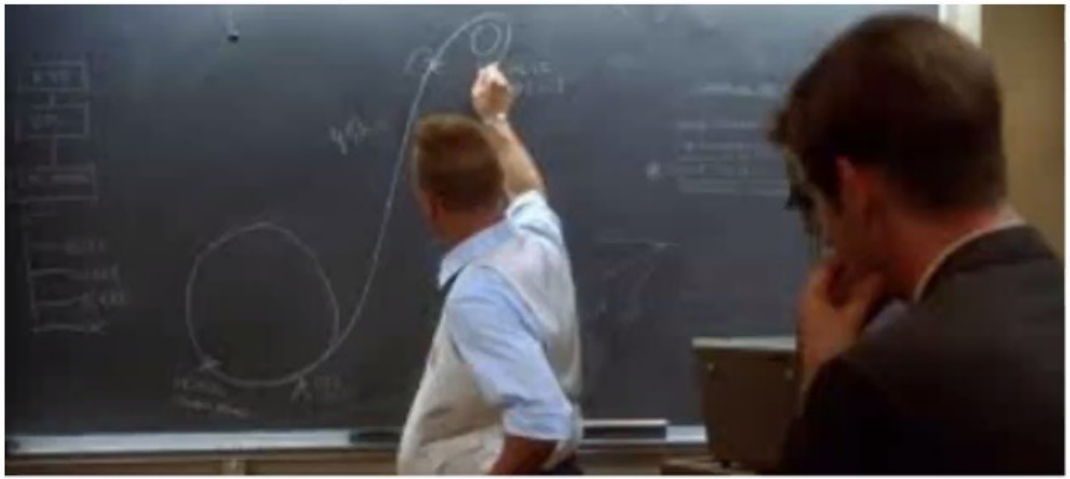
Apollo 13 – Universal Pictures



"Power is Everything"*

John Aaron- Apollo 13 Flight Controller